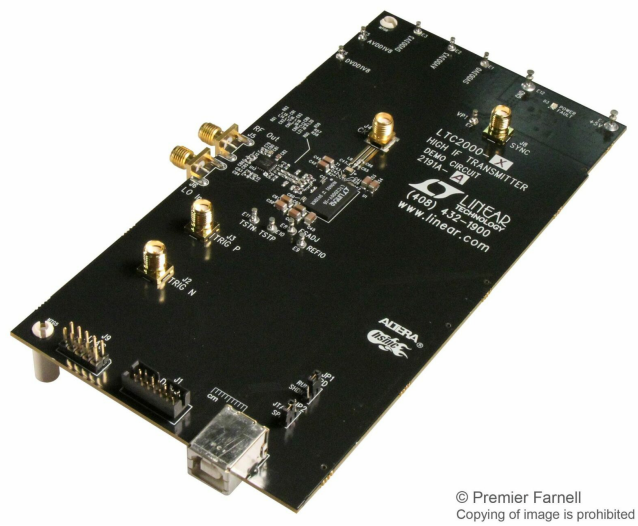

LINEAR TECHNOLOGY LTC2000-16 Demonstration Circuit Installation Guide

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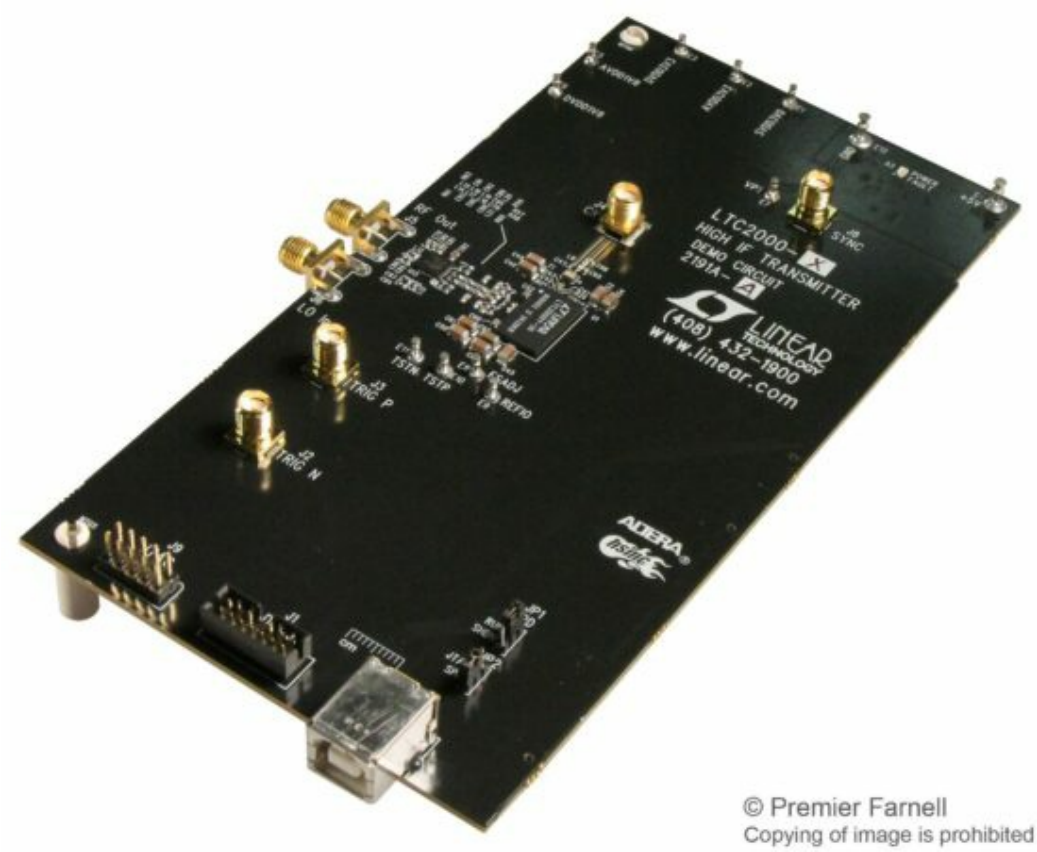


LTC2000, LTC2000A
16-, 14-, 11-Bit, 2.5Gsps to 2.7Gsps DACs

DESCRIPTION

Demonstration circuit 2085 supports the LTC®2000 and LTC2000A, a high speed, high dynamic range family of DACs. It was specially designed for applications that require differential DC coupled outputs. DC2085 supports the complete family of the LTC2000 including 16, 14 and 11 bit parts. For all the variations see Table 1.

The circuitry on the analog outputs is optimized for analog frequencies from DC-1.08GHz.

Design files for this circuit board are available at
http://www.linear.com/demo/DC2085

Table 1. DC2085 Variants

DC2085 VARIANTS	PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	OUTPUT FREQUENCY
DC2085A-A	LTC2000-16	16-Bit	2.5Gsps	DC-1000MHz
DC2085A-B	LTC2000-14	14-Bit	2.5Gsps	DC-1000MHz
DC2085A-C	LTC2000-11	11-Bit	2.5Gsps	DC-1000MHz
DC2085A-D	LTC2000A-16	16-Bit	2.7Gsps	DC-1080MHz
DC2085A-E	LTC2000A-14	14-Bit	2.7Gsps	DC-1080MHz
DC2085A-F	LTC2000A-11	11-Bit	2.7Gsps	DC-1080MHz

PERFORMANCE SUMMARY

Specifications are at TA = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage – DC2085	This supply must provide up to 800mA	4.8	5.0	5.2	V
Sampling Frequency (Sample Clock Frequency)		300		2500 or 2700	MHz
Sample Clock Level (Single-Ended)	Use a 50Ω Source	0		15	dBm
LVDS Inputs	Differential Input Voltage Range	±0.2		±0.6	V
	Common Mode Voltage Range	0.4		1.8	V

QUICK START PROCEDURE

DC2085 is easy to set up to evaluate the performance of the LTC2000. Refer to Figure 1 for proper measurement equipment set-up and follow the procedure below:

Setup

If the Altera Stratix IV GX FPGA Development Kit was not supplied with the DC2085 demonstration circuit, follow the Altera Stratix IV demo manual to install the required software and for connecting the Altera Stratix IV to the DC2085 and to a PC.

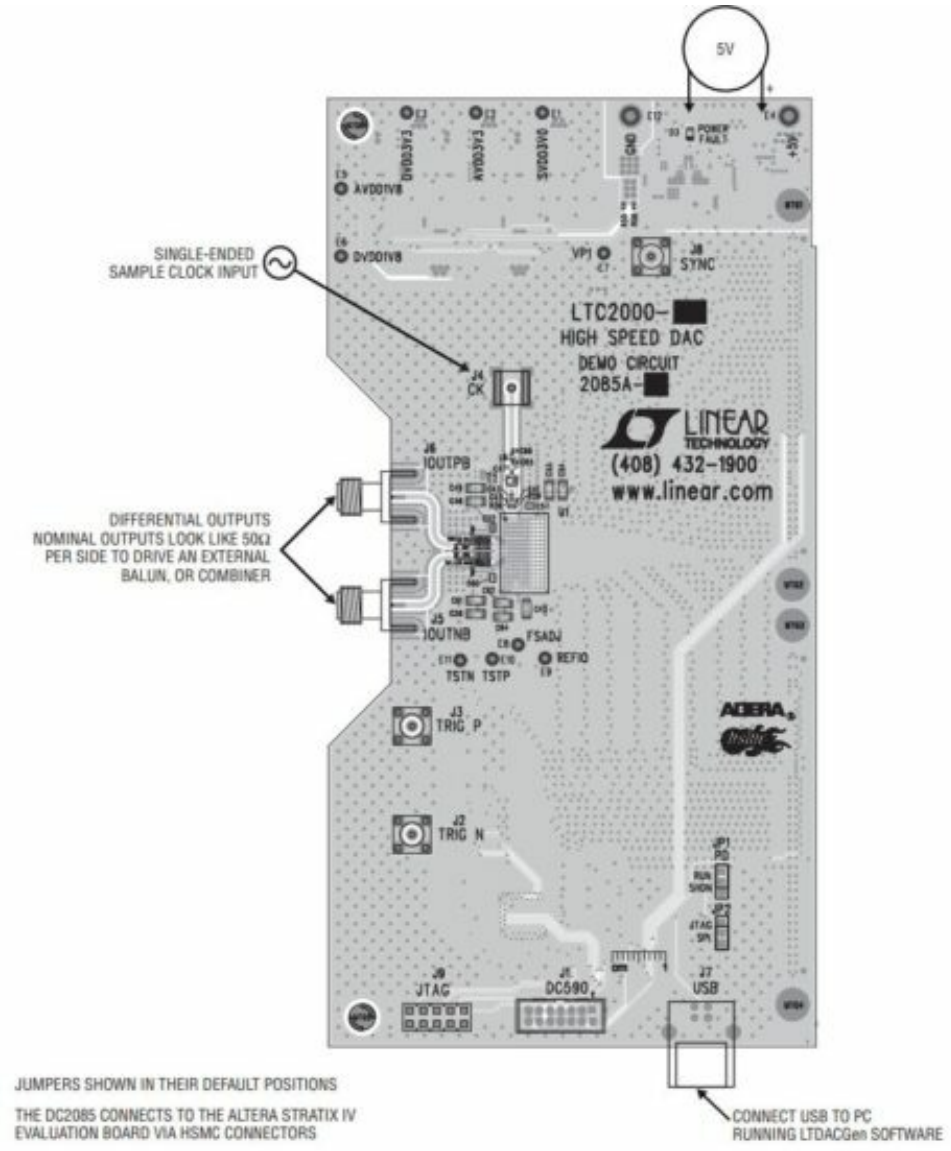


Figure 1. DC2085 Setup (zoom for details)

HARDWARE SETUP

SMAs

J2 & J3: Differential Trigger Input. Apply a signal to J2 from a 50Ω driver. Absorptive filters are required for data sheet performance. Use J2 and J3 if the trigger is a differential signal.

J4: Sample Clock Input. Apply a clock signal to this SMA connector from a 50Ω driver. A 0dBm clock source should be sufficient, but for best phase noise and jitter performance, use the highest possible amplitude and slew rate, up to 15dBm.

J5 & J6: Differential Output Signals. These SMAs provide access to the differential outputs of the DAC. The output impedance is designed to be 50Ω at each SMA, or 100Ω differential. Connect an external balun or combiner to these pins to drive a single-ended spectrum analyzer. Linear Technology has various coupon boards for specific frequencies and applications. More information is available at www.linear.com.

J8: SYNC. This SMA is to provide access to the sync pin of the LT8614. It is not used in normal use.

Turrets

+5V: Positive Input Voltage for the DAC and Digital Circuits.
This voltage feeds a series of regulators that supply the proper voltages for the DAC. The voltage range for this turret is 4.8V to 5.2V. Note: For close-in phase noise plots, driving this voltage is not ideal. There is a known 20kHz noise hump in the spectrum that is generated by the regulators. For the best phase noise performance,

back drive the onboard regulators with the provided turrets from a low noise supply.

GND: Ground Connection. This demo board has only a single ground plane. This turret should be tied to the GND terminal of the power supply being used.

SVDD3V0: Optional 3.0V Input. This pin is connected directly to the SVDD pin of the DAC. It requires a supply that can deliver up to 100mA. Driving this pin will shut down the onboard regulator.

AVDD3V3: Optional 3.3V Input. This pin is connected directly to the AVDD3V3 pin of the DAC. It requires a supply that can deliver up to 200mA. Driving this pin will shut down the onboard regulator.

DVDD3V3: Optional 3.3V Input. This pin is connected directly to the DVDD3V3 pin of the DAC. It requires a supply that can deliver up to 50mA. Driving this pin will shut down the onboard regulator.

AVDD1V8: Optional 1.8V Input. This pin is connected directly to the AVDD1V8 pin of the DAC. It requires a supply that can deliver up to 1A. Driving this pin will shut down the onboard regulator.

DVDD3V3: Optional 1.8V Input. This pin is connected directly to the DVDD1V8 pin of the DAC. It requires a supply that can deliver up to 500mA. Driving this pin will shut down the onboard regulator.

VP1: This is a test point that is at the output of the onboard switching regulator. It is meant for test purposes. It can also be driven to 2.5V to shut down the output of the switching regulator.

TSTP & TSTN: These pins are tied directly to the TSTP and TSTN pins of the DAC. They can be used to measure the internal temperature and timing of the LVDS inputs. FSADJ: This is an optional pin that is tied directly to the FSADJ pin of the DAC. It can be used to set the full-scale output current of the DAC. In normal operation this pin is tied to GND through 500Ω to set a current of 40mA at the output.

REFIO: This pin is tied directly to the REFIO pin of the DAC and is used to set the reference voltage for the DAC. Normally it is internally set to 1.25V but can be overdriven with an external voltage from 1.1V to 1.4V.

Jumpers

The DC2085 demonstration circuit should have the following jumper settings as default positions.
JP1: PD. In the RUN position this pin results in normal operation of the DAC. In the SHDN position the DAC is powered down. (Default: RUN or up)

JP2: SPI and JTAG. This jumper selects how the FPGA is programmed. In the SPI position the FPGA is programmed from the onboard FTDI chip and the LTDACGen software. In the JTAG position the J9 is used with a JTAG programmer to program the FPGA. (Default: SPI or down)

Connectors

J1: DC590. This is an optional header that can be used to program the DAC with the DC590. (Default: removed)
J9: JTAG. This is an optional header that can be used to program the FPGA through a JTAG programmer. (Default: removed)
J7: USB. Connect a USB cable from J7 to a computer with the LTDACGen software installed.
J10 & J11: HSMC Connectors. These connectors are designed to connect to the Altera Stratix IV development board. All of the communication between the FPGA and the DAC is routed through these connectors.

APPLYING POWER AND SIGNALS TO THE DC2085 DEMONSTRATION CIRCUIT

If a Stratix IV demo board is used to supply data to the DC2085, the two boards should first be bolted together and a proper connection should be made. If Linear Technology provided the Stratix IV board the proper bit file is already installed in flash memory and will begin to operate when the board is powered on. If an unprogrammed FPGA board is used, refer to the appropriate documentation on how to program it.

Power should be applied to the system in this order:

1. Connect the Altera board to the provided power supply.
2. Connect the USB cable to J7.
3. Apply a clock to J4.
4. Connect any optional output board to J5 and J6.
5. Turn on the voltage to the Altera board.
6. Connect the 5V from a bench supply to the +5V turret on the DC2085.
7. Open the LTDACGen software and hit connect.

LTDACGen should report back that it is connected to the FPGA. See Figure 2:

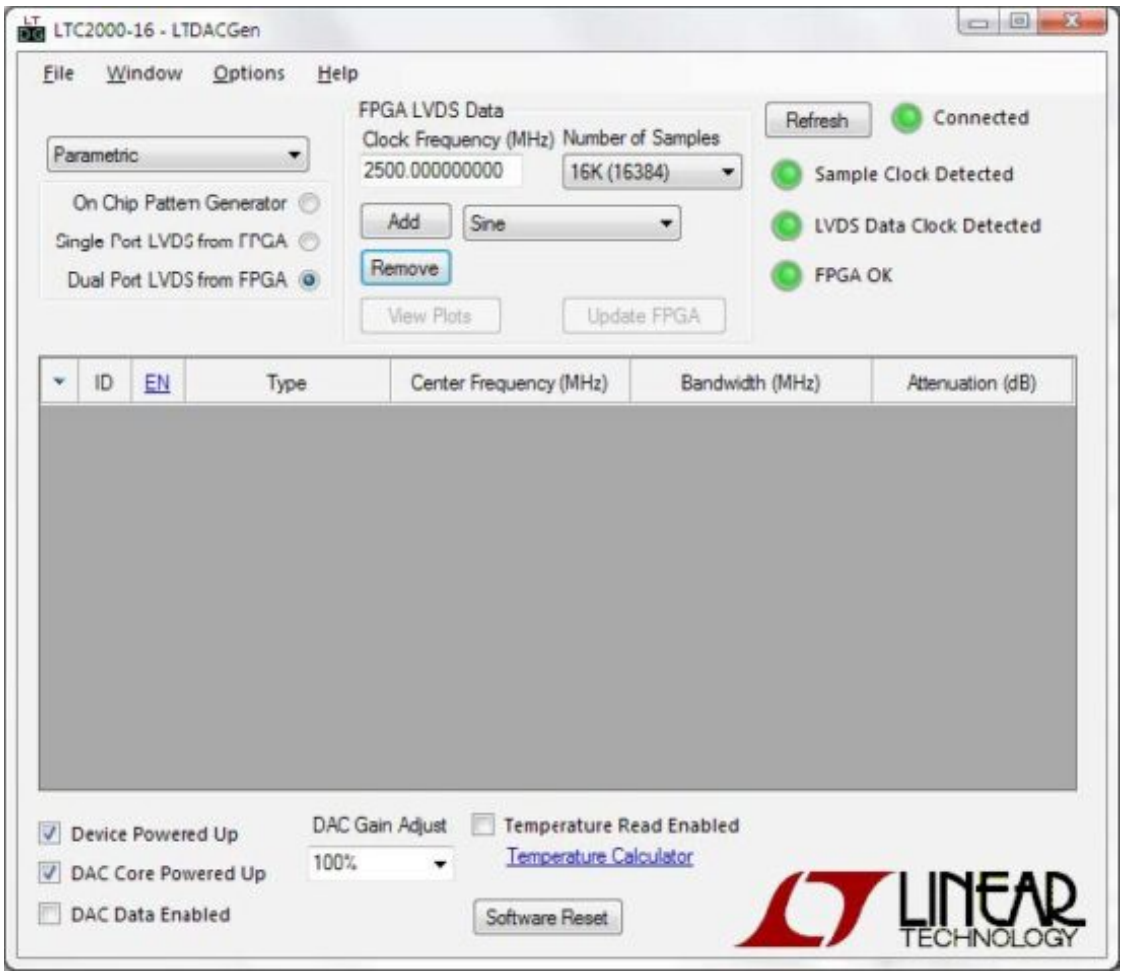


Figure 2. LTDACGen Connected to FPGA

ANALOG OUTPUT NETWORK

The analog output network of the DC2085 has been designed to maximize the performance of the LTC2000. The LTC2000 drives two 50Ω resistors on each side to minimize the impedance it sees. This maximizes the SFDR the DAC is able to produce. If a larger signal swing is required this impedance can be increased, but the SFDR might degrade. The output also has a pi network of 50Ω resistors to pad the output impedance of the board up to 50Ω per side. This allows the demo board to drive a 50Ω analyzer through a balun or other combiner.

Linear Technology has various coupon boards for specific frequencies and applications. More information is available at www.linear.com.

SAMPLE CLOCK

The sample clock to the DC2085 demonstration circuit board is marked J4. As a default it is a single-ended 50Ω input port. There is an onboard balun that does a singleended to differential translation.

For the best noise performance, the sample input must be driven with a very low jitter signal generator source. The amplitude should be as large as possible up to ±1.8V or 9dBm.

SOFTWARE

The software for the DC2085, LTDACGen is available at www.linear.com free of charge. It simplifies the creation of complex waveforms and loading them into the FPGA to test the DC2085. For more information about how to use the LTDACGen software, refer to the help files that come with the software.

RESULTS

After everything is set up and the software is connected to the DAC demo system, a sine wave can be added to the output waveform. The default frequency is 399.932861328MHz (Figure 3). By clicking Update FPGA, the data is sent to the FPGA and is then used to program the DAC. A spectrum analyzer can then be used to view the results (Figure 4).

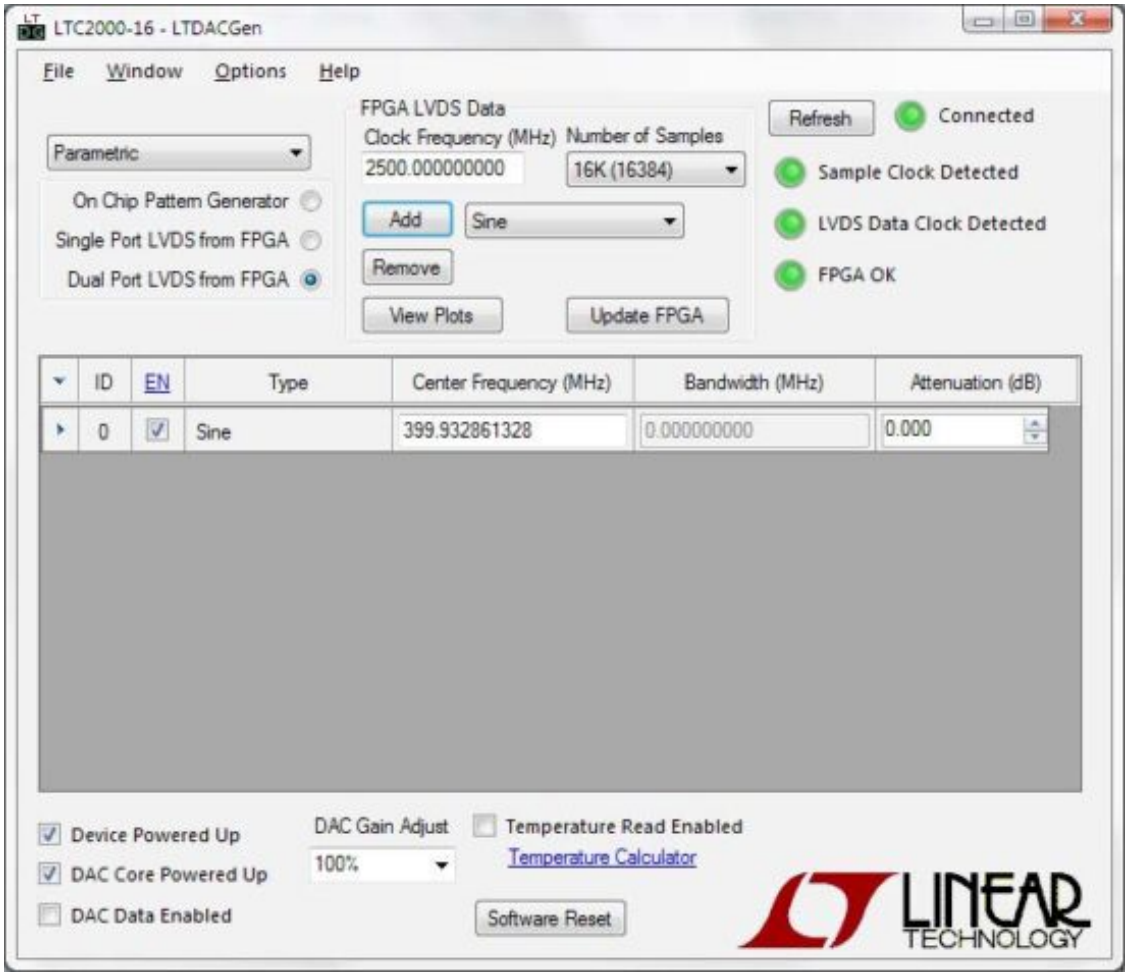
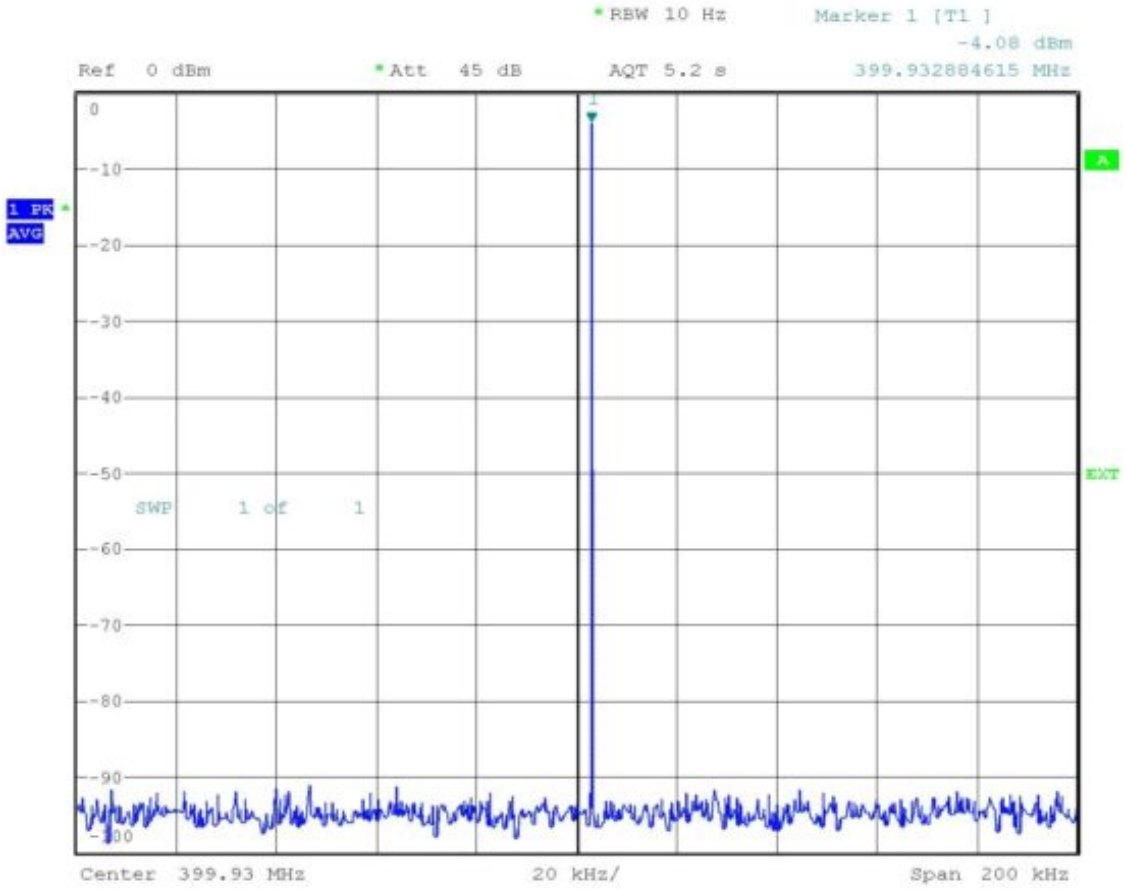


Figure 3. Default Frequency



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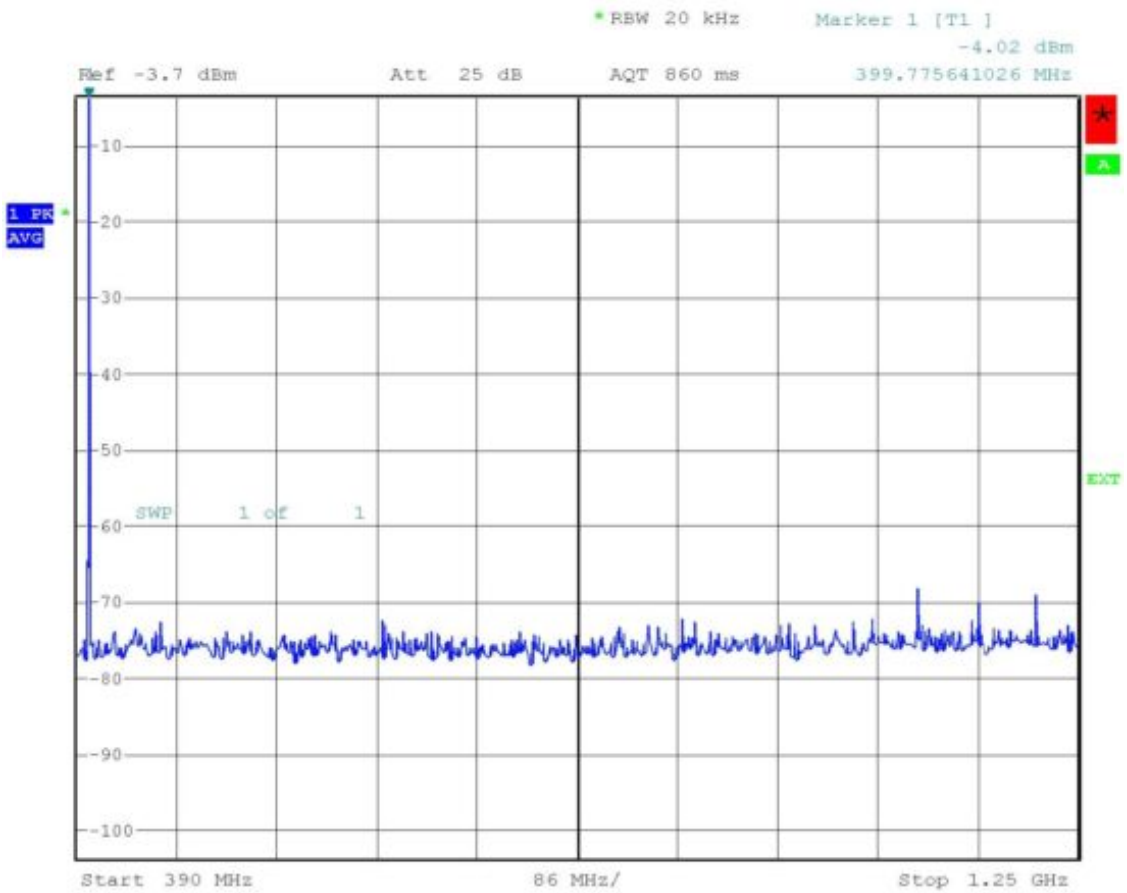

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Figure 4. DC2085 Results. Close-In (Top) and Wideband (Bottom)

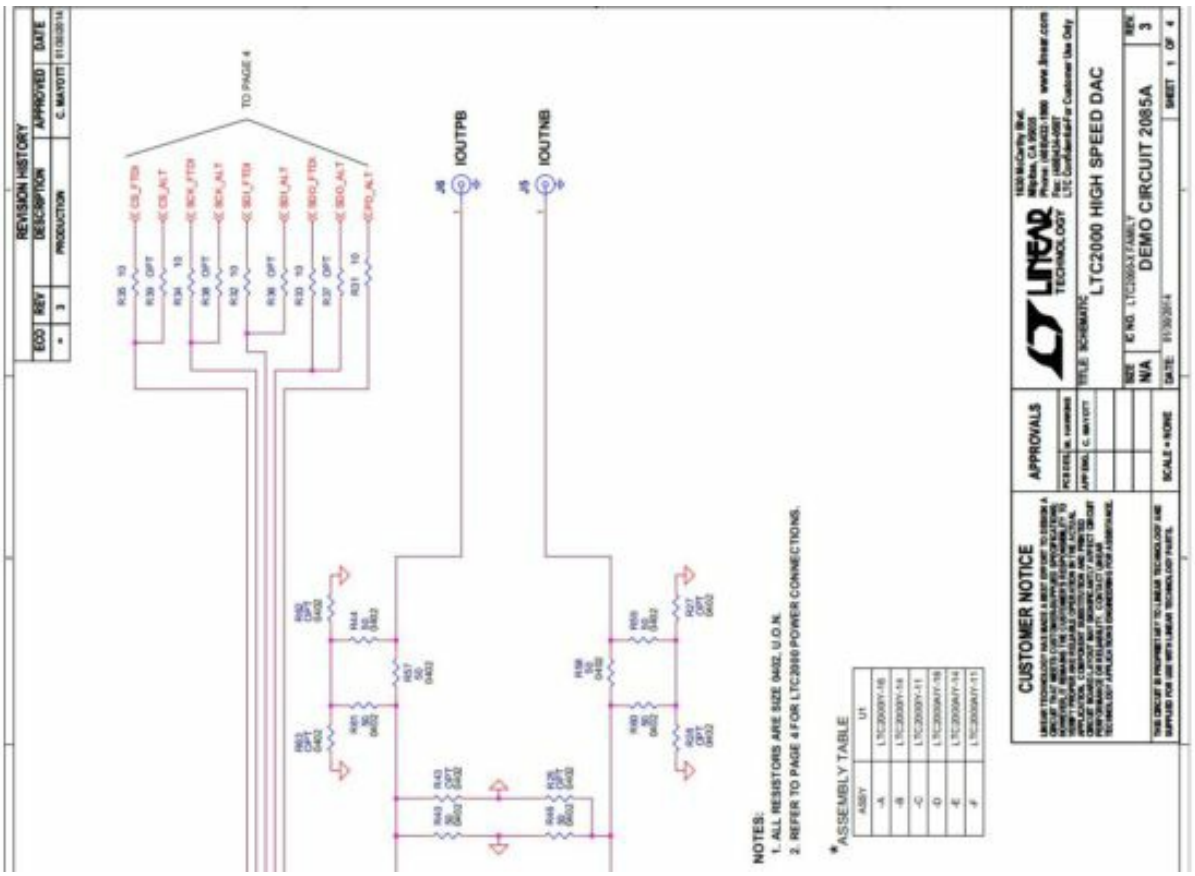
PARTS LIST

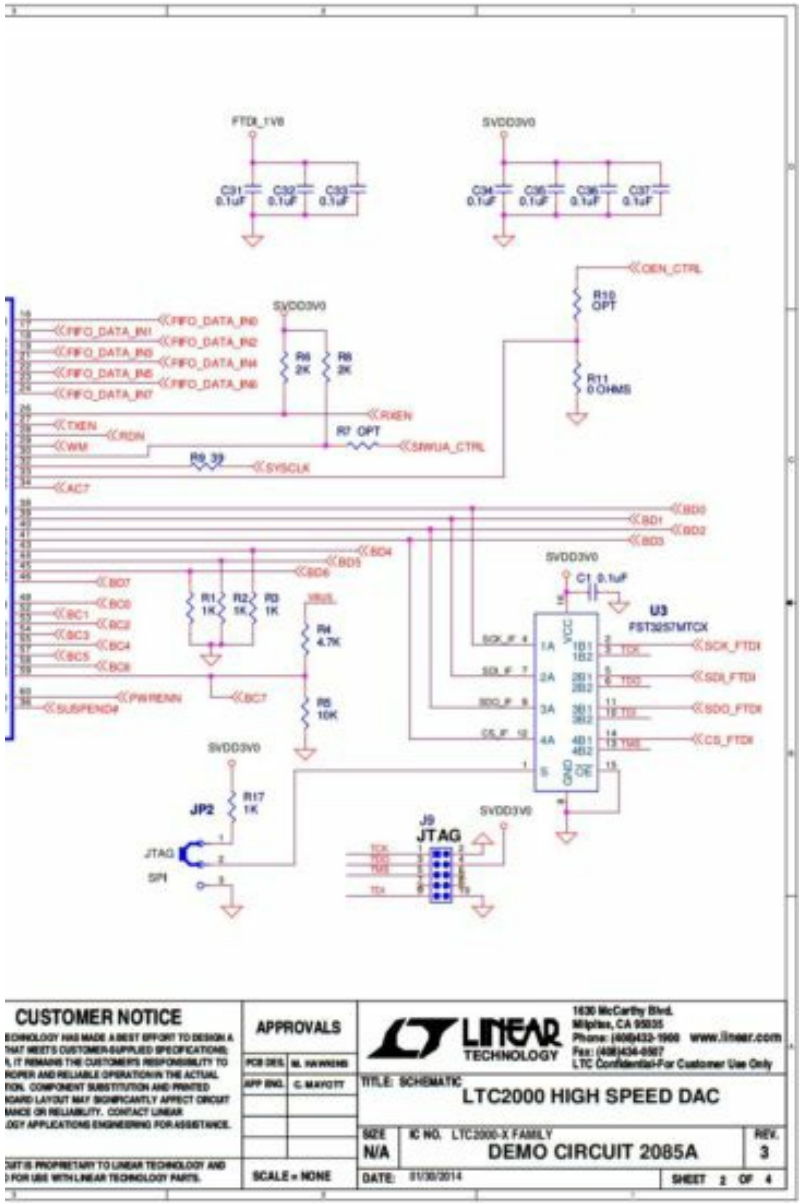
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	13	C1, C25, C26, C29, C31, C32, C33, C34, C35, C36, C37, C71, C72	CAP., X7R, 0.1µF, 16V 10% 0402	AVX, 0402YC104KAT2A
2	4	C2, C3, C8, C19	CAP., NPO, 0.01µF, 25V 5% 0603	TDK, C1608C0G1H103J
3	9	C4, C6, C9, C11, C14, C18, C67, C68, C69	CAP., X7R, 1µF, 16V 10% 0603	AVX, 0603YC105KAT2A
4	5	C5, C7, C10, C12, C15	CAP., TANT., 47µF, 16V 10% 7343	AVX, TAJD476K016RNJ
5	4	C13, C16, C27, C28	CAP., X5R, 4.7µF, 16V 20% 1206	TDK, C3216X5R1C475M
6	2	C17, C40	CAP., X5R, 10µF, 10V 20% 0603	AVX, 0603ZD106MA2T
7	1	C20	CAP., C0G, 4.7pF, 50V ± 0.25pF 0603	AVX, 06035A4R7CAT2A
8	2	C21, C24	CAP., X7R, 0.1µF, 16V 10% 0603	TDK, C1608X7R1C104K
9	1	C22	CAP., X7R, 1µF, 25V 10% 0603	TDK, C1608X7R1E105K
10	2	C23, C70	CAP., X7R, 47µF, 10V 10% 1210	MURATA, GRM32ER71A476KE15L
11	1	C30	CAP., X5R, 3.3µF, 16V 10% 0603	TDK, C1608X5R1C335K
12	2	C38, C39	CAP., C0G, 27pF, 50V 5% 0402	TDK, C1005C0G1H270J
13	2	C41, C42	CAP., C0G, 100pF, 25V 5% 0201	TDK, C0603C0G1E101J
14	1	C43	CAP., X5R, 0.01µF, 16V 10% 0402	MURATA, GRM155R61C103KA01D
15	1	C44	CAP., X7R, 47nF, 25V 10% 0402	MURATA, GRM155R71E473KA88D
16	9	C45, C48, C49, C53, C54, C58, C61, C62, C64	CAP., X5R, 100µF, 6.3V 20% 1206	TDK, C3216X5R0J107M
17	10	C46, C50, C51, C52, C55, C56, C57, C59, C60, C63	CAP., X7S, 2.2µF, 4V 20% 0306	MURATA, LLL185C70G225ME01L
18	1	C47	CAP., C0G, 10pF, 25V 5% 0201	MURATA, GRM0335C1E100JA01D
19	0	C65	CAP., OPT, 0402	OPTION
20	1	C66	CAP., NP0, 1pF, 25V ±.25pF 0402	AVX, 04023A1R0CAT2A
21	2	C73, C74	CAP., X7R, 4.7µF, 50V 10% 1206	MURATA, GRM31CR71H475KA12L
22	1	C75	CAP., X7R, 10µF, 50V 10% 1210	MURATA, GRM32ER71H106KA12L
23	2	C76, C77	CAP., X5R, 1µF, 50V 10% 0603	MURATA, GRM188R61H105KAALD
24	1	D1	DIODE, TVS, 70V,SMA	DIODES INC./ ZETEX, SMAT70A-13-F
25	1	D2	DIODE, TVS, 24V,SMA	DIODES INC./ ZETEX, SMAJ24A-13-F
26	1	D3	LED, RED, WATERCLEAR, 0805	WÜRTH, 150080RS75000
27	10	E1, E2, E3, E5–E11	TEST POINT, TURRET, .061, PBF	MILL-MAX, 2308-2-00-80-00-00-07-0
28	2	E4, E12	TEST POINT, TURRET, .094, PBF	MILL-MAX, 2501-2-00-80-00-00-07-0
29	2	JP1, JP2	HEADER, 3 PIN, .079	SULLINS, NRPN031PAEN-RC
30	1	J1	HEADER, 2×7 DUAL ROW	MOLEX 87831-1420
31	3	J2, J3, J8	CON., SMA JACK, STRAIGHT, THRU-HOLE	AMPHENOL CONNEX, 132134
32	1	J4	CON., SMA PCB TOP MOUNT	AEP, 9650-1113-005
33	2	J5, J6	CON., SMA 50Ω EDGE-LAUNCH	EMERSON, 142-0701-851
34	1	J7	CONNECTOR, USB TYPE B, RIGHT ANGLE PCB MOUNT	FCI, 61729-0010BLF
35	1	J9	HEADER, 2X5, 0.100	SAMTEC, TSW-105-07-L-D
36	2	J10, J11	CONNECTOR, HSMC	SAMTEC, ASP-122952-01

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
37	6	L1, L2, L3, L4, L6, L7	FERRITE BEAD, 33Ω AT 100mHz, 1206	MURATA, BLM31PG330SN1L
38	1	L5	INDUCTOR, 2.2µH, 20% HIGH CURRENT, SMT	VISHAY, IHLP2020BZER2R2M11
39	1	L8	INDUCTOR, CERAMIC CHIP, 1nH, 5%, 0402	COILCRAFT, 0402CS-1N0XJLU
40	1	L9	FERRITE BEAD, 30Ω AT 100mHz, 0805	TDK, MPZ2012S300A
41	1	L10	INDUCTOR, 6.8µH, 20% HIGH CURRENT, SMT	VISHAY, IHLP2020BZER6R8M11
42	2	MTG5, MTG6	STANDOFF, NYLON 0.5"	KEYSTONE, 8833 (SNAP ON)
43	2	Q1, Q2	TRANSISTOR, N-CH. POWER MOSFET, SOIC 8L	FAIRCHILD, FDS8870
44	6	R1, R2, R3, R13, R17, R30	RES., CHIP, 1k, 1/16W, 5% 0402	VISHAY, CRCW04021K00JNED
45	1	R4	RES., CHIP, 4.7k, 1/16W, 5% 0402	YAGEO, RC0402JR-074K7L
46	4	R5, R14–R16	RES., CHIP, 10k, 1/16W, 5% 0402	YAGEO, RC0402JR-0710KL
47	2	R6, R8	RES., CHIP, 2k, 1/16W, 5% 0402	VISHAY, CRCW04022K00JNED
48	0	R7, R10, R23, R24, R25, R27, R28, R36, R37, R38, R39, R43, R62, R63	RES., CHIP, OPT, 0402	OPTION
49	1	R9	RES., CHIP, 39Ω, 1/16W, 1% 0402	VISHAY, CRCW040239R0FKED
50	1	R11	RES., CHIP, 0Ω JUMPER, 1/16W, 0402	VISHAY, CRCW04020000Z0ED
51	1	R12	RES., CHIP, 12k, 1/16W, 5% 0402	VISHAY, CRCW040212K0JNED
52	1	R18	RES., CHIP, 2.2k, 1/16W, 5% 0402	VISHAY, CRCW04022K20JNED
53	2	R19, R20	RES., CHIP, 3.24k, 1/16W, 1% 0402	VISHAY, CRCW04023K24FKED
54	1	R21	RES., CHIP, 1k, 1/16W, 1% 0402	YAGEO, RC0402FR-071KL
55	1	R22	RES., CHIP, 7.15k, 1/16W, 1% 0402	VISHAY, CRCW04027K15FKED
56	2	R26, R29	RES., CHIP, 49.9Ω, 1/6W, 1% 0201	VISHAY, CRCW020149R9FNED
57	7	R31-R35, R41, R42	RES., CHIP, 10Ω, 1/16W, 1% 0402	VISHAY, CRCW040210R0FKED
58	10	R40, R44, R46, R47, R48, R57, R58, R59, R60, R61	RES., CHIP, 50Ω, HIGH FREQ., 1/20W, 0.1% 0402	VISHAY, FC0402E50R0BST1
59	1	R45	RES., CHIP, 499Ω, 1/16W, 1% 0402	VISHAY, CRCW0402499RFKED
60	1	R49	RES., CHIP, 41.2k, 1/10W, 1% 0603	VISHAY, CRCW060341K2FKEA
61	1	R50	RES., CHIP, 309k, 1/10W, 1% 0603	VISHAY, CRCW0603309KFKEA
62	1	R51	RES., CHIP, 243k, 1/10W, 1% 0603	VISHAY, CRCW0603243KFKEA
63	1	R52	RES., CHIP, 50Ω, 1/8W, 5% 0603	VISHAY, FC0603E50R0JST1
64	1	R53	RES., CHIP, 560Ω, 1/10W, 5% 0603	VISHAY, CRCW0603560RJNEA
65	1	R54	RES., CHIP, 10k, 1/10W, 1% 0603	VISHAY, CRCW060310K0FKEA
66	2	R55, R56	RES., CHIP, 20Ω, 1/16W, 1% 0402	VISHAY, CRCW040220R0FKED
67	1	T1	TRANSFORMER, BALUN	ANAREN, B0430J50100AHF
68	1	U2	IC, USB TO MULTIPURPOSE UART/FIFO, TQFP	FTDI, FT2232HL
69	1	U3	IC, QUAD MUX/DEMUX, TSSOP-16	FAIRCHILD, FST3257MTCX
70	1	U4	IC, EEPROM 1kBIT 3MHZ, 8TSSOP	MICROCHIP, 93LC46C-I/ST
71	1	U5	IC, MICROPOWER REGULATOR, SO-8	LINEAR TECHNOLOGY, LT1763CS8-3#PBF
72	2	U6, U7	IC, MICROPOWER REGULATOR, SO-8	LINEAR TECHNOLOGY, LT1763CS8-3.3#PBF
73	1	U8	IC, BUCK REGULATOR, QFN	LINEAR TECHNOLOGY, LT8614IUDC#PBF
74	1	U9	IC, VOLTAGE REFERENCE, MSOP	LINEAR TECHNOLOGY, LTC6655CHMS8-2.048#PBF

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
75	2	U10, U11	I.C., LOW DROPOUT REGULATOR, 3×3mm, DFN	LINEAR TECHNOLOGY, LT3080EDD#PBF
76	1	U12	I.C., 80V IDEAL DIODE, DFN-6L	LINEAR TECHNOLOGY, LTC4359HDCB-#TRPBF
77	2	XJP1, XJP2	SHUNT, 2mm	SAMTEC, 2SN-BK-G
78	1	Y1	CRYSTAL, 12.0 MHz, SMT	ABRACON, ABMM2-12.000MHZ-E2-T
DC2085A-A Required Circuit Components				
1	1		GENERAL BOM	DC2085A
2	1	U1	IC, 16-BIT 2.5Gsps DAC	LINEAR TECHNOLOGY, LTC2000IY-16
DC2085A-B Required Circuit Components				
1	1		GENERAL BOM	DC2085A
2	1	U1	IC, 14-BIT 2.5Gsps DAC	LINEAR TECHNOLOGY, LTC2000IY-14
DC2085A-C Required Circuit Components				
1	1		GENERAL BOM	DC2085A
2	1	U1	IC, 11-BIT 2.5Gsps DAC	LINEAR TECHNOLOGY, LTC2000IY-11
DC2085A-D Required Circuit Components				
1	1		GENERAL BOM	DC2085A
2	1	U1	IC, 16-BIT 2.7Gsps DAC	LINEAR TECHNOLOGY, LTC2000AIY-16
DC2085A-E Required Circuit Components				
1	1		GENERAL BOM	DC2085A
2	1	U1	IC, 14-BIT 2.7Gsps DAC	LINEAR TECHNOLOGY, LTC2000AIY-14
DC2085A-F Required Circuit Components				
1	1		GENERAL BOM	DC2085A
2	1	U1	IC, 11-BIT 2.7Gsps DAC	LINEAR TECHNOLOGY, LTC2000AIY-11

SCHEMATIC DIAGRAM





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RT IS PROPRIETARY TO LINEAR TECHNOLOGY AND) FOR USE WITH LINEAR TECHNOLOGY PARTS.

APPROVALS	
PCB DES.	M. HAWKINS
APP ENG.	C. MAYOTT

SCALE = NONE

LINEAR TECHNOLOGY

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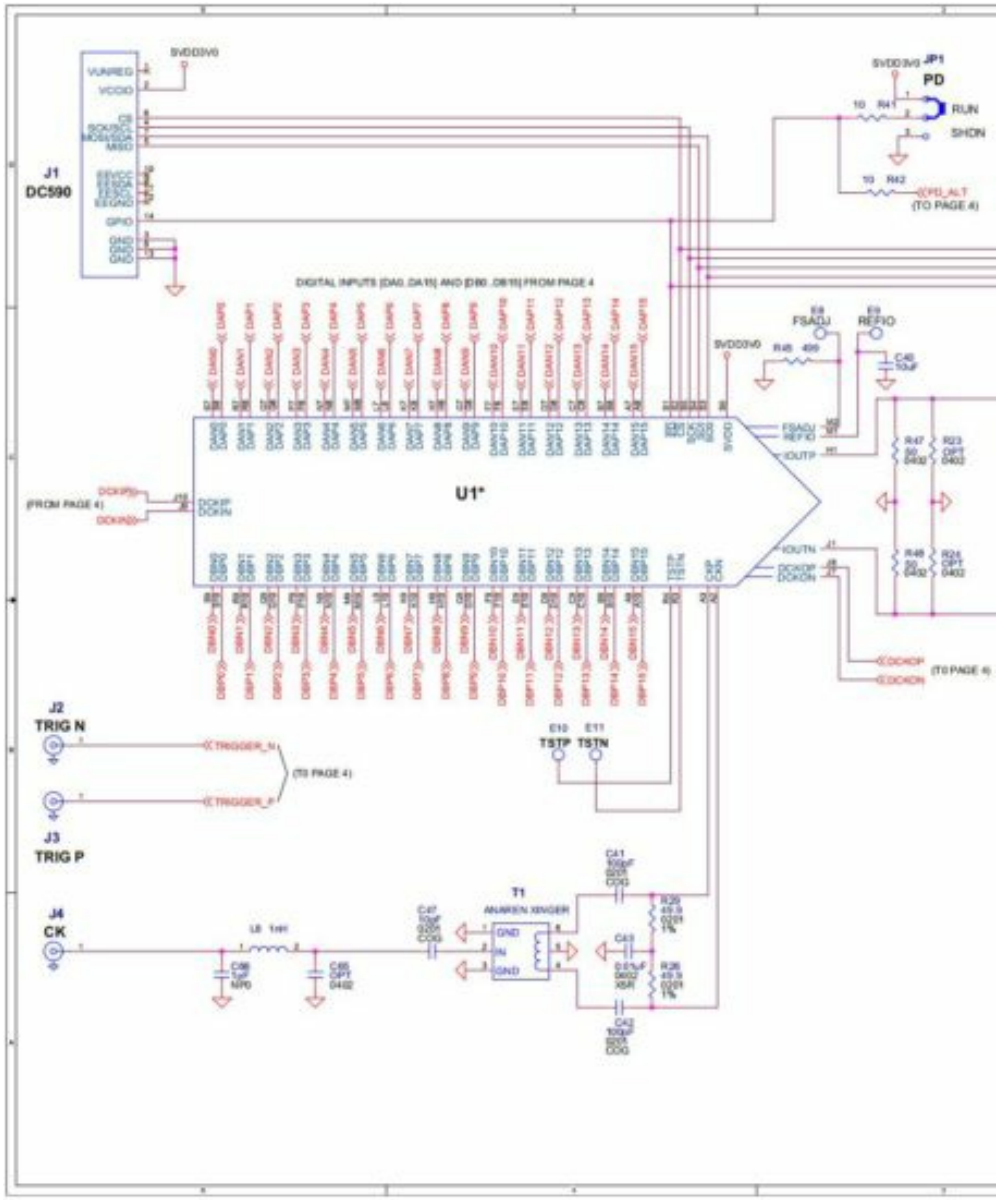
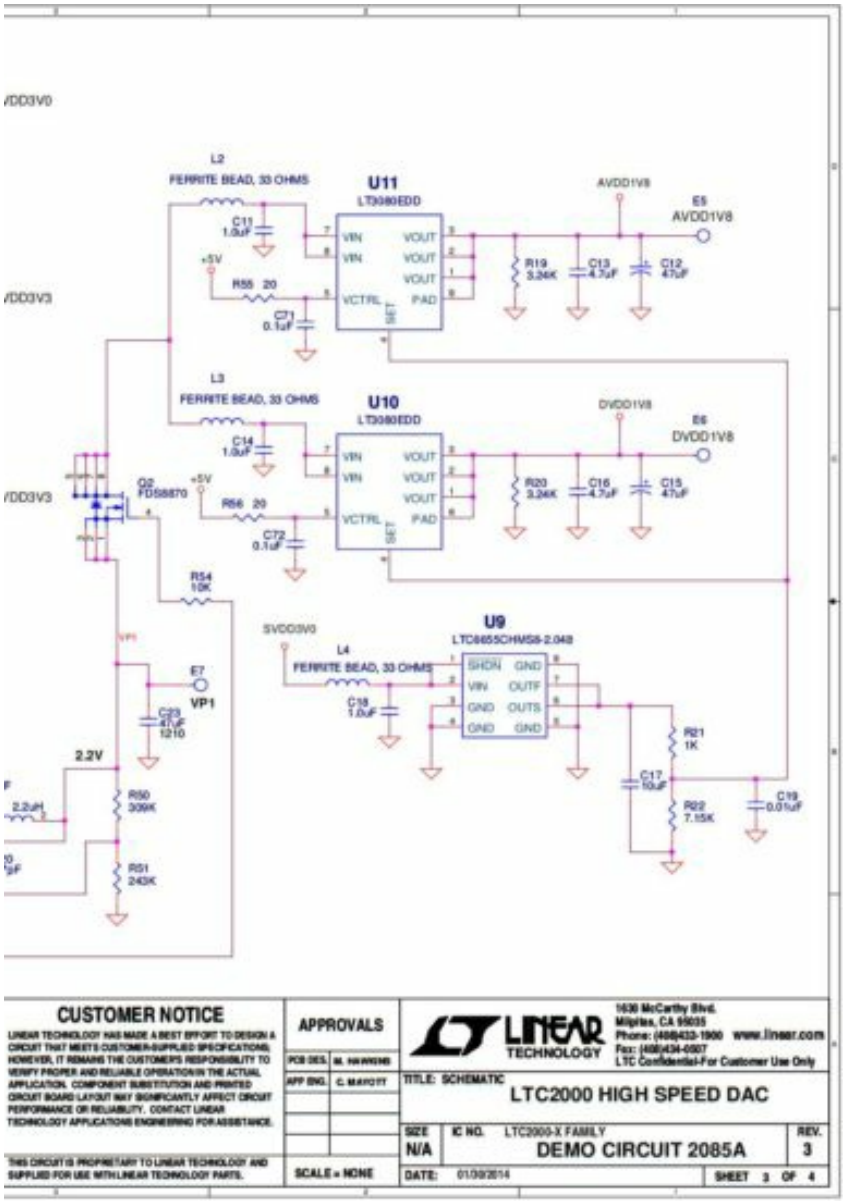
TITLE: SCHEMATIC
LTC2000 HIGH SPEED DAC

SIZE N/A | IC NO. LTC2000-X FAMILY
DEMO CIRCUIT 2085A
REV. 3

DATE: 01/30/2014 | SHEET 2 OF 4

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FERRITE BEAD, 33 OHMS
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AVDD1V8
E5
AVDD1V8
C11
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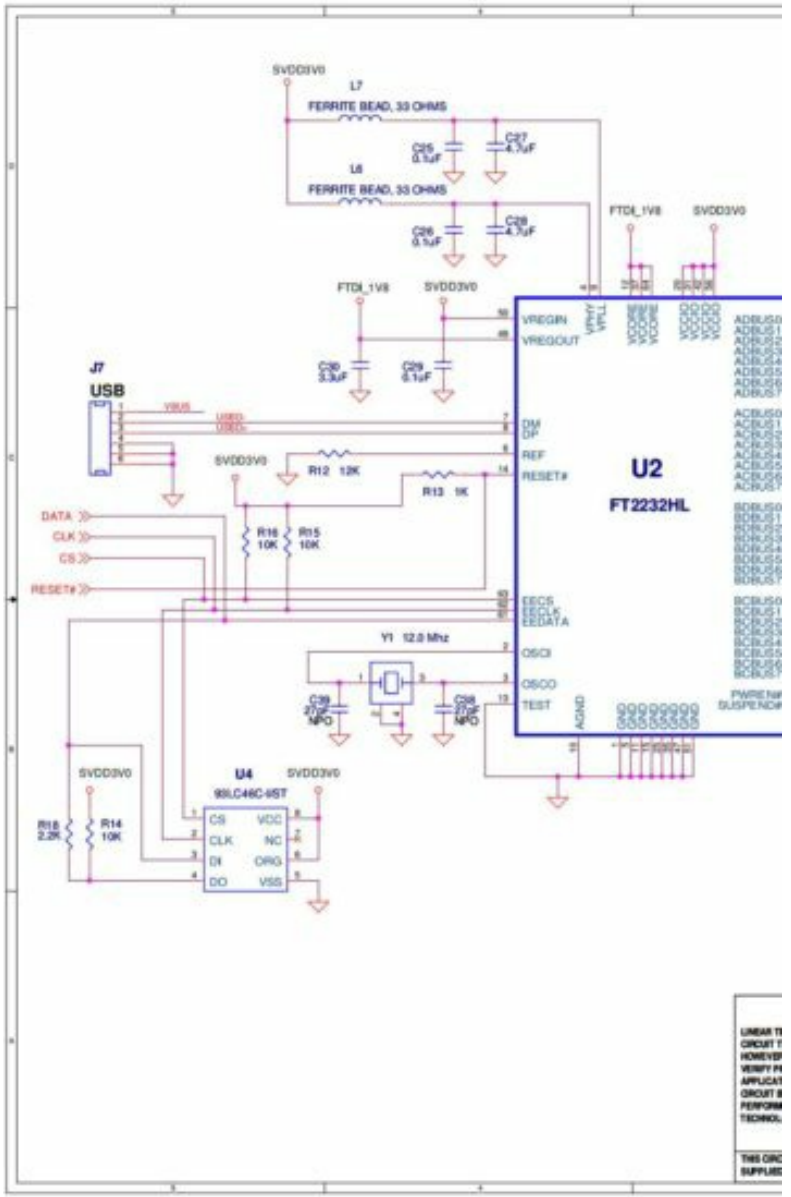
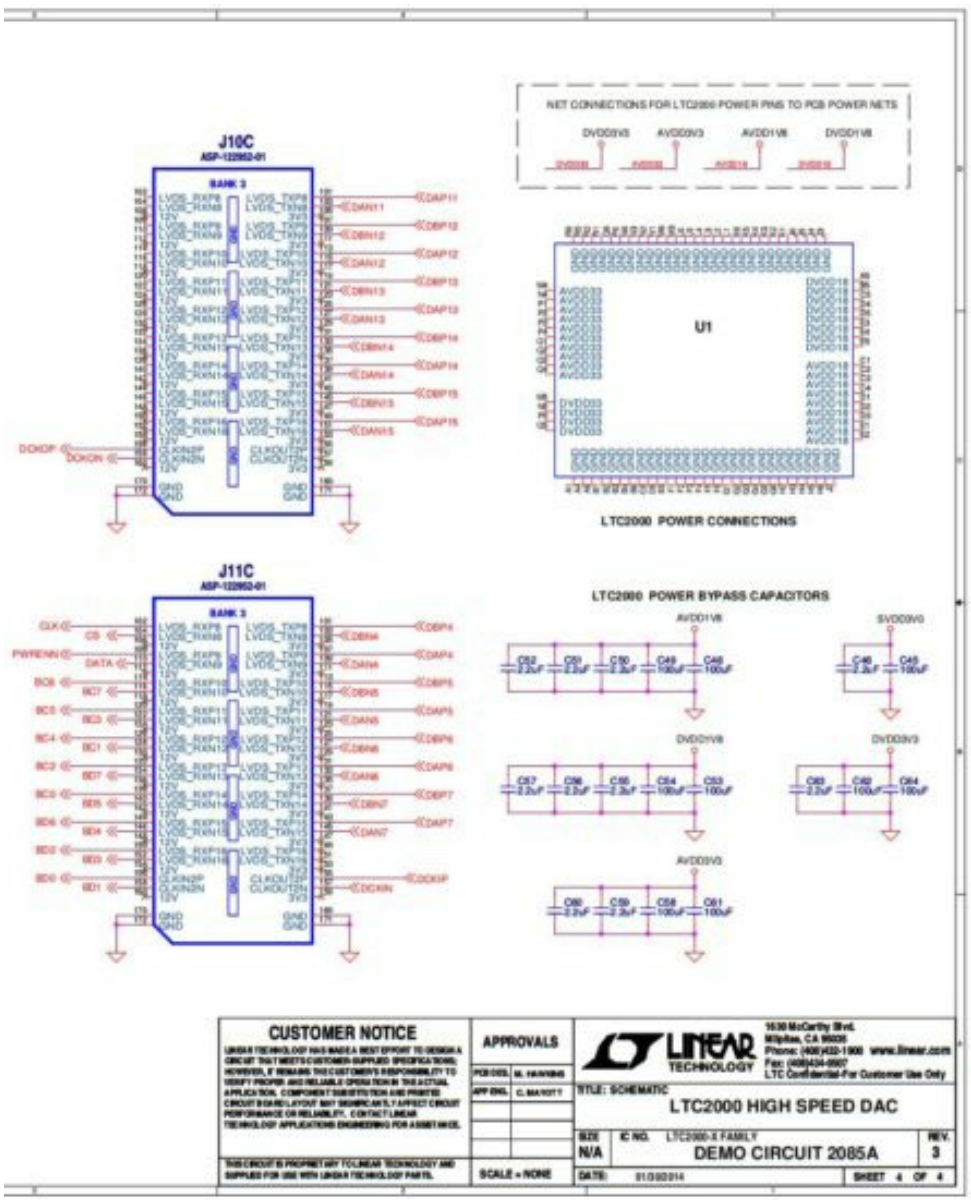
+5V
R55 20
C71
0.1uF
R19
3.24K
C13
4.7uF
C12
47uF
L3
FERRITE BEAD, 33 OHMS
U10
LT3080EDD
DVDD1V8
E6
DVDD1V8
C14
1.0uF
Q2
FDS8870
+5V
R56 20
C72
0.1uF
R20
3.24K
C16
4.7uF
C15
47uF
R54
10K
VP1
E7
VP1
C23
47uF
1210
2.2V
R50
309K
2.2uH
R51
243K
SVDD3V0
L4
FERRITE BEAD, 33 OHMS
U9
LTC6655CHMS8-2.048
SHDN
GND
VIN
OUTF
GND
OUTS
GND
GND
C18
1.0uF
R21
1K
C17
10uF
R22
7.15K
C19
0.01uF
CUSTOMER NOTICE
LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.
THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.
APPROVALS
PCB DES.
APP ENG.
SCALE = NONE
LINEAR TECHNOLOGY
1630 McCarthy Blvd.
Milpitas, CA 95035
Phone: (408)432-1900 www.linear.com
Fax: (408)434-0507
LTC Confidential-For Customer Use Only
TITLE: SCHEMATIC
LTC2000 HIGH SPEED DAC
SIZE
N/A
IC NO.
LTC2000-X FAMILY
DEMO CIRCUIT 2085A
REV.
3
DATE:
SHEET 3 OF 4


SVDD3V0
L7
FERRITE BEAD, 33 OHMS
C25
0.1uF
C27
4.7uF
L8
FERRITE BEAD, 33 OHMS
C26
0.1uF
C28
4.7uF
FTDI_1V8
SVDD3V0
C30
3.3uF
C29
0.1uF
J7
USB
VBUS
USBD-
USBD+
DM
DP
REF
RESET#
U2
FT2232HL
VREGIN
VREGOUT
R12 12K
R13 1K
R16
10K
R15
10K
DATA
CLK
CS
RESET#
EECS
EECLK
EEDATA
Y1 12.0 Mhz
OSCI
OSCO
TEST
AGND
C39
27pF
C38
27pF
U4
93LC46C-I/ST
CS
CLK
DI
DO
VCC
NC
ORG
VSS
R18
2.2K
R14
10K
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
ACBUS0
ACBUS1
ACBUS2
ACBUS3
ACBUS4
ACBUS5
ACBUS6
ACBUS7
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
BCBUS0
BCBUS1
BCBUS2
BCBUS3
BCBUS4
BCBUS5
BCBUS6
BCBUS7
PWREN#
SUSPEND#


J10C
ASP-122952-01
BANK 3
J11C
ASP-122952-01
BANK 3
NET CONNECTIONS FOR LTC2000 POWER PINS TO PCB POWER NETS
DVDD3V3
AVDD3V3
AVDD1V8
DVDD1V8
U1
LTC2000 POWER CONNECTIONS
LTC2000 POWER BYPASS CAPACITORS
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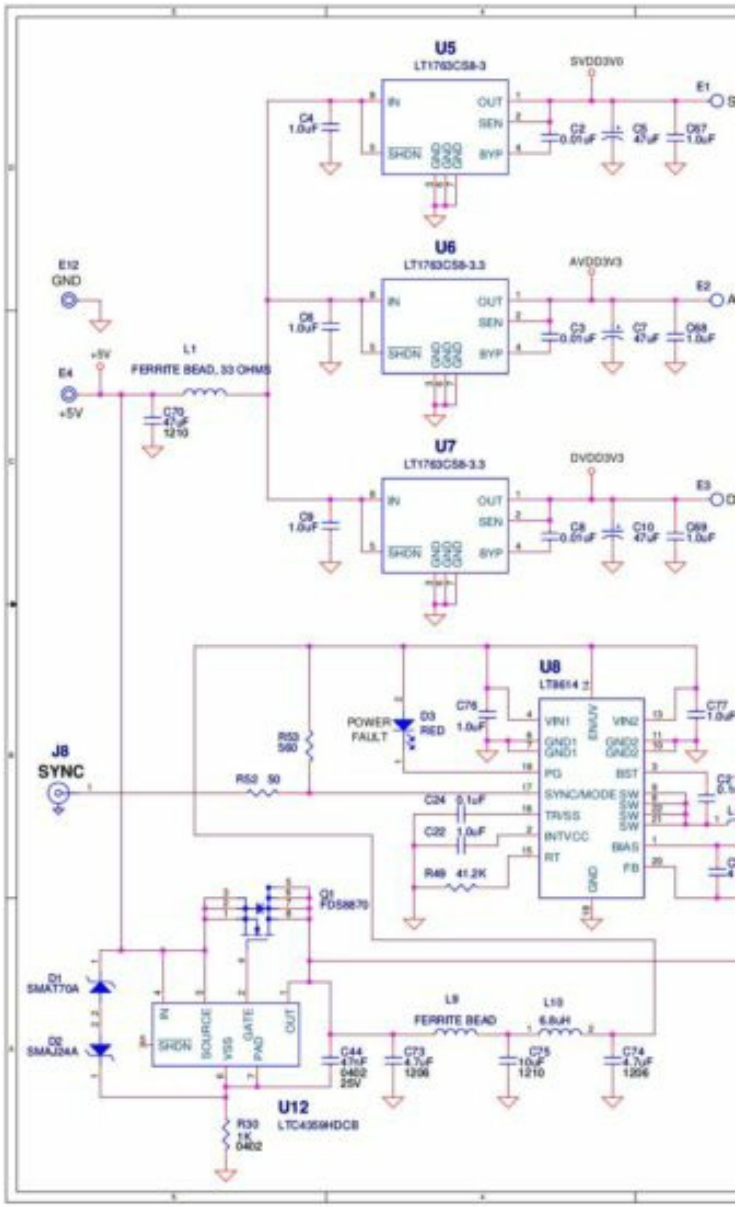
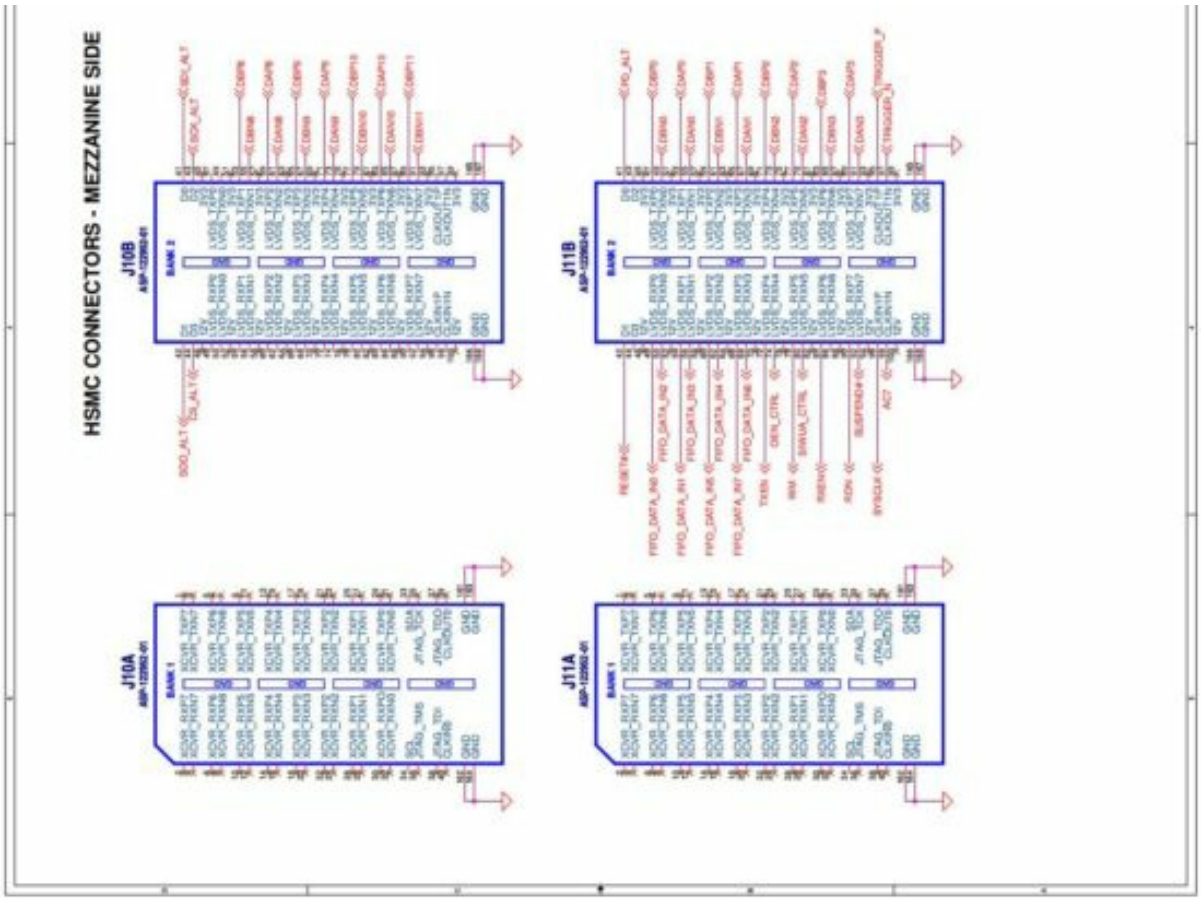
DEMO CIRCUIT 2085A
REV.
3
DATE:
SHEET 4 OF 4
SCALE = NONE


U5
LT1763CS8-3
U6
LT1763CS8-3.3
U7
LT1763CS8-3.3
U8
LT8614
U12
LTC4359HDCB
L1
FERRITE BEAD, 33 OHMS
J8
SYNC
E12
GND
E4
+5V
SVDD3V0
AVDD3V3
DVDD3V3
POWER FAULT
D3
RED
Q1
FDS8870
D1
SMAT70A
D2
SMAJ24A
L9
FERRITE BEAD
L10
6.8uH



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	**LINEAR TECHNOLOGY LTC2000-16 Demonstration Circuit** [pdf] Installation Guide LTC2000-16 Demonstration Circuit, LTC2000-16, Demonstration Circuit, Circuit

References

- Mixed-signal and digital signal processing ICs | Analog Devices
- Product Evaluation Boards and Kits | Design Center | Analog Devices
- LTC2000 Datasheet and Product Info | Analog Devices
- LTC2000A Datasheet and Product Info | Analog Devices
- User Manual