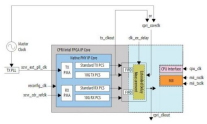

intel v19.4.2 CPRI FPGA IP User Guide

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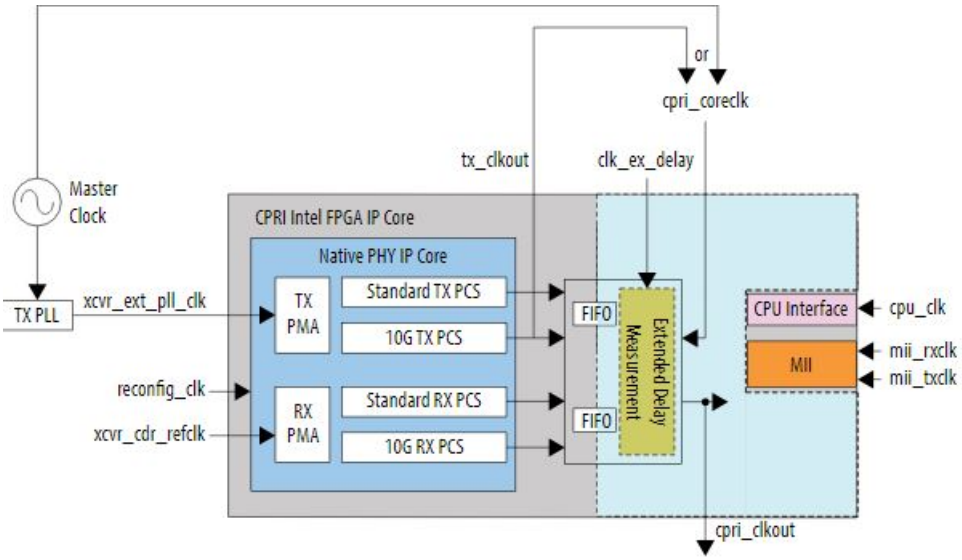

Product Information

Version	Description	Impact	Related Information
v19.6.0	Added support for GMII Ethernet PCS Bypass mode. Added parameter Ethernet PCS Bypass.	—	Intel Quartus Prime Pro Edition: Version 22.3 Software and Device Support Release Notes
v19.5.0	Added the Spyglass CDC support for the Intel Agilex F-tile devices.	—	Intel Quartus Prime Pro Edition: Version 22.2 Software and Device Support Release Notes
v19.4.3	Added support for QuestaSim* simulator. Removed support for ModelSim* SE and NCSim simulator.	—	Intel Quartus Prime Pro Edition: Version 22.1 Software and Device Support Release Notes
v19.4.2	Added 1.2288G CPRI Line Bit Rate support for Intel Agilex F-tile devices.	—	Intel Quartus Prime Pro Edition: Version 21.4 Software and Device Support Release Notes
v19.4.0	Added new parameter: Generate example design for (ED_TYPE). Added support for the Intel Agilex F-tile devices. Added new parameter: Enable resynchronization of CPRI radio frame number to desired value. Added new signal: aux_bfn_resync_value [11:0]. Added Xcelium* simulator support for Design Example.	—	N/A
v19.3.0	Improved Synopsys Design Constraint file. Added ability to constraint each instance specifically so that no constraints overlap between CPRI instances of different configurations.	—	Intel Quartus Prime Pro Edition: Version 20.4 Software and Device Support Release Notes
v19.2.0	Added support for the Intel Stratix 10 E-tile devices. Added new parameters: Transceiver tile to be used and Enable Reed-Solomon Forward Error Correction (RS-FEC).	—	Intel Quartus Prime Pro Edition: Version 19.2 Software and Device Support Release Notes
v18.1	Changed the name of the IP to CPRI Intel FPGA IP in Intel Quartus Prime IP Catalog. Renamed the IP parameter: Altera Debug Master Endpoint (ADME) to Native PHY Debug Master Endpoint (NPDME).	—	N/A

Product Usage Instructions

1. Ensure you have the required version of Intel Quartus Prime Pro Edition installed.
2. Refer to the specific version of the CPRI Intel FPGA IP listed in the table above for detailed information on its features and improvements.

3. Follow the instructions provided in the related information documents for each version to properly configure and use the CPRI Intel FPGA IP.
4. If using a simulator, make sure to use the supported simulator mentioned in the respective version's description.
5. For any further assistance or feedback, refer to the "Send Feedback" section in the user manual or contact the product support team.

CPRI Intel® FPGA IP Core Release Notes

The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus® Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Introduction to Intel FPGA IP Cores
- CPRI Intel FPGA IP User Guide

CPRI Intel FPGA IP v19.6.0

Table 1. v19.6.0 2022.11.15

Intel Quartus Prime Pro Edition Version	Description	Impact
22.3	Added support for GMII Ethernet PCS Bypass mode.	—
	Added parameter **Ethernet PCS Bypass**.	—
	Added the following signals (available when the **Ethernet PCS Bypass** parameter is turned on): • gmii_rx_fifo_rvalid • gmii_rx_fifo_rdata • gmii_tx_fifo_wready • gmii_tx_fifo_wdata	—

Related Information

Intel Quartus Prime Pro Edition: Version 22.3 Software and Device Support Release Notes

CPRI Intel FPGA IP v19.5.0

Table 2. v19.5.0 2022.10.07

Intel Quartus Prime Pro Edition Version	Description	Impact
22.2	Added the dynamic rate switch support for the Intel Agilex ™ F-tile devices in both CPRI Intel FPGA IP and Design Example.	—
	Added the following signals:	—
	• ehip_tx_pll_refclk_hs_link	
	• ehip_tx_pll_refclk_ls_link	
	• ehip_rx_cdr_refclk_hs_link	
	• ehip_rx_cdr_refclk_ls_link	
	Added the Spyglass CDC support for the Intel Agilex F-tile devices.	—

Related Information
Intel Quartus Prime Pro Edition: Version 22.2 Software and Device Support Release Notes

CPRI Intel FPGA IP v19.4.3

Table 3. v19.4.3 2022.07.01

Intel Quartus Prime Pro Edition Version	Description	Impact
22.1	Added support for QuestaSim* simulator.	—
	Removed support for ModelSim* SE and NCSim simulator.	—

Related Information
Intel Quartus Prime Pro Edition: Version 22.1 Software and Device Support Release Notes

CPRI Intel FPGA IP v19.4.2

Table 4. v19.4.2 2022.04.04

Intel Quartus Prime Pro Edition Version	Description	Impact
21.4	Added 1.2288G CPRI Line Bit Rate support for Intel Agilex F-tile devices.	—

Related Information
Intel Quartus Prime Pro Edition: Version 21.4 Software and Device Support Release Notes

CPRI Intel FPGA IP v19.4.0

Table 5. v19.4.0 2021.11.11

Intel Quartus Prime Pro Edition Version	Description	Impact
21.2	Added new parameter: **Generate example design** for (ED_TYPE)	—
21.1	Added support for the Intel Agilex F-tile devices.	—
	Added new parameter: **Enable resynchronization of CPRI radio frame number to desired value**.	—
	Added new signal: aux_bfn_resync_value [11:0].	—
	Added Xcelium* simulator support for Design Example.	—

Related Information

- Intel Quartus Prime Pro Edition: Version 21.1 Software and Device Support Release Notes
- Intel Quartus Prime Pro Edition: Version 21.2 Software and Device Support Release Notes

CPRI Intel FPGA IP v19.3.0

Table 6. v19.3.0 2021.03.05

Intel Quartus Prime Pro Edition Version	Description	Impact
20.4	Added support for the Intel Agilex E-tile devices.	—
	Added 12165.12 Mbps line bit rate support for Intel Arria® 10 devices.	—
	Improved Synopsys Design Constraint file. Added ability to constraint each instance specifically so that no constraints overlap between CPRI instances of different configurations.	—
	Added 3072.0 Mbps, 6144.0 Mbps and 12165.12 Mbps line bit rates support for Intel Stratix® 10 E-tile devices.	—

Related Information
Intel Quartus Prime Pro Edition: Version 20.4 Software and Device Support Release Notes

CPRI Intel FPGA IP v19.2.0
Table 7. v19.2.0 2019.10.01

Intel Quartus Prime Pro Edition Version	Description	Impact
19.2	Added support for the Intel Stratix 10 E-tile devices.	—
	Added new parameters: **Transceiver tile to be used** and **Enable Reed-Solomon Forward Error Correction (RS-FEC)**.	—

Related Information
Intel Quartus Prime Pro Edition: Version 19.2 Software and Device Support Release Notes
CPRI Intel FPGA IP v18.1
Table 8. v18.1 2019.05.17

Intel Quartus Prime Version	Description	Impact
18.1	Changed the name of the IP to CPRI Intel FPGA IP in Intel Quartus Prime IP Catalog.	—
	Renamed the IP parameter: **Altera Debug Master Endpoint (ADME)** to **Native PHY Debug Master Endpoint (NPDME)**.	—
	Added new register: IP_INFO.	—
	Added new register bit in TX_SCR Register: tx_scr_active.	—
	Added register DEBUG_STATUS at offset 0xA0	
	Added 12165.12 Mbps and 24330.24 Mbps line bit rate support for Intel Stratix 10 devices.	
	Added the Hybrid core clocking mode.	
	Added support for 64-bit interface.	

Related Information

- Intel Quartus Prime Pro Edition: Version 18.1 Software and Device Support Release Notes
- Intel Quartus Prime Standard Edition: Version 18.1 Software and Device Support Release Notes

CPRI v7.0 IP Core v17.1

Table 9. Version 17.1 January 2019

Description	Impact
First release of the CPRI v7.0 IP core.	—
Verified in the Intel Quartus Prime v17.1 software.	—
The Intel Stratix 10 devices with H- and L- tile transceivers are now available in Intel Quartus Prime Pro Edition v17.1 for all CPRI line bit rates except 0.6144 Gbps.	—
Added new parameter: **Data path width**.	
Enable line bit rate auto-negotiation is now available for Intel Stratix 10 devices.	—
Added new hybrid clock source input.	—
Added Arria V GZ device support for the CPRI line bit rate of 8.11008 Gbps.	—
Change the name of the IP in Intel Quartus Prime IP catalog to **CPRI**.	—

CPRI v6.0 IP Core v17.0
Table 10. Version 17.0 January 2018

Description	Impact
Verified in the Intel Quartus Prime v17.0 software.	—
The Intel Stratix 10 device support with H- and L-tile transceivers are now available in Intel Quartus Prime Pro Edition v17.0 for CPRI line bit rates of 1.2288 Gbps and 10.1376 Gbps.	—
Removed Intel Arria 10 device family support for CPRI line bit rate of 0.6144 Gbps.	—
Added new parameters **VCCR_GXB and VCCT_GXB supply voltage for the transceiver** in Intel Stratix 10 IP core device variations.	—
Added the following new registers and signals in Intel Stratix 10 IP core device variations: • Added two new registers: XCVR_TX_FIFO_DELAY, and XCVR_RX_FIFO_DELAY. • Added two new signals: latency_sclk, latency_sreset_n	—

CPRI v6.0 IP Core v14.1
Table 11. Version 14.1 December 2014

Description	Impact	Notes
Verified in the Quartus II software v14.1.	—	—

CPRI v6.0 IP Core v14.0
Table 12. Version 14.0 June 2014

Description	Impact	Notes
First release of the CPRI v6.0 IP core.	—	—
Upgraded to support the new IP Catalog. For more information about the IP Cat alog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	—	—
Renamed **Include Vendor Specific Space (VSS) access through CPU interf ace** parameter to **Include all control word access through CPU interface** to better explain the function of the parameter. The parameter functionality remains as it was in the 13.1 and 13.0 releases.	—	—
Renamed **Receiver buffer depth** parameter to **Receiver FIFO depth**. The par ameter functionality remains as it was in the 13.1 and 13.0 releases.	—	—

CPRI v5.0 IP Core v13.1
Note: The CPRI IP core v5.0 is scheduled for product obsolescence and discontinued support as described in PDN1603. Therefore, Intel does not recommend use of this IP core in new designs. For more information about the current Intel FPGA IP offering, refer to the Intel FPGA Intellectual Property website.

Version 13.1 November 2013

Description	Impact	Notes
Removed support for HardCopy IV GX device family.	—	—
Improved the demonstration testbench.	—	—
Improved resource utilization.	—	—

Related Information
Product Discontinuance Notification: PDN1603
CPRI v5.0 IP Core v13.0
Table 14. Version 13.0 May 2013

Description	Impact	Notes
Added new parameter for user control of inclusion or exclusion of software interfa ce to full control words.	—	—
Added new parameter for user control of inclusion or exclusion of round-trip delay calibration feature.	—	—
Reduced resource utilization in 28-nm devices.	—	—

Related Information
Product Discontinuance Notification: PDN1603

CPRI Intel FPGA IP User Guide Archives

For the latest and previous versions of the CPRI Intel FPGA IP user guide, refer to the CPRI Intel FPGA IP User Guide HTML version. Select your desired version and click Download. If an IP or software version is not listed, the user guide for the previous IP or software version applies. IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IPs have a new IP versioning scheme from Intel Corporation. All rights reserved. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Intel warrants the performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services. *Other names and brands may be claimed as the property of others. ISO 9001:2015 Registered CPRI Intel® FPGA IP Core Release Notes

- Online Version
- Send Feedback
- **ID:** 683403
- **Version:** 2022.11.15

Documents / Resources

	intel v19.4.2 CPRI FPGA IP [pdf] User Guide v19.4.2, v19.6.0, v19.5.0, v19.4.2 CPRI FPGA IP, CPRI FPGA IP, FPGA IP, IP

References

- 1. Introduction to Intel® FPGA IP Cores
- 1. CPRI Intel® FPGA IP Core Release Notes
- 1. About the CPRI Intel® FPGA IP Core
- 1. Intel® Quartus® Prime Pro Edition Version 21.4 Software and Device...
- 1. Intel® Quartus® Prime Pro Edition Version 22.1 Software and Device...
- 1. Intel® Quartus® Prime Pro Edition Version 22.2 Software and Device...
- 1. Intel® Quartus® Prime Pro Edition Version 22.3 Software and Device...
- 1. About the CPRI Intel® FPGA IP Core
- Intel ISO 9001:2015 Registrations