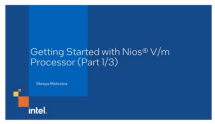

Nios V Processor Intel FPGA IP Software User Guide

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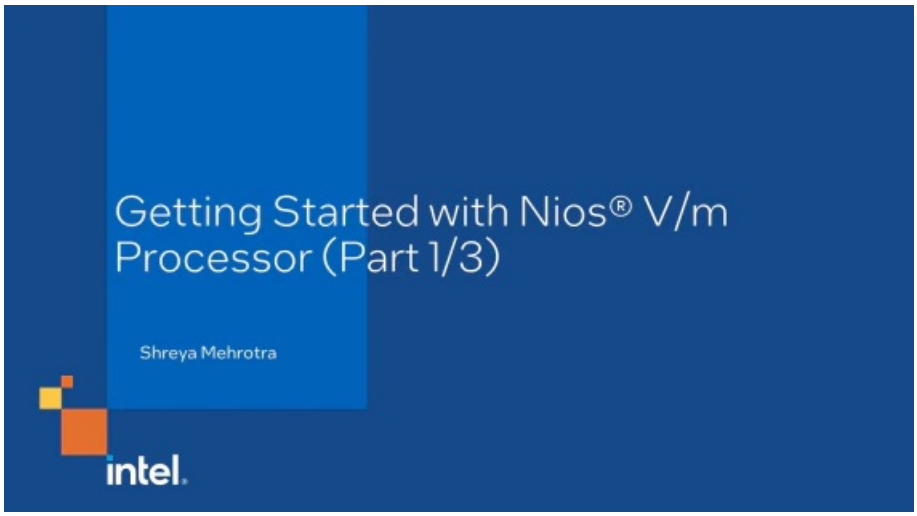

Nios® V Processor Intel® FPGA IP Release Notes

The Intel® FPGA IP version (X.Y.Z) number can change with each Intel Quartus® Prime software version. A

change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Nios V Processor Reference Manual
  Provides information about the Nios V processor performance benchmarks, processor architecture, the programming model, and the core implementation (Intel Quartus Prime Pro Edition User Guide).
- Nios II and Embedded IP Release Notes
- Nios V Embedded Processor Design Handbook
  Describes how to most effectively use the tools, recommends design styles, and practices for developing, debugging, and optimizing embedded systems using the Nios® V processor and Intel-provided tools (Intel Quartus Prime Pro Edition User Guide).
- Nios® V Processor Software Developer Handbook
  Describes the Nios® V processor software development environment, the tools that are available, and the process to build software to run on Nios® V processor (Intel Quartus Prime Pro Edition User Guide).

Nios® V/m Processor Intel FPGA IP (Intel Quartus Prime Pro Edition) Release Notes

Nios® V/m Processor Intel FPGA IP v22.3.0

Table 1. v22.3.0 2022.09.26

Intel Quartus Prime Version	Description	Impact
22.3	• Enhanced prefetch logic. Updated the following performance and benchmark numbers: — FMAX — Area — Dhrystone — CoreMark • Remove exceptionOffset and exceptionAgent parameters from _hw.tcl. *Note:* Only impacted BSP generation. No impact on RTL or circuit. • Changed debug reset: — Added ndm_reset_in port — Renamed dbg_reset to dbg_reset_out.	_

Nios® V/m Processor Intel FPGA IP v21.3.0

Table 2.v21.3.0 2022.06.21

Intel Quartus Prime Version	Description	Impact
22.2	• Added a reset request interface • Removed unused signals that caused a latch interface • Fixed debug reset issue: — Updated the routing of ndmreset to prevent the debug module from resetting.	–

Nios® V/m Processor Intel FPGA IP v21.2.0

Table 3. v21.2.0 2022.04.04

Intel Quartus Prime Version	Description	Impact
22.1	• Added new design examples in the Nios® V/m Processor Intel FPGA IP core parameter editor: — uC/TCP-IP IPerf Example Design — uC/TCP-IP Simple Socket Server Example Design	–
	• Bug Fix: — Addressed issues causing unreliable accesses to the MARCHID, MIMPID, and MVENDORID CSRs. — Enabled reset capability from the debug module to allow the core to be reset through a debugger. — Enabled support for trigger. The Nios V processor core supports 1 trigger. — Addressed reported synthesis warnings and lint issues. — Addressed an issue from the debug ROM that caused a corruption in the return vector. — Fixed an issue which prevented access to GPR 31 from the debug module.	–

Nios V/m Processor Intel FPGA IP v21.1.1

Table 4. v21.1.1 2021.12.13

Intel Quartus Prime Version	Description	Impact
21.4	• Bug Fix: — Trigger registers accessible but triggers were not supported issue fixed.	Illegal instruction exception prompted when accessing trigger registers.
	• Added new Design Example in the Nios V/m Processor Intel FPGA IP core parameter editor. — GSFI Bootloader Example Design — SDM Bootloader Example Design	–

Nios V/m Processor Intel FPGA IP v21.1.0

Table 5.v21.1.0 2021.10.04

Intel Quartus Prime Version	Description	Impact
21.3	Initial Release	–

Nios V/m Processor Intel FPGA IP (Intel Quartus Prime Standard Edition) Release Notes

Nios V/m Processor Intel FPGA IP v1.0.0

Table 6. v1.0.0 2022.10.31

Intel Quartus Prime Version	Description	Impact
22.1std	Initial release.	–

Archives

Intel Quartus Prime Pro Edition

Nios V Processor Reference Manual Archives

For the latest and previous versions of this user guide, refer to Nios® V Processor Reference Manual. If an IP or software version is not listed, the user guide for the previous IP or software version applies.
IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

Nios V Embedded Processor Design Handbook Archives

For the latest and previous versions of this user guide, refer to Nios® V Embedded Processor Design Handbook. If an IP or software version is not listed, the user guide for the previous IP or software version applies.
IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

Nios V Processor Software Developer Handbook Archives

For the latest and previous versions of this user guide, refer to Nios® V Processor Software Developer Handbook. If an IP or software version is not listed, the user guide for the previous IP or software version applies.
IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

Intel Quartus Prime Standard Edition

Refer to the following user guides for information about the Nios V processor for the Intel Quartus Prime Standard Edition.

Related Information

- Nios® V Embedded Processor Design Handbook Describes how to most effectively use the tools, recommends design styles, and practices for developing, debugging, and optimizing embedded systems using

the Nios® V processor and Intel-provided tools (Intel Quartus Prime Standard Edition User Guide).

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