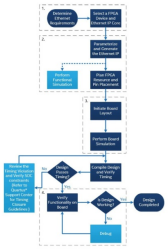

intel Migration Guidelines from Arria 10 to Stratix 10 for 10G Ethernet Subsystem User Guide

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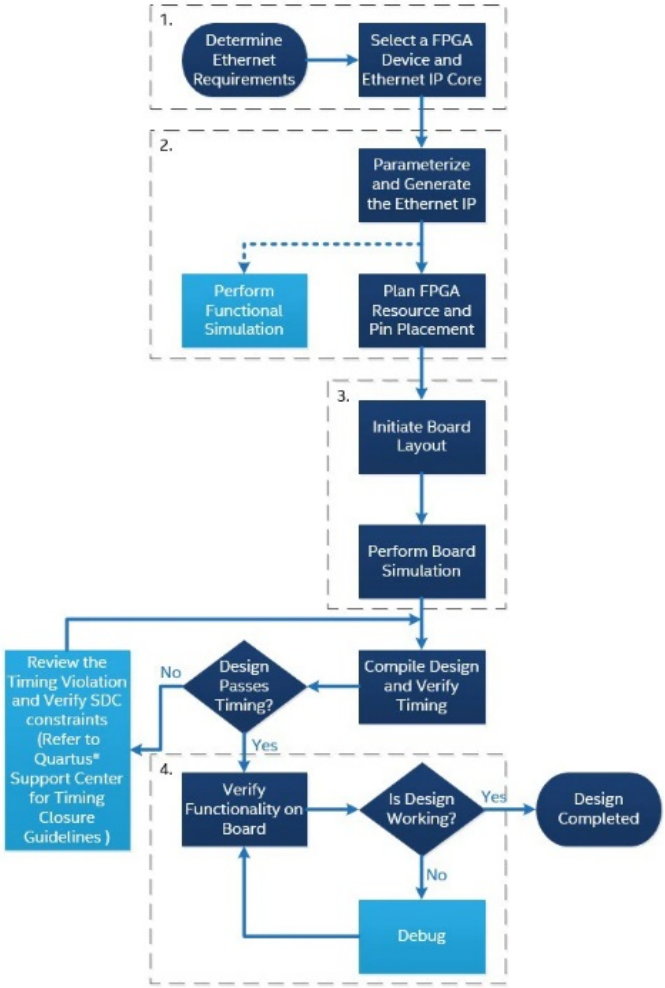
intel Migration Guidelines from Arria 10 to Stratix 10 for 10G Ethernet Subsystem

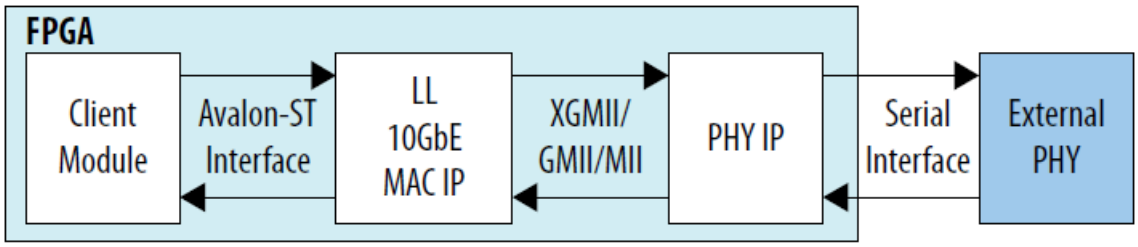


Migration Guidelines from Intel® Arria® 10 to Intel® Stratix® 10 for 10G Ethernet Subsystem

The Low Latency (LL) Ethernet 10G (10GbE) Media Access Controller (MAC) Intel® FPGA IP core includes Intel Stratix® 10 and Intel Arria® 10 design examples that are compliant with IEEE 802.3-2008 specifications. The interfaces between Intel Stratix 10 LL 10GbE MAC Intel FPGA IP core and physical interface (PHY) IP core are different compared to Intel Arria 10 LL 10GbE MAC Intel FPGA IP core with PHY IP core.

These migration guidelines are meant for those are familiar with Intel Arria 10 LL 10GbE MAC Intel FPGA IP core. Use these migration guidelines if you want to migrate your Intel Arria 10 LL 10GbE MAC design to use Intel Stratix 10 devices.

Intel Stratix 10 LL 10GbE MAC System



Comparison between Intel Stratix 10 and Intel Arria 10 Design Examples for LL 10GbE MAC Intel FPGA IP Core

Design Example	MAC Variant	PHY	Development Kit	Intel Arria 10	Intel Stratix 10
10GBASE-R Ethernet	10G	Native PHY (Support L/H-tile Native PHY for Intel Stratix 10)	Intel Arria 10/ Intel Stratix 10 GX Transceiver Signal Integrity	Yes	Yes
1G/2.5G Ethernet with 1588	1G/2.5G	1G/2.5G/5G/10G Multi-rate Ethernet PHY	Intel Arria 10/ Intel Stratix 10 GX Transceiver Signal Integrity	Yes	Yes
1G/2.5G/10G Ethernet	1G/2.5G/10G	1G/2.5G/5G/10G Multi-rate Ethernet PHY	Intel Arria 10/ Intel Stratix 10 GX Transceiver Signal Integrity	Yes	Yes
10GBASE-R Register Mode Ethernet	10G	Native PHY	Intel Arria 10 GX Transceiver Signal Integrity	Yes	Not available
XAUI Ethernet	10G	XAUI PHY	Intel Arria 10 GX FPGA	Yes	Not available
1G/10G Ethernet	1G/10G	1G/10GbE and 10GBASE-KR PHY	Intel Arria 10 GX Transceiver Signal Integrity	Yes	Not available
continued.					

Design Example	MAC Variant	PHY	Development Kit	Intel Arria 10	Intel Stratix 10
1G/10G Ethernet with 1588	1G/10G	1G/10GbE and 10GBASE-KR PHY	Intel Arria 10 GX Transceiver Signal Integrity	Yes	Not available
10M/ 100M/1G/10G Ethernet	10M/ 100M/1G/10G	1G/10GbE and 10GBASE-KR PHY	Intel Arria 10 GX Transceiver Signal Integrity	Yes	Not available
10M/ 100M/1G/10G Ethernet with 1588	10M/ 100M/1G/10G	1G/10GbE and 10GBASE-KR PHY	Intel Arria 10 GX Transceiver Signal Integrity	Yes	Not available
1G/2.5G Ethernet	1G/2.5G	1G/2.5G/5G/10G Multi-rate Ethernet PHY	Intel Arria 10 GX Transceiver Signal Integrity	Yes	Not available
10G USXGMII Ethernet	1G/2.5G/5G/10G (USXGMII)	1G/2.5G/5G/10G Multi-rate Ethernet PHY	Intel Arria 10 GX Transceiver Signal Integrity	Yes	Not available

Note:
You can access the listed design examples through the LL 10GbE MAC parameter editor in the Intel Quartus® Prime Pro Edition software.

Related Information

- Low Latency Ethernet 10G MAC User Guide
- Intel Stratix 10 Low Latency Ethernet 10G MAC Design Example User Guide
- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

Supported Configurations for Intel Stratix 10 and Intel Arria 10 LL 10GbE MAC Designs

The following table lists all the possible Intel Stratix 10 and Intel Arria 10 Ethernet IP configurations.

Supported Configurations for Intel Arria 10 and Intel Stratix 10 Ethernet IP Configuration

IP Core		Intel Arria 10	Intel Stratix 10
LL 10GbE MAC	Speed	• 10G	
		• 1G/10G	
		• 10M/100M/1G/10G	
		• 1G/2.5G	
		• 1G/2.5G/10G	
		• 1G/2.5G/5G/10G (USXGMII interface)	
		• 10M/100M/1G/2.5G	
		• 10M/100M/1G/2.5G/10G	
	IEEE 1588v2 feature	• 10G	• 10G
		• 1G/10G	• 1G/10G
		• 10M/100M/1G/10G	• 10M/100M/1G/10G
		• 1G/2.5G	• 1G/2.5G
			• 1G/2.5G/10G

continued.

IP Core		Intel Arria 10	Intel Stratix 10
1G/2.5G/5G/10G Multi-rate Ethernet PHY	Speed	• 2.5G • 1G/2.5G • 1G/2.5G/10G (MGBASE-T PHY) • 1G/2.5G/5G/10G (USXGMII interface/NBASE-T PHY)	
	IEEE 1588v2 feature	• 2.5G • 1G/2.5G	• 2.5G • 1G/2.5G • 1G/2.5G/10G Not supported for enabled SGMII mode.
	SGMII Mode	Not available	• 1G/2.5G • 1G/2.5G/10G
XAUI PHY		Available	Not available
Intel Stratix 10 L-tile/H-tile Transceiver Native PHY		Not available	Supported presets: • 10GBASE-R • 10GBASE-R 1588 • 10GBASE-R Low Latency • 10GBASE-R with KR FEC
Intel Arria 10 Transceiver Native PHY		Supported presets: • 10GBASE-R • 10GBASE-R Register Mode • 10GBASE-R Low Latency • 10GBASE-R with KR FEC	Not available
Intel Arria 10 1G/10GbE and 10GBASE-KR PHY		Available	Not available
Intel Stratix 10 10GBASE-KR PHY		Not available	Available

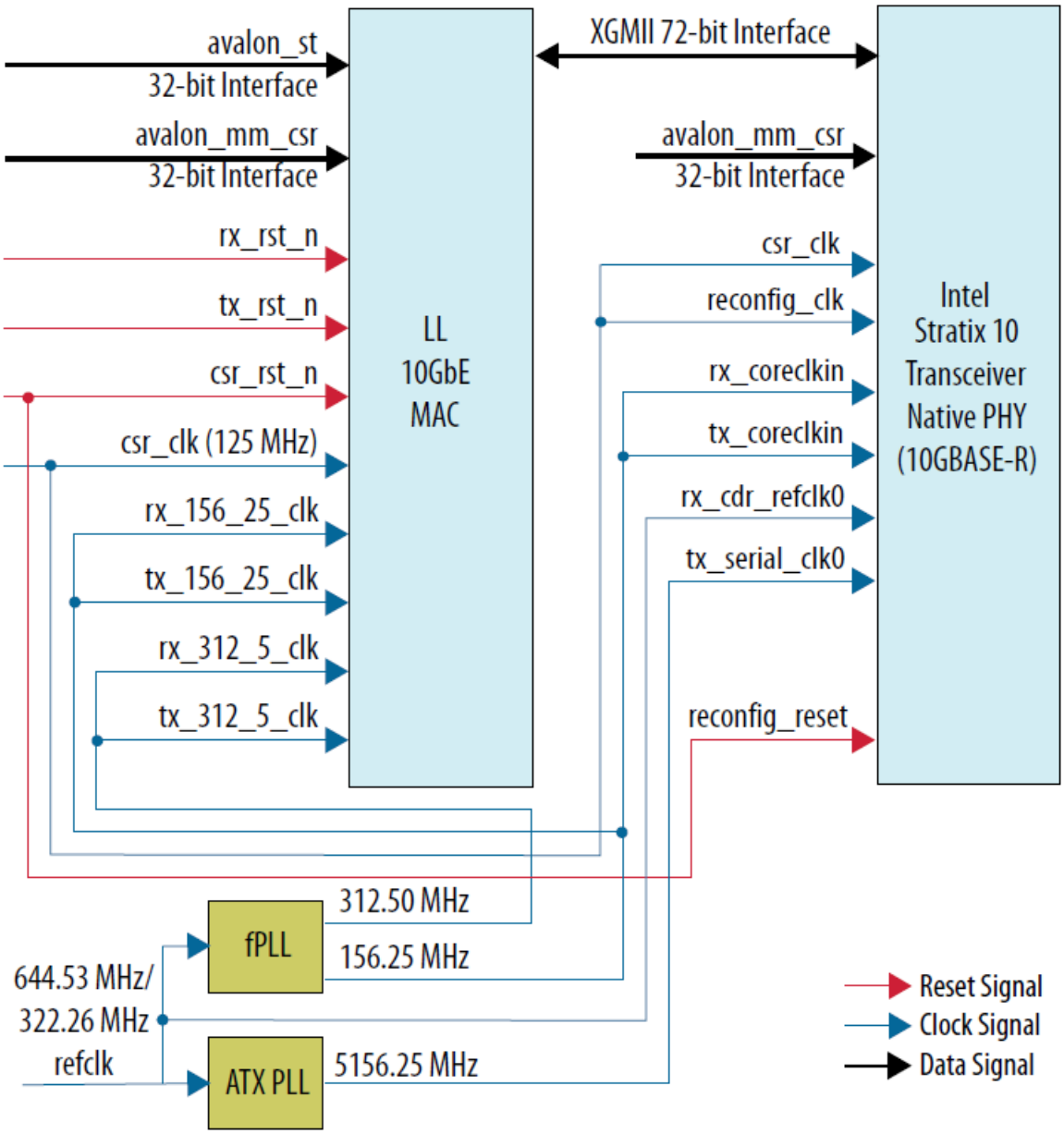
Clocking and Reset Infrastructure

Intel Stratix 10 LL 10GbE MAC and Intel Stratix 10 Transceiver Native PHY IP Cores

You can configure the Intel Stratix 10 Transceiver Native PHY IP core to implement 10GBASE-R PHY with the Ethernet-specific physical layer running at 10.3125 Gbps data rate as defined in Clause 49 of IEEE 802.3-2008 specification. This configuration provides an XGMII to LL 10GbE MAC Intel FPGA IP core and implements a single-channel 10.3125Gbps PHY for a direct connection to a small form-factor pluggable plus (SFP+) optical module using the small form-factor interface (SFI) electrical specification.

The following figure illustrates the migration from an Intel Arria 10 design to an Intel Stratix 10 design.

Clocking and Reset Scheme for LL 10GbE MAC and Intel Stratix 10 Transceiver Native PHY in 10GBASE-R Design Example Interface



Related Information

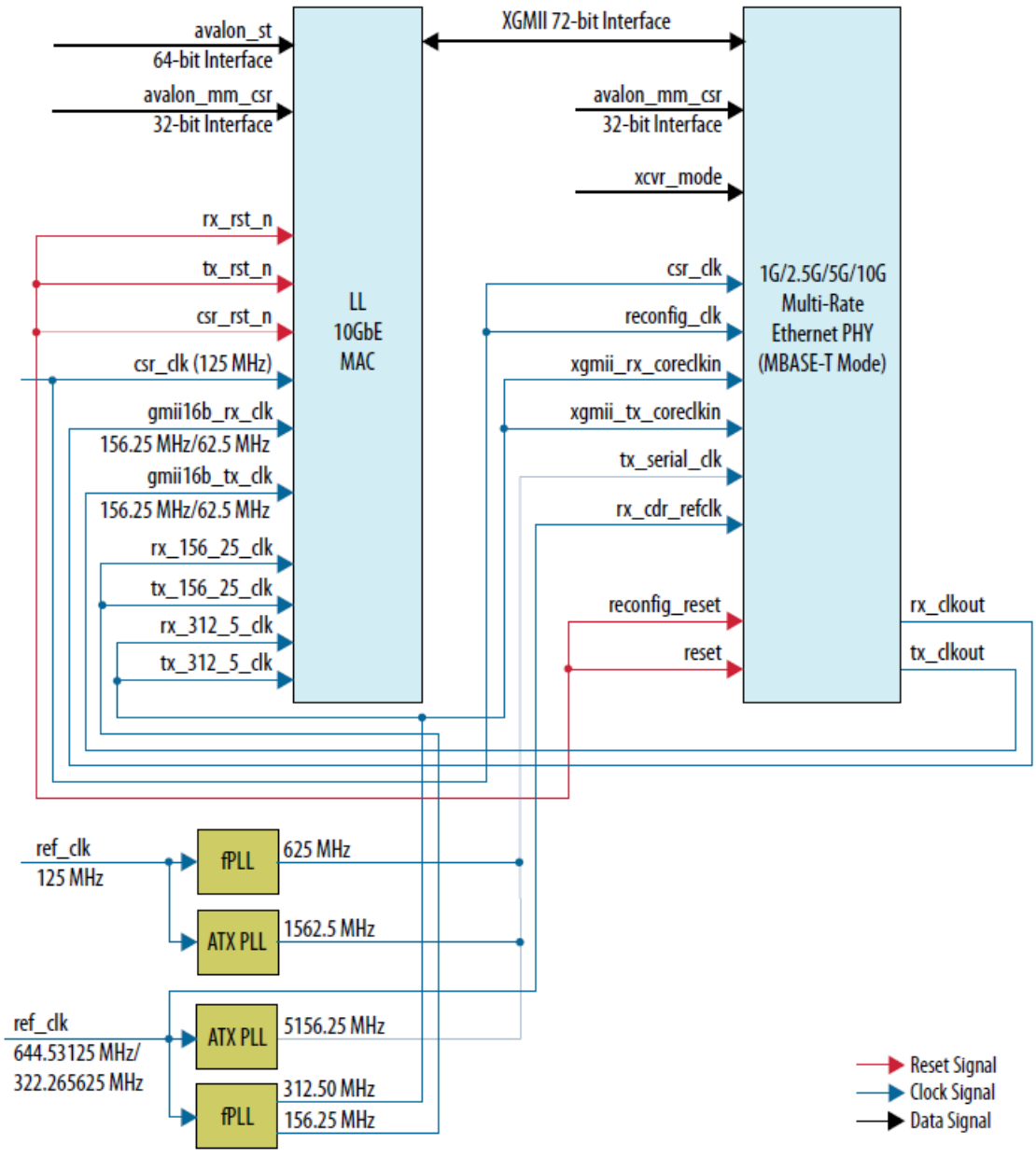
AN795: Implementing Guidelines for 10G Ethernet Subsystem Using Low Latency 10G MAC IP Core in Arria 10 Devices

Intel Stratix 10 LL 10GbE MAC and Intel Stratix 10 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP Cores

1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP core for Intel Stratix 10 devices provides GMII and XGMII to the LL 10GbE MAC Intel FPGA IP core. The 1G/ 2.5G/5G/10G Multi-rate Ethernet PHY IP core implements a single channel 1G/ 2.5G/5G/10Gbps serial PHY. The design provides a direct connection to 1G/2.5GbE dual speed SFP+ pluggable modules, MGBASE-T copper external PHY devices, or chip-to-chip interfaces. These IP cores support reconfigurable data rates.

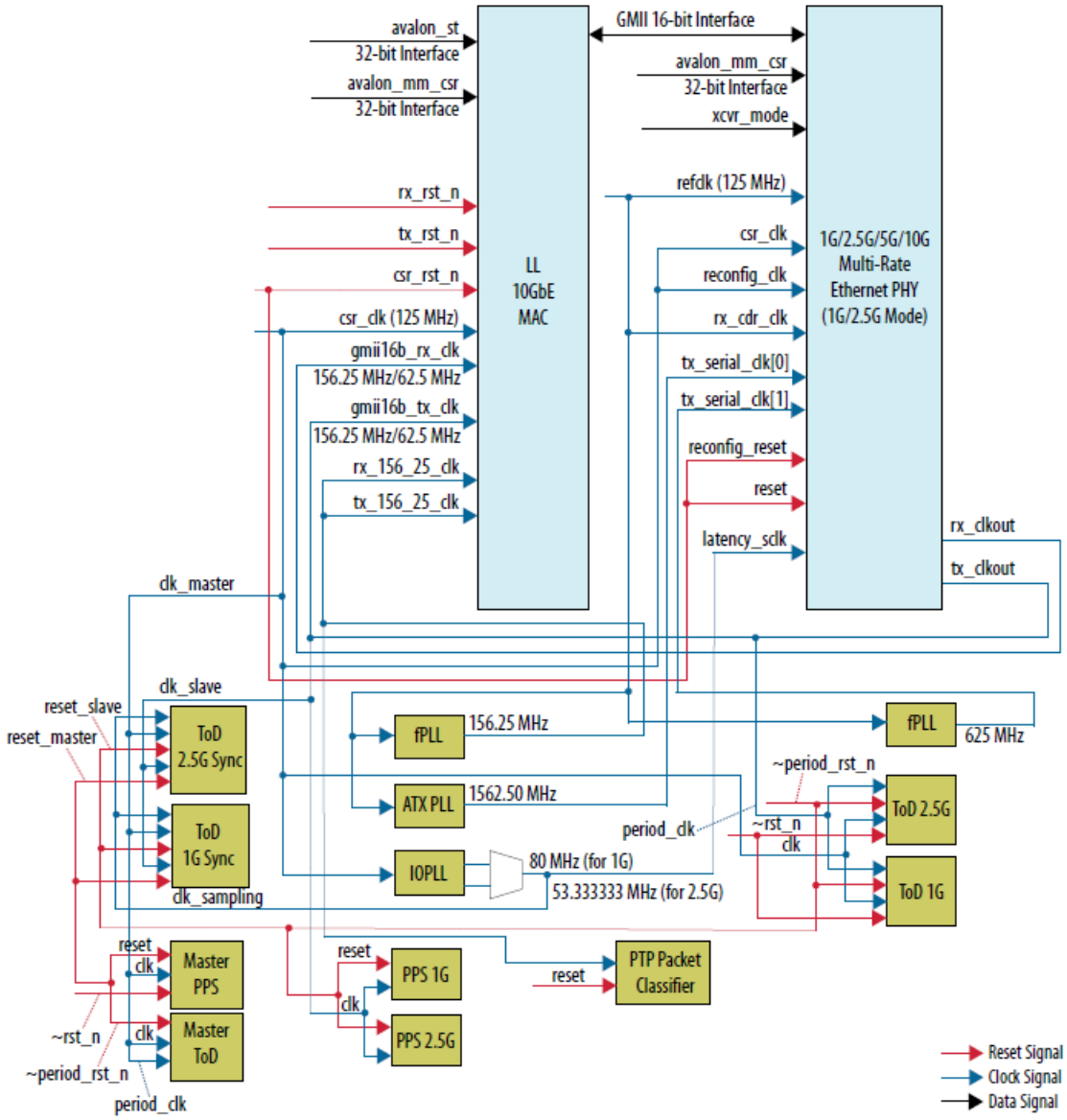
The following figure illustrates then migration from an Intel Arria 10 design to a Intel Stratix 10 design.

Clocking and Reset Scheme for LL 10GbE MAC and 1G/2.5G/5G/10G Multi-rate Ethernet PHY Design Example (1G/2.5G/10G Mode) for Intel Stratix 10 Deviecs



The following figure illustrates the latest clocking and reset scheme of the 1G/2.5G Ethernet with IEEE 1588v2 feature design example targeted on Intel Stratix 10 devices. There are differences between this solution and the version that was introduced in the Intel Arria 10 devices. Modification is needed when migrating design from the Intel Arria 10 devices to the Intel Stratix 10 devices.

Clocking and Reset Scheme for LL 10GbE MAC and 1G/2.5G/5G/10G Multi-rate Ethernet PHY Design Example (1G/2.5G Mode with IEEE 1588v2 Feature) for Intel Stratix 10 Devices

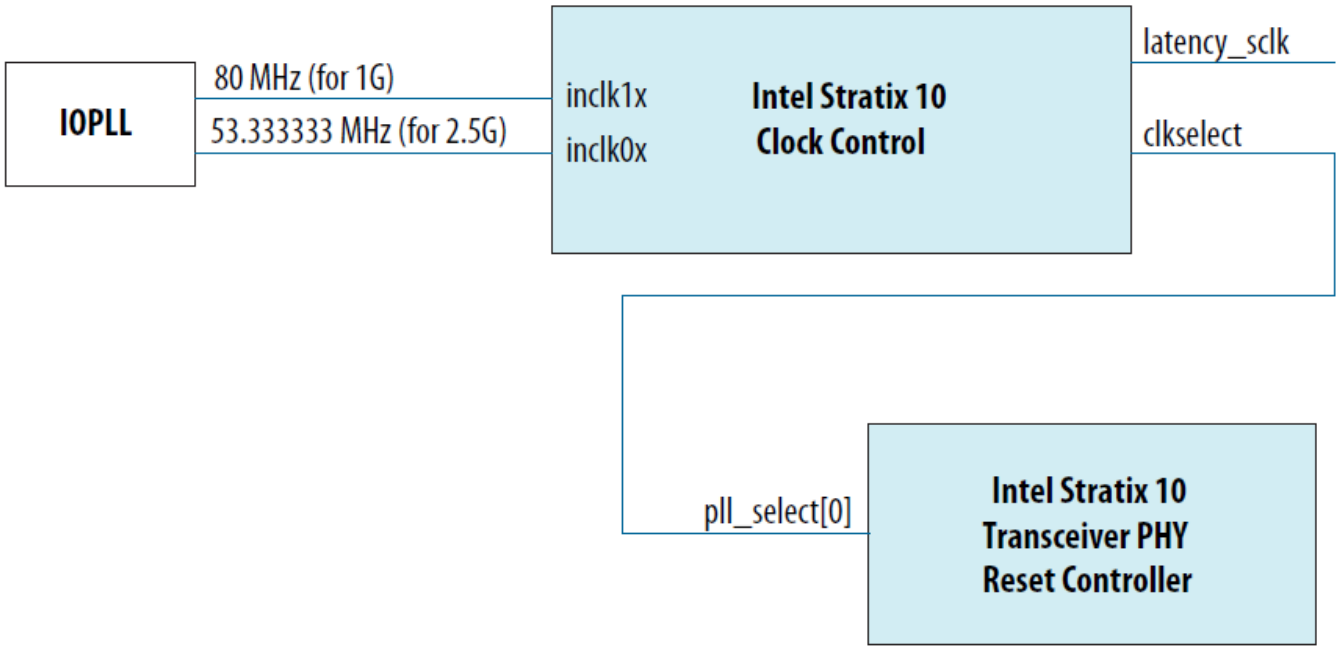


A new input clock port latency_sclk is available in Intel Stratix 10 devices. This port is available when you turn on the Enable latency measurement ports parameter in the Intel Stratix 10 L/H-Tile Transceiver Native PHY IP core or the Enable IEEE 1588 Precision Time Protocol parameter in the 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP core. This port is required for the deterministic latency measurement model for Intel Stratix 10 devices. For more information, refer to the Deterministic Latency Use Model chapter in Intel Stratix 10 L/H-Tile Transceiver PHY User Guide.

To connect an I/O phase-locked loop (IOPLL), add an Intel Stratix 10 Clock Control (stratix10_clkctrl) IP from the IP Catalog. The IOPLL provides two sampling clocks in this design: 53.33 MHz for 2.5G mode and 80 MHz for 1G mode.

The following figure illustrates the connectivity details based on the 1G/2.5G Ethernet design.

Connectivity Diagram for 1G/2.5G Ethernet with 1588 Design for Intel Stratix 10 Devices



You must ensure that the inclk0x port connects to 2.5G sampling clock and the inclk1x port connects to 1G sampling clock. The output clock port of clock control becomes the latency_sclk port. For design migration from the Intel Arria 10 devices to the Intel Stratix 10 devices, you can reuse the similar connectivity between the 1G/2.5G reconfiguration block and transceiver reset controller.

Related Information

- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide
- **AN795:** Implementing Guidelines for 10G Ethernet Subsystem Using Low Latency 10G MAC IP Core in Arria 10 Devices
- Intel Stratix 10 Clocking and PLL User Guide

IP Register Mapping

The LL 10GbE MAC Intel FPGA IP core for Intel Stratix 10 devices uses the same register map as LL 10GbE MAC Intel FPGA IP core for Intel Arria 10 devices. The Multi-rate Ethernet PHY and 10GBASE-R PHY presets also use the same register map for both Intel Stratix 10 and Intel Arria 10 designs. The LL 10GbE MAC Intel FPGA IP core for Intel Stratix 10 devices still supports backward compatibility with 10GbE IP with 64-bit Avalon Memory-Mapped (MM) adapter.

Related Information
Low Latency Ethernet 10G MAC User Guide.

Signal Connectivity Differences between Intel Stratix 10 and Intel Arria 10 Ethernet Design Examples

For LL 10GbE MAC Intel FPGA IP core, there are no new signals introduced for Intel Stratix 10 devices. There are new asynchronous reset status signals introduced in Intel Stratix 10 L/H-Tile Transceiver Native PHY IP Core. The differences apply to all Ethernet PHY IP cores, which include all variants of 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP cores and 10GBASE-R PHY Intel FPGA IP core.

Interface Signal Differences Between Intel Stratix 10 L/H-Tile Transceiver Native PHY/Multi-rate Ethernet PHY and Intel Arria 10 Transceiver Native PHY/Multi-rate Ethernet PHY

Note: <n> = The number of lanes.

Intel Stratix 10 Interface Signals	Intel Arria 10 Interface Signals	Comments
tx_analogreset_stat[<n>-1 :0]	Not available	These reset status ports are newly introduced in Intel Stratix 10 devices only. Connect to the corresponding signal in the Transceiver PHY Reset Controller IP core, which implements the appropriate reset sequence for the device.
rx_analogreset_stat[<n>-1 :0]	Not available	
tx_digitalreset_stat[<n>- 1:0]	Not available	
rx_digitalreset_stat[<n>- 1:0]	Not available	
latency_sclk	Not available	Latency measurement input reference clock. Sampling clock for measuring the latency of the transceiver application interface block (AIB) datapath. This port is available when the latency measurement ports option in the Intel Stratix 10 L/H-Tile Transceiver Native PHY IP core or the IEEE 1588 Precision Time Protocol option in the 1G / 2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP core is enabled.
reconfig_address [log_2<n> +10:0]	reconfig_address [log_2<n>+9: 0]	Reconfiguration address signal connected to the reconfiguration block. Address bus that used to specify address to be accessed for both read and write operations.

Interface Signal Differences Between Intel Stratix 10 Transceiver Reset Controller IP and Intel Arria 10 Transceiver Reset Controller IP

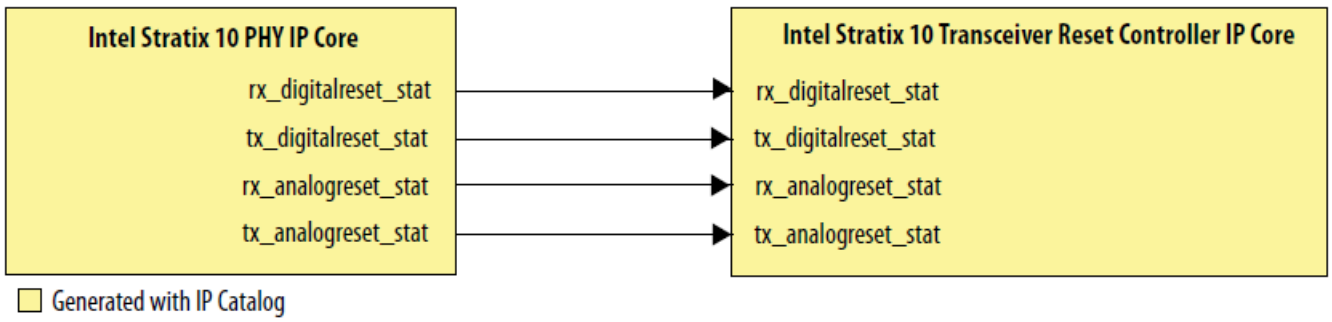
Note: <n> = The number of lanes.

Intel Stratix 10 Interface Signals	Intel Arria 10 Interface Signals	Comments
tx_analogreset_stat[<n>-1:0]	Not available	This is reset status signal from the Transceiver Native PHY IP Core. There is one tx_analogreset_stat per channel. When asserted, reset sequence for TX PMA begins. When deasserted, reset sequence for TX PMA ends.
rx_analogreset_stat[<n>-1:0]	Not available	This is reset status signal from the Transceiver Native PHY IP Core. There is one rx_analogreset_stat per channel. When asserted, reset sequence for RX PMA begins. When deasserted, reset sequence for RX PMA ends.
tx_digitalreset_stat[<n>- 1:0]	Not available	This is reset status signal from the Transceiver Native PHY IP Core. There is one tx_digitalreset_stat per channel. When asserted, reset sequence for TX PCS begins.
continued.		

Intel Stratix 10 Interface Signals	Intel Arria 10 Interface Signals	Comments
		When deasserted, reset sequence for TX PCS ends.
rx_digitalreset_stat[<n>- 1:0]	Not available	This is reset status signal from the Transceiver Native PHY IP Core. There is one rx_digitalreset_stat per channel. When asserted, reset sequence for RX PCS begins. When deasserted, reset sequence for RX PCS ends.

The following figure illustrates the connectivity of reset status signals for the Intel Stratix 10 Ethernet 10G subsystem design. This is applicable if you use either the Intel Stratix 10 L-tile/H-tile Native PHY IP core or the 1G/2.5G/5G/10G Multi-rate PHY Intel FPGA IP core.

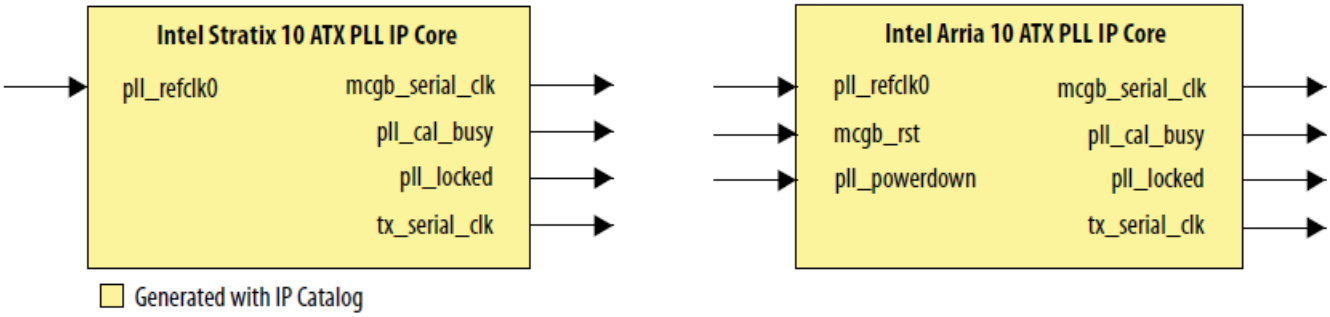
Reset Status Signals Connectivity Diagram for Intel Stratix 10 PHY IP Core and Reset Controller IP Core



There are some changes to the ATX PLL and fPLL interface signals for the Intel Stratix 10 devices compared to the Intel Arria 10 devices. If you are migrating Ethernet designs from a Intel Arria 10 device to a Intel Stratix 10 device, remove the mcgb_rst and pll_powerdown reset signals because they are not available in Intel Stratix 10.

The following figure illustrates the difference between Intel Stratix 10 L-Tile/H-Tile ATX PLL and Intel Arria 10 ATX PLL.

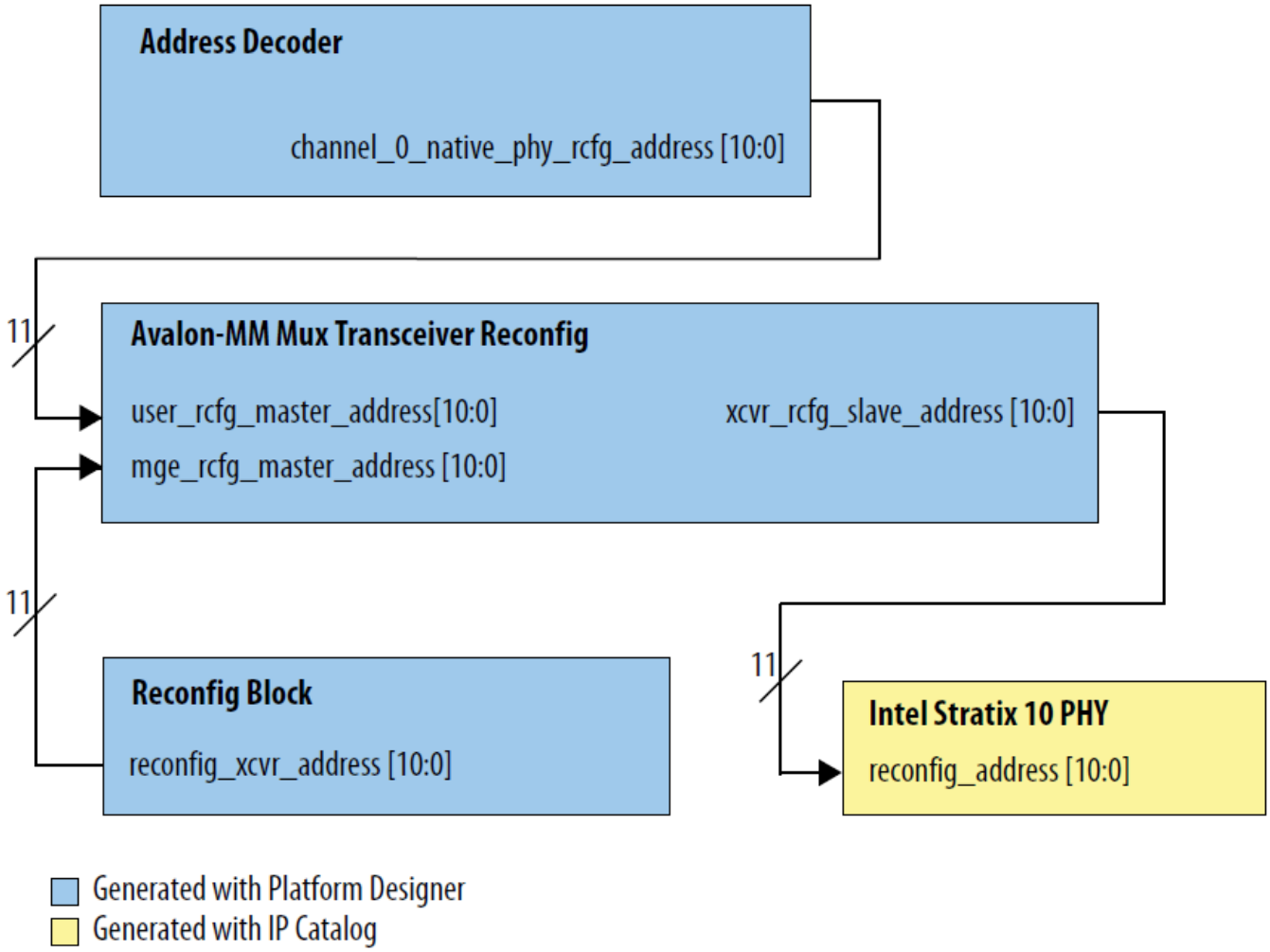
Comparison between Interface Signals for Intel Stratix 10 L-Tile/H-Tile Transceiver ATX PLL and Intel Arria 10 Transceiver ATX PLL



Another change on Intel Stratix 10 L-Tile/H-Tile Transceiver PHY is the additional 1 bit added to the reconfig_address bus, compared to the Intel Arria 10 Transceiver PHY version. The same change is required for the Multi-rate PHY as it is created by using the Native PHY as the baseline.

The following figure illustrates how to connect the reconfig_address.

Block Diagram on Reconfiguration Address Connectivity for Intel Stratix 10 Ethernet Subsystem Design
The example shown is based on the Ethernet design example model. For the blocks that are generated by Platform Designer, you can obtain the modules from the design example files.



Related Information

- Intel Stratix 10 Low Latency Ethernet 10G MAC Design Example User Guide
- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide
- Intel Stratix 10 Clocking and PLL User Guide

Migration Flow

Only Intel Quartus Prime Pro Edition software offers Intel Stratix 10 designs. If you are using an Intel Arria 10 Ethernet design from the Intel Quartus Prime Standard Edition, you need to migrate to Intel Quartus Prime Pro Edition version for any Intel Stratix 10 design.

Related Information
Intel Quartus Prime Pro Edition Handbook Volume 1: Design and Compilation

- Provides more information about upgrading IP cores and Qsys Pro systems to Quartus Prime Pro Edition software.

Document Revision History for AN 808

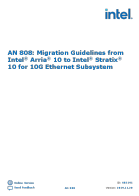
Migration Guidelines from Intel Arria 10 to Intel Stratix 10 for 10G Ethernet Subsystem

Document Version	Changes
2019.11.20	• Rebranded as Intel. • Updated Figure: Clocking and Reset Scheme for LL 10GbE MAC and 1G/2.5G/5G/10G Multi-rate Ethernet PHY Design Example (1G/2.5G Mode with IEEE 1588v2 Feature) for Intel Stratix 10 Devices. • Made editorial updates throughout the document.

Date	Version	Changes
June 2017	2017.06.19	Initial release.

AN 808: Migration Guidelines from Intel® Arria® 10 to Intel® Stratix® 10 for 10G Ethernet Subsystem.

Documents / Resources

	intel Migration Guidelines from Arria 10 to Stratix 10 for 10G Ethernet Subsystem [pdf] User Guide Migration Guidelines from Arria 10 to Stratix 10 for 10G Ethernet Subsystem, Migration Guidelines, Arria 10 Migration Guidelines, Stratix 10 Migration Guidelines, 10G Ethernet Subsystem Migration Guidelines