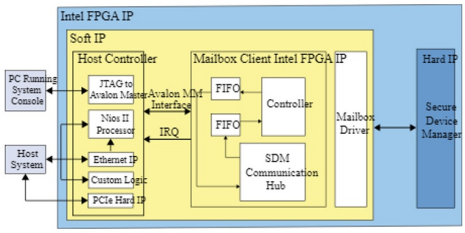

Mailbox Client Intel FPGA IP User Guide

Mailbox Client Intel® FPGA IP Release Notes

Contents

Mailbox Client Intel® FPGA IP Release Notes

Intel® Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.
FPGA IP versions match the Intel Quartus®
The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Introduction to Intel FPGA IP Cores
- Mailbox Client Intel FPGA IP User Guide
- Errata for other IP cores in the Knowledge Base

1.1. Mailbox Client Intel FPGA IP v20.2.0

Table 1. v20.2.0 2022.09.26

Intel Quartus Prime Version	Description	Impact
22.3	Added LibRSU support with Nios® V processor to use with the secure device manager (SDM).	—

1.2. Mailbox Client Intel FPGA IP v20.1.2

Table 2. v20.1.2 2022.03.28

Intel Quartus Prime Version	Description	Impact
22.	Updated response for CONFIG_STATUS command to include information on the configuration clock source.	Allows configuration of FPGA without a tile refclk present at time of configuration.
	Enhanced the interrupt status register (ISR) and interrupt enable register (IER) to add protection for command/response and read/ write FIF0s.	
	Removed mailbox command REBOOT_HPS as this command is unavailable for this IP.	

1.3. Mailbox Client Intel FPGA IP v20.1.1

Table 3. v20.1.1 2021.12.13

Intel Quartus Prime Version	Description	Impact
21.4	• Updated crypto service-specific parameter name from HAS_OFFLOAD to Enable Crypto Service • Replace safeclib memcpy implementation with generic memcpy in HAL driver.	—

1.4. Mailbox Client Intel FPGA IP v20.1.0

Table 4. v20.1.0 2021.10.04

Intel Quartus Prime Version	Description	Impact
21.3	Added HAS_OFFLOAD parameter to support cryptographic offloading. This feature is only available for Intel Agilex™ devices.	When set, the IP enables the crypto AXI initiator interface.
	Changed the Release Notes part number from RN-1201 to RN-1259.	—

1.5. Mailbox Client Intel FPGA IP v20.0.2

Table 5. v20.0.2 2021.03.29

Intel Quartus Prime Version	Description	Impact
21.	Added support to reset Timer 1 and Timer 2 delay registers during the event of Mailbox Client Intel FPGA IP reset assertion.	No impact in Timer 1 and Timer 2 registers usage in Intel Quartus Prime software version from 20.2 and 20.4. You must regenerate the Mailbox Client Intel FPGA IP when moving from Intel Quartus Prime software version 20.4 or earlier to Intel Quartus Prime software version 21.1.
	Added support to enable the connection capability between Mailbox Client Intel FPGA IP IRQ signal and Nios II processor IRQ signal.	You must migrate to Intel Quartus Prime software version 21.1 and regenerate Mailbox Client Intel FPGA IP to enable this feature.

1.6. Mailbox Client Intel FPGA IP v20.0.0

Table 6. v20.0.0 2020.04.13

Intel Quartus Prime Version	Description	Impact
20.	Added support for the EOP_TIMEOUT interrupt which indicates that the full command did not include the End of Packet.	You can use these interrupts to handle error detection for incomplete transactions.
	Added support for the BACKPRESSURE_TIMEOUT interrupt which indicates that an error within the SDM occurred.	

1.7. Mailbox Client Intel FPGA IP v19.3

Table 7. v19.3 2019.09.30

Intel Quartus Prime Version	Description	Impact
19.	Added device support for Intel Agilex devices.	You can now use this IP in I ntel Agilex devices.
	Added support for an COMMAND_INVALID interrupt which indicates the command length specified the header does n ot match the actual command sent.	You can use this interrupt to identify incorrectly specified commands.
	Changed the name of this IP from Intel FPGA Stratix 10 M ailbox Client to Mailbox Client Intel FPGA IP.	This IP now supports both In tel Stratix® 10 and Intel Agil ex devices. Use the new na me to find this P in the Intel Quartus Prime software or o n the web.
	Added new IP version structure.	The IP version number may change from one Intel Quart us Prime software version to another.

1.8. Intel FPGA Stratix 10 Mailbox Client v17.1

Table 8. v17.1 2017.10.30

Intel Quartus Prime Version	Description	Impact
17.	Initial release.	—

1.9. Mailbox Client Intel FPGA IP User Guide Archives

For the latest and previous versions of this user guide, refer to Mailbox Client Intel FPGA IP User Guide. If an IP or software version is not listed, the user guide for the previous IP or software version applies.
IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

Mailbox Client Intel®
FPGA IP Release Notes
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Documents / Resources

	intel Mailbox Client Intel FPGA IP [pdf] User Guide Mailbox Client Intel FPGA IP, Client Intel FPGA IP, Intel FPGA IP, FPGA IP, IP

References

- 1. Introduction to Intel® FPGA IP Cores
- 1. Mailbox Client Intel FPGA IP User Guide
- 1. Intel® Quartus® Prime Design Suite Version 18.1 Update Release...
- 1. Mailbox Client Intel® FPGA IP Release Notes
- Intel ISO 9001:2015 Registrations
- FPGA Knowledge Base Articles Search