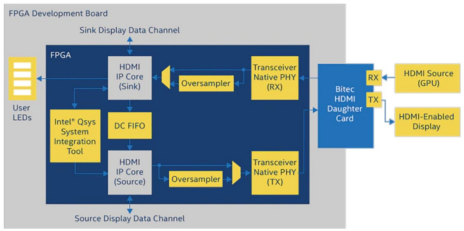

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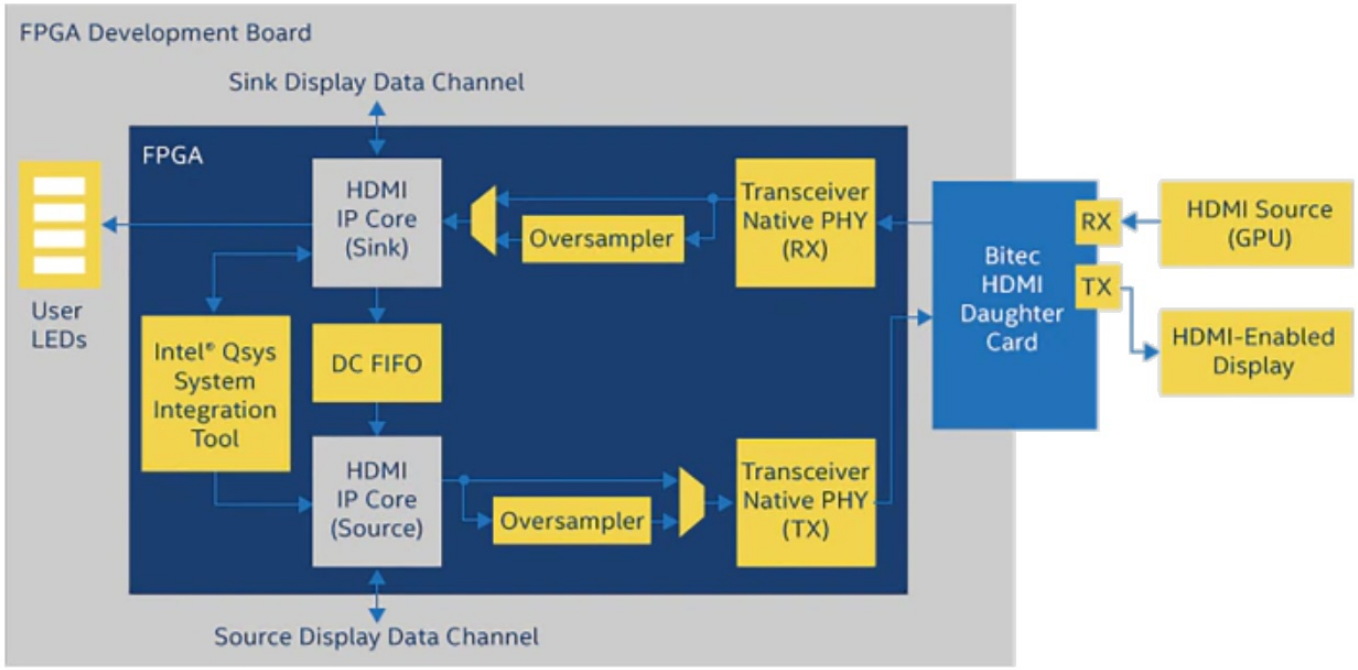
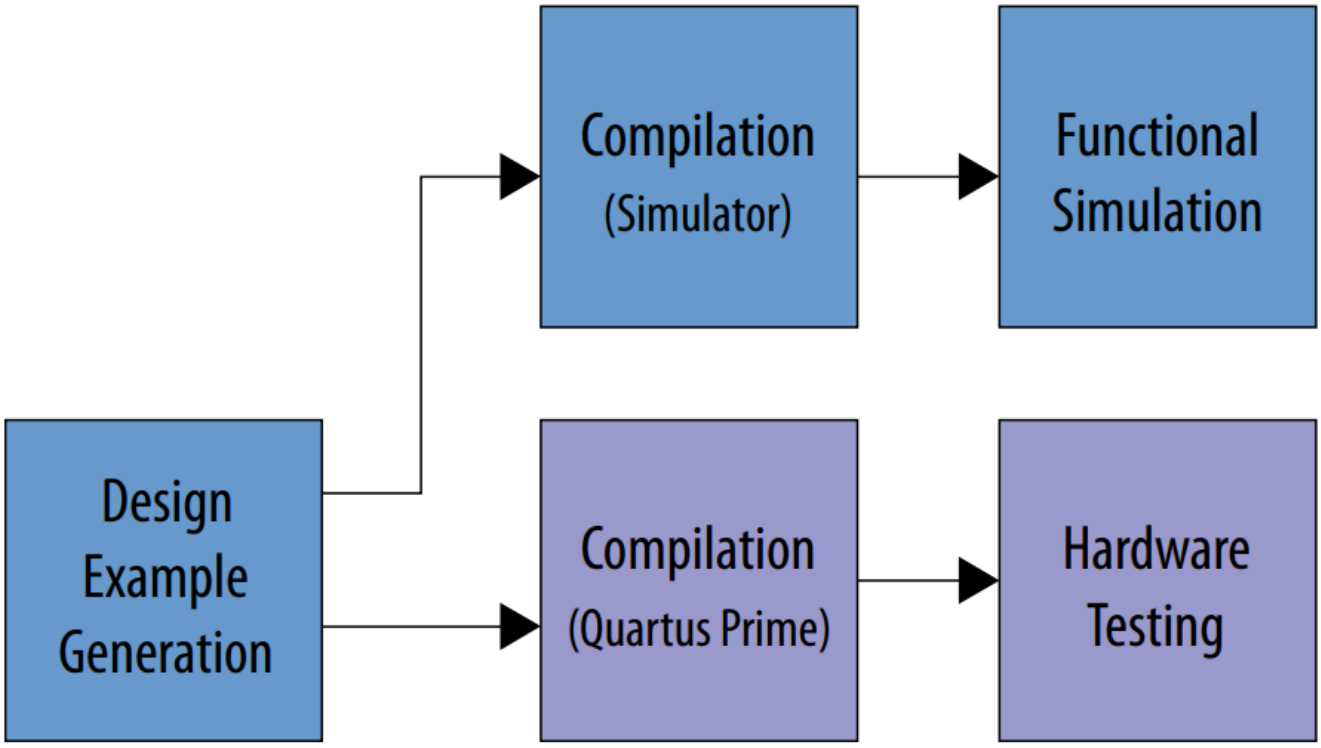


Contents

HDMI PHY Design Example Quick Start Guide for Intel® Arria® 10 Devices

The HDMI PHY Intel® FPGA IP design example for Intel Arria® 10 devices features a HDMI 2.0 RX-TX retransmit design that supports compilation and hardware testing.
When you generate a design example, the parameter editor automatically creates the files necessary to simulate, compile, and test the design in hardware.

Figure 1. Development Steps

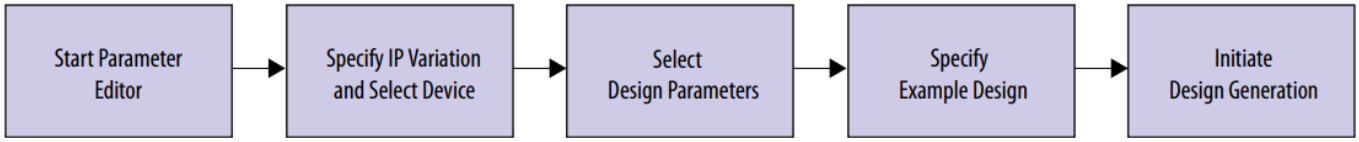


Related Information
HDMI PHY Intel FPGA IP User Guide

Generating the Design

Use the HDMI PHY Intel FPGA IP parameter editor in the Intel Quartus® Prime software to generate the design examples.

Figure 2. Generating the Design Flow

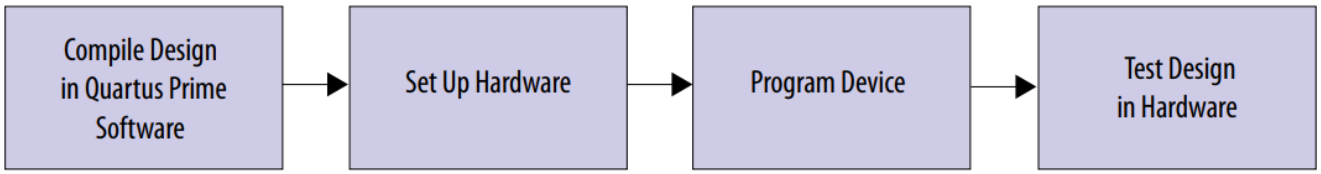


1. Create a project targeting Intel Arria 10 device family and select the desired device.
2. In the IP Catalog, locate and double-click Interface Protocols ➤ Audio & Video ➤ HDMI TX PHY Intel FPGA IP (or HDMI RX PHY Intel FPGA IP). The New IP Variant or New IP Variation window appears.
3. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file named .ip or .qsys.
4. Click OK. The parameter editor appears.

5. On the Design Example tab, select Arria 10 HDMI RX-TX Retransmit.
6. Select Simulation to generate the testbench, and select Synthesis to generate the hardware design example. You must select at least one of these options to generate the design example files.
   If you select both, the generation time is longer.
7. For Generate File Format, select Verilog or VHDL.
8. For Target Development Kit, select Intel Arria 10 GX FPGA Development Kit. If you select a development kit, then the target device changes to match the device on target board. For Intel Arria 10 GX FPGA Development Kit, the default device is 10AX115S2F4I1SG.
9. Click Generate Example Design.

Compiling and Testing the Design

To compile and run a demonstration test on the hardware example design, follow these steps:



1. Ensure hardware example design generation is complete.
2. Launch the Intel Quartus Prime software and open the **.qpf file: /quartus/a10_hdmi2_demo.qpf**
3. Click Processing ➤ Start Compilation.
4. After successful compilation, a .sof file is generated in the quartus/ output_files directory.
5. Connect Bitec HDMI 2.0 FMC Daughter Card Rev 11 to the on-board FMC port B (J2).
6. Connect TX (P1) of the Bitec FMC daughter card to an external video source.
7. Connect RX (P2) of the Bitec FMC daughter card to an external video sink or video analyzer.

8. Ensure all switches on the development board are in default position.
9. Configure the selected Intel Arria 10 device on the development board using the generated .sof file (Tools ➤ Programmer).
10. The analyzer should display the video generated from the source. Compiling and Testing the Design

Related Information
Intel Arria 10 FPGA Development Kit User Guide

HDMI PHY Intel FPGA IP Design Example Parameters

Table 1. HDMI PHY Intel FPGA IP Design Example Parameters for Intel Arria 10 Devices

These options are available for Intel Arria 10 devices only.

Parameter	Value	Description
Available Design Example		
Select Design	Arria 10 HDMI RX-TX Retransmit	Select the design example to be generated.
Design Example Files		
Simulation	On, Off	Turn on this option to generate the necessary files for the simulation testbench.
Synthesis	On, Off	Turn on this option to generate the necessary files for Intel Quartus Prime compilation and hardware demonstration.
Generated HDL Format		
Generate File Format	Verilog, VHDL	Select your preferred HDL format for the generated design example fileset. *Note:* This option only determines the format for the generated top level IP files. All other files (e.g., example testbenches and top level files for hardware demonstration) are in Verilog HDL format.

Target Development Kit		
Select Board	No Development Kit ,	Select the board for the targeted design example.
	Arria 10 GX FPGA Development Kit, Custom Development Kit	• No Development Kit: This option excludes all hardware aspects for the design example. The IP core sets all pin assignments to virtual pins. • Arria 10 GX FPGA Development Kit: This option automatically selects the project's target device to match the device on this development kit. You may change the target device using the **Change Target Device** parameter if your board revision has a different device variant. The IP core sets all pin assignments according to the development kit.
		• Custom Development Kit: This option allows the design example to be tested on a third party development kit with an Intel FPGA. You may need to set the pin assignments on your own.

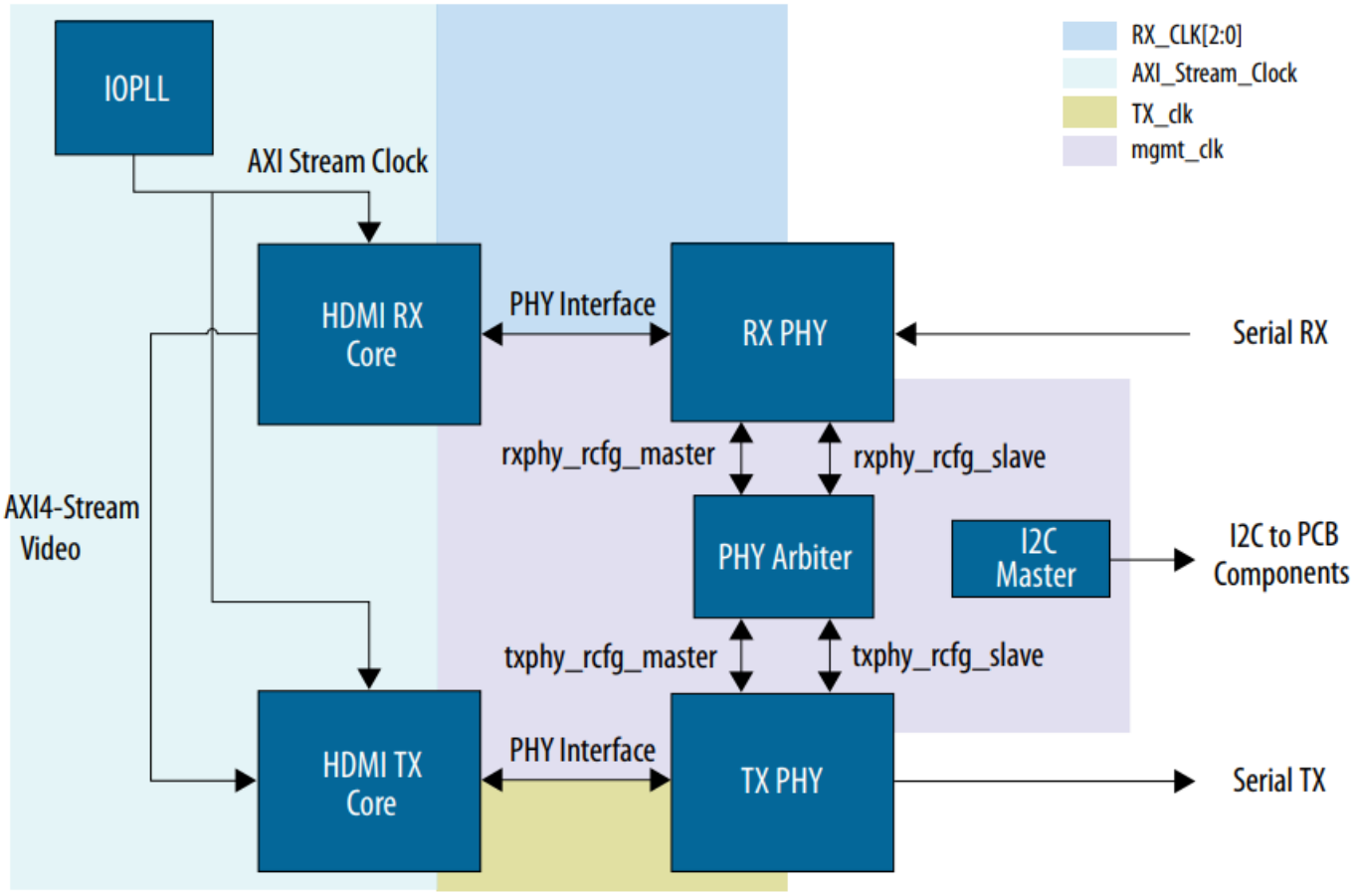
Target Device		
Change Target Device	On, Off	Turn on this option and select the preferred device variant for the development kit.

HDMI 2.0 PHY Design Example

The HDMI PHY Intel FPGA IP design example demonstrates one HDMI instance parallel loopback comprising three RX channels and four TX channels, operating at data rates up to 6 Gbps.

The generated HDMI PHY Intel FPGA IP design example is the same as the design example generated in the HDMI Intel FPGA IP core. However, this design example uses the new TX PHY, RX PHY, and PHY arbiter instead of custom RTL in the HDMI Intel FPGA IP core design example.

Figure 3. HDMI 2.0 PHY Design Example



Module	Description
RX PHY	The RX PHY recovers serial HDMI data and send this to the HDMI RX core in parallel format on the recovered clock domains (rx_clk[2:0]). The data is decoded into video

Module	Description
	data to be output via AXI4-stream video. The RX PHY also sends vid_clk and ls_clk signals to the HDMI RX core via the PHY interface.
HDMI TX Core	The HDMI TX core receives AXI4-stream video data a nd encodes this into HDMI format parallel data. The H DMI TX core sends this data to the TX PHY.
HDMI RX Core	The IP receives the serial data from the RX PHY and p erforms data alignment, channel deskew, TMDS decoding, auxiliary data decoding, video data decoding, audio data decoding, and descrambling.
TX PHY	Receives and serializes the parallel data from the HD MI TX core and outputs HDMI TMDS streams. The TX PHY produces tx_clk for the HDMI TX core. The TX P HY also generates vid_clk and ls_clk and sends these signals to the HDMI TX core via the PHY interface.
IOPLL	Generates 300 MHz AXI serial stream clock for the AX I4- stream interface.
I2C Master	To configure the various PCB components.

Hardware and Software Requirements

Intel uses the following hardware and software to test the design example.

Hardware

- Intel Arria 10 GX FPGA Development Kit

- HDMI Source (Graphics Processor Unit (GPU)
- HDMI Sink (Monitor)
- Bitec HDMI FMC 2.0 daughter card (Revision 11)
- HDMI cables

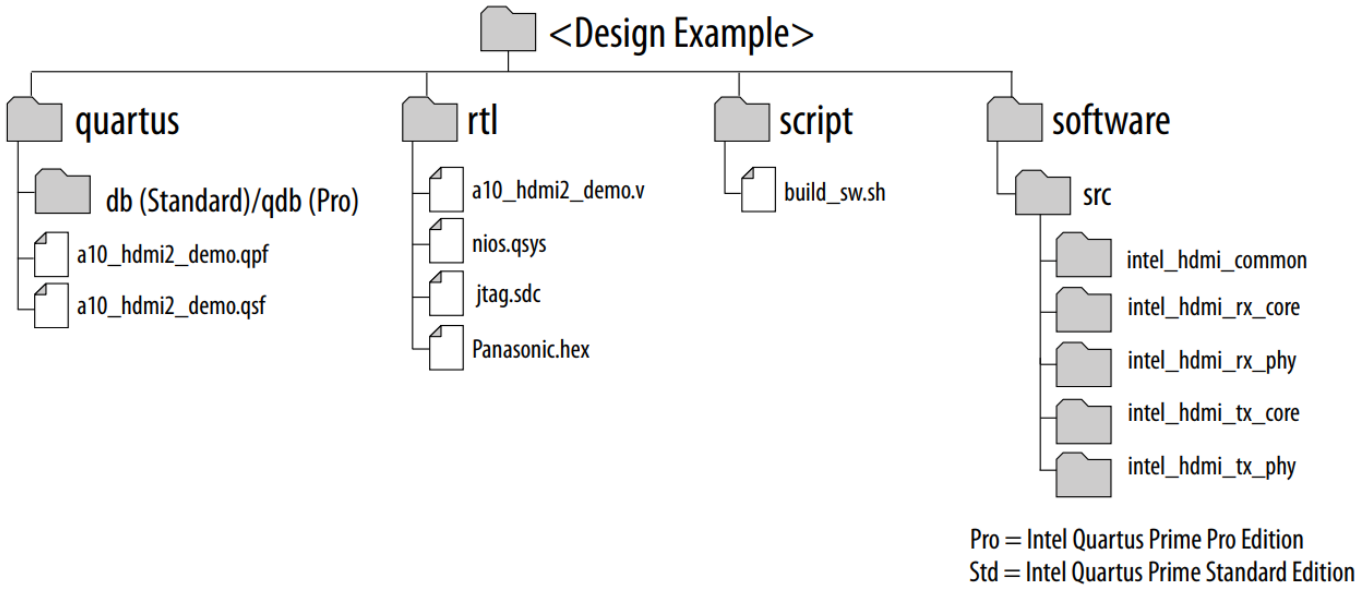
Software

- Intel Quartus Prime Pro Edition (for hardware testing)
- ModelSim* – Intel FPGA Edition, ModelSim – Intel FPGA Starter Edition, NCSim, Riviera-PRO*, VCS* (Verilog HDL only)/VCS MX, or Xcelium* Parallel simulator

Directory Structure

The directories contain the generated file for the HDMI Intel FPGA IP design example.

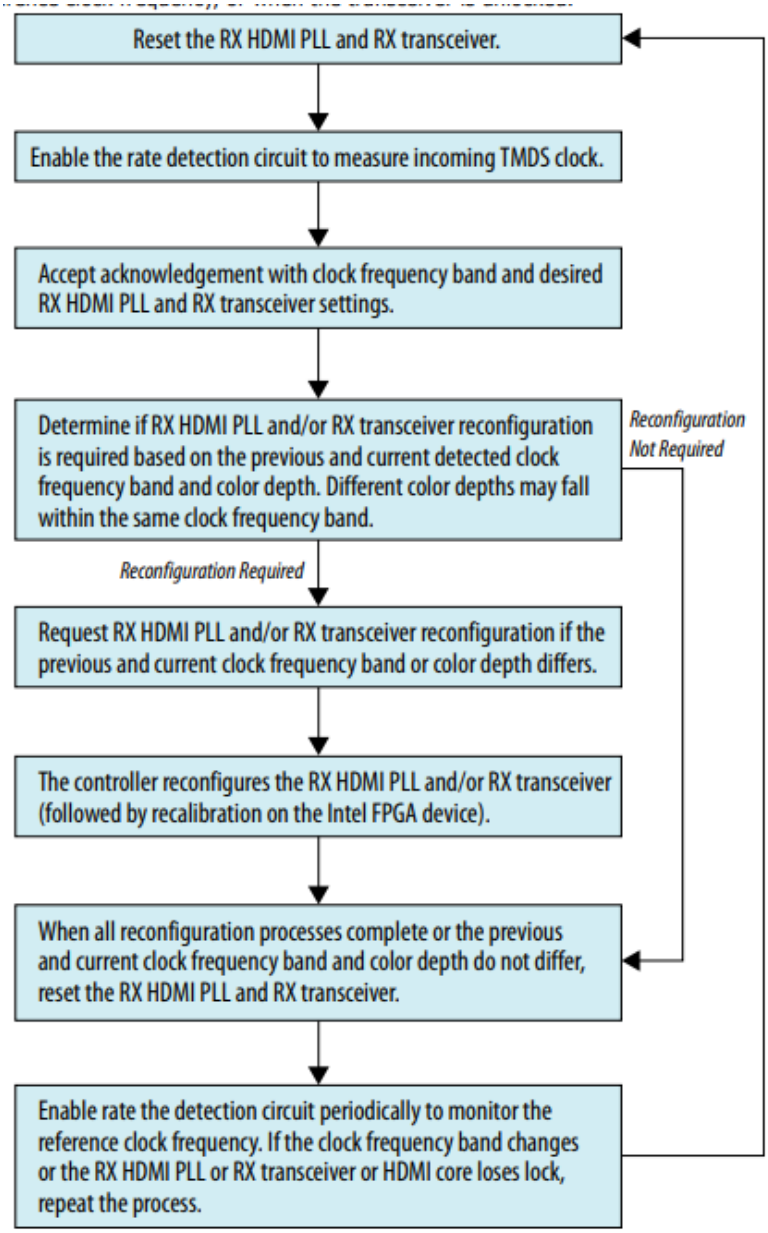
Figure 4. Directory Structure for the Design Example



Reconfiguration Sequence Flow

Figure 5. Multi-rate Reconfiguration Sequence Flow

The figure illustrates the multi-rate reconfiguration sequence flow of the controller when it receives input data stream and reference clock frequency, or when the transceiver is unlocked.



Interface Signals

The tables list the signals for the HDMI PHY Intel FPGA IP design example.

Table 3. Top-Level Signals

Signal	Direction	Width	Description
On-board Oscillator Signal			
clk_fpga_b3_p	Input	1	100 MHz free running clock for core reference clock
refclk_fmcb_p	Input	1	Fixed rate reference clock for power-up calibration of the transceiver. It is 625 MHz by default but can be of any frequency

User Push Buttons and LEDs			
cpu_resetn	Input	1	Global reset
user_led_g	Output	2	Green LED display

HDMI FMC Daughter Card Pins on FMC Port B			
fmcb_gbtclk_m2c_p_0	Input	1	HDMI RX TMDS clock
fmcb_dp_m2c_p	Input	3	HDMI RX red, green, and blue data channels • Bitec daughter card revision 11 — [0]: RX TMDS Channel 1 (Green) — [1]: RX TMDS Channel 2 (Red) — [2]: RX TMDS Channel 0 (Blue)

fmcb_dp_c2m_p	Output	4	HDMI TX clock, red, green, and blue d ata channels • Bitec daughter card revision 11 — [0]: TX TMDS Channel 2 (Red) — [1]: TX TMDS Channel 1 (Green) — [2]: TX TMDS Channel 0 (Blue) — [3]: TX TMDS Clock Channel
fmcb_la_rx_p_9	Input	1	HDMI RX +5V power detect
fmcb_la_rx_p_8	Input	1	HDMI RX hot plug detect
fmcb_la_rx_n_8	Input	1	HDMI RX I2C SDA for DDC and SCD C
fmcb_la_tx_p_10	Input	1	HDMI RX I2C SCL for DDC and SCD C
fmcb_la_tx_p_12	Input	1	HDMI TX hot plug detect
fmcb_la_tx_n_12	Input	1	HDMI I2C SDA for DDC and SCDC
fmcb_la_rx_p_10	Input	1	HDMI I2C SCL for DDC and SCDC

fmcb_la_tx_p_11	Input	1	HDMI I2C SDA for redriver control
fmcb_la_rx_n_9	Input	1	HDMI I2C SCL for redriver control

Clocking Scheme

The following is the clocking scheme of the HDMI PHY Intel FPGA IP design example:

- clk_fpga_b3_p is a 100 MHz fixed rate clock for running the NIOS processor and control functions. If the supplied frequency is correct, the user_led_g[1] toggles for every second.
- refclk_fmcb_p is a fixed rate reference clock for power-up calibration of the transceivers. It is 625 MHz by default but can be of any frequency.
- fmcb_gbtclk_m2c_p_0 is the TMDS clock for HDMI RX. This clock is also used to drive the HDMI TX transceivers. If the supplied frequency is 148.5 MHz, the user_led_g[0] toggles for every second.

Hardware Setup

The HDMI PHY Intel FPGA IP design example is HDMI 2.0b capable and performs a loop-through demonstration for a standard HDMI video stream.

To run the hardware test, connect an HDMI-enabled device such as a graphics card with HDMI interface to the HDMI RX connector on the Bitec HDMI 2.0 daughter card, which route the data to the transceiver RX block and HDMI RX.

1. The HDMI sink decodes the port into a standard video stream and sends it to the clock recovery core.
2. The HDMI RX core decodes the video, auxiliary, and audio data to be looped back via AXI4-stream interface to the HDMI TX core.
3. The HDMI source port of the FMC daughter card transmits the image to a monitor.
4. Press the cpu_resetn button once to perform system reset.

   Note: If you want to use another Intel FPGA development board, you must change the device assignments and the pin assignments. The transceiver analog setting is tested for the Intel Arria 10 FPGA development kit and Bitec HDMI 2.0 daughter card. You may modify the settings for your own board.

Document Revision History for the HDMI PHY Intel FPGA IP Design Example User Guide

Document Version	Intel Quartus Prime Version	IP Version	Changes
2022.07.20	22.2	1.0.0	Initial release.

Documents / Resources

	intel HDMI PHY FPGA IP Design Example [pdf] User Guide HDMI PHY FPGA IP Design Example, HDMI PHY, FPGA IP Design Example, HDMI PHY IP Design Example, FPGA IP Design Example, IP Design Example, 732781