



# intel GX Device Errata and Design Recommendations User Guide

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## intel GX Device Errata and Design Recommendations



## About this Document

This document provides information about known device issues affecting Intel® Arria® 10 GX/GT devices. It also offers design recommendations you should follow when using Intel Arria 10 GX/GT devices.

## Design Recommendations for Intel Arria 10 GX/GT Devices

The following section describes recommendations you should follow when using Intel Arria 10 GX/GT devices.

### Intel Arria 10 Device Lifetime Guidance

The table below describes the Intel Arria 10 product family lifetime guidance corresponding to VGA gain settings.

VGA Gain Setting	Device Lifetime Guidance for Continuous Operation <a href="#">(1)</a>	
	100°C T <sub>J</sub> (Years)	90°C T <sub>J</sub> (Years)
0	11.4	11.4
1	11.4	11.4
2	11.4	11.4
3	11.4	11.4
4	11.4	11.4
5	9.3	11.4
6	6.9	11.4
7	5.4	11.4

### Design Recommendation

If you are using VGA gain settings of 5, 6, or 7 and require an 11.4-year lifetime, Intel recommends either one of the following guidelines:

- Change the VGA gain setting to 4, and re-tune the link, or
- Limit the junction temperature T<sub>J</sub> to 90°C.

(1) Device lifetime recommendation calculation assumes the device is configured and the transceiver is always powered up (24 x 7 x 365).

### Device Errata for Intel Arria 10 GX/GT Devices

Issue	Affected Devices	Planned Fix
<a href="#">Automatic Lane Polarity Inversion for PCIe Hard IP</a> on page 6	All Intel Arria 10 GX/GT devices	No planned fix
<a href="#">Link Equalization Request Bit in the PCIe Hard IP Cannot Be Cleared by Software</a> on page 7	All Intel Arria 10 GX/GT devices	No planned fix
<a href="#">High VCCBAT Current when VCC is Powered Down</a> on page 8	All Intel Arria 10 GX/GT devices	No planned fix
<a href="#">Failure on Row Y59 When Using the Error Detection Cyclic Redundancy Check (EDCRC) or Partial Reconfiguration (PR)</a> on page 9	<ul style="list-style-type: none"> <li>Intel Arria 10 GX 160 devices</li> <li>Intel Arria 10 GX 220 devices</li> <li>Intel Arria 10 GX 270 devices</li> </ul>	No planned fix
	<ul style="list-style-type: none"> <li>Intel Arria 10 GX 320 devices</li> </ul>	
<a href="#">GPIO Output may not meet the On-Chip Series Termination (Rs OCT) without Calibration Resistance Tolerance Specification or Current Strength Expectation</a> on page 10	<ul style="list-style-type: none"> <li>Intel Arria 10 GX 160 devices</li> <li>Intel Arria 10 GX 220 devices</li> <li>Intel Arria 10 GX 270 devices</li> <li>Intel Arria 10 GX 320 devices</li> </ul>	No planned fix
	<ul style="list-style-type: none"> <li>Intel Arria 10 GX 480 devices</li> </ul>	
	<ul style="list-style-type: none"> <li>Intel Arria 10 GX 570 devices</li> </ul>	
	<ul style="list-style-type: none"> <li>Intel Arria 10 GX 660 devices</li> </ul>	

### Automatic Lane Polarity Inversion for PCIe Hard IP

For Intel Arria 10 PCIe Hard IP open systems where you do not control both ends of the PCIe link, Intel does not guarantee automatic lane polarity inversion with the Gen1x1 configuration, Configuration via Protocol (CvP), or Autonomous Hard IP mode. The link may not train successfully, or it may train to a smaller width than expected. There is no planned workaround or fix. For all other configurations, refer to the following workaround.

- **Workaround:** Refer to the Knowledge Database for details to workaround this issue.
- **Status:** Affects Intel Arria 10 GX/GT devices. Status: No planned fix.
- **Related Information:** Knowledge Database

### Link Equalization Request bit of the PCIe Hard IP

The Link Equalization Request bit (bit 5 of the Link Status 2 Register) is set during PCIe Gen3 link equalization. Once set, this bit cannot be cleared by software. The autonomous equalization mechanism is not affected by this issue, but the software equalization mechanism may be impacted depending on the usage of the Link Equalization Request bit.

- **Workaround**  
Avoid using software-based link equalization mechanism for both PCIe endpoint and root port implementations.
- **Status**

- **Affects:** Intel Arria 10 GX/GT devices.
- **Status:** No planned fix.

#### High VCCBAT Current when VCC is Powered Down

If you power off VCC when VCCBAT remains powered on, VCCBAT may draw higher current than expected. If you use the battery to maintain volatile security keys when the system is not powered up, VCCBAT current could be up to 120  $\mu$ A, resulting in shortened battery life.

#### Workaround

Contact your battery provider to evaluate the impact to the retention period of the battery used on your board. There is no impact if you connect the VCCBAT to the on-board power rail.

#### • Status

- Affects: Intel Arria 10 GX/GT devices
- Status: No planned fix.

#### Failure on Row Y59 When Using the Error Detection Cyclic Redundancy Check (EDCRC) or Partial Reconfiguration (PR)

When the error detection cyclic redundancy check (EDCRC) or partial reconfiguration (PR) feature is enabled, you may encounter unexpected output from clocked components such as flip-flop or DSP or M20K or LUTRAM that are placed at row 59 in Intel Arria 10 GX devices.

This failure is sensitive to temperature and voltage.

Intel Quartus® Prime software version 18.1.1 and later displays the following error message:

- In Intel Quartus Prime Standard Edition:
  - Info (20411): EDCRC usage detected. To ensure reliable operation of these features on the targeted device, certain device resources must be disabled.
  - Error (20412): You must create a floorplan assignment to block out the device resources at row Y=59 and ensure reliable operation with EDCRC. Use the Logic Lock (Standard) Regions Window to create an empty reserved region with origin X0\_Y59, height = 1 and width = <#>. Also, review any existing Logic Lock (Standard) regions that overlap that row and ensure if they account for the unused device resources.
- In Intel Quartus Prime Pro Edition:
  - Info (20411): PR and/or EDCRC usage detected. To ensure reliable operation of these features on the targeted device, certain device resources must be disabled.
  - Error (20412): You must create a floorplan assignment to block out the device resources at row Y=59 and ensure reliable operation with PR and/or EDCRC. Use the Logic Lock Regions Window to create an empty reserved region, or add set\_instance\_assignment -name EMPTY\_PLACE\_REGION "X0 Y59 X<#> Y59-R:C-empty\_region" -to | directly to your Quartus Settings File (.qsf). Also, review any existing Logic Lock regions that overlap that row and ensure if they account for the unused device resources.

#### Note:

Intel Quartus Prime software versions 18.1 and earlier do not report these errors.

**Workaround**

Apply the empty logic lock region instance in the Quartus Prime Settings File (.qsf) to avoid use of row Y59. For more information, refer to the corresponding knowledge base.

**Status**

Affects:

- Intel Arria 10 GX 160 devices
- Intel Arria 10 GX 220 devices
- Intel Arria 10 GX 270 devices
- Intel Arria 10 GX 320 devices

Status: No planned fix.

**GPIO Output may not meet the On-Chip Series Termination (Rs OCT) without Calibration Resistance Tolerance Specification or Current Strength Expectation****Description**

The GPIO pull-up impedance may not meet the on-chip series termination (Rs OCT) without calibration resistance tolerance specification mentioned in the Intel Arria 10 device datasheet. While using the current strength selection, the GPIO output buffer may not meet expected current strength at VOH voltage level when driving HIGH.

**Workaround**

Enable the on-chip series termination (Rs OCT) with calibration in your design.

**Status**

Affects:

- Intel Arria 10 GX 160 devices
- Intel Arria 10 GX 220 devices
- Intel Arria 10 GX 270 devices
- Intel Arria 10 GX 320 devices
- Intel Arria 10 GX 480 devices
- Intel Arria 10 GX 570 devices
- Intel Arria 10 GX 660 devices

Status: No planned fix.

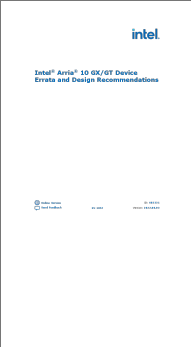
**Document Revision History for Intel Arria 10 GX/GT Device Errata and Design Recommendations**

Document Version	Changes
2022.08.03	Added a new erratum: <i>GPIO Output may not meet the On-Chip Series Termination (Rs OCT) without Calibration Resistance Tolerance Specification or Current Strength Expectation.</i>
2020.01.10	Added a new erratum: <i>Failure on Row Y59 When Using the Error Detection Cyclic Redundancy Check (EDCRC) or Partial Reconfiguration (PR).</i>
2019.12.23	Added a new erratum: <i>Link Equalization Request Bit in the PCIe Hard IP Cannot Be Cleared by Software.</i>
2017.12.20	Added a new erratum: <i>High V<sub>CCBAT</sub> Current when V<sub>CC</sub> is Powered Down.</i>
2017.07.28	Initial release.

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## Documents / Resources

	<a href="#">intel GX Device Errata and Design Recommendations</a> [pdf] User Guide GX, GT, GX Device Errata and Design Recommendations, Device Errata and Design Recommendations, Errata and Design Recommendations, Design Recommendations, Recommendations
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## References

- [intel Why does my Arria 10 PCIe Hard IP link width downtrain?](#)
- [intel FPGA Knowledge Base Articles Search](#)
- [intel 1. About this Document](#)
- [intel Intel ISO 9001:2015 Registrations](#)