intel F-Tile DisplayPort FPGA IP Design Example User Guide

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Contents

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Updated for Intel® Quartus® Prime Design Suite: 22.2 IP Version: 21.0.1

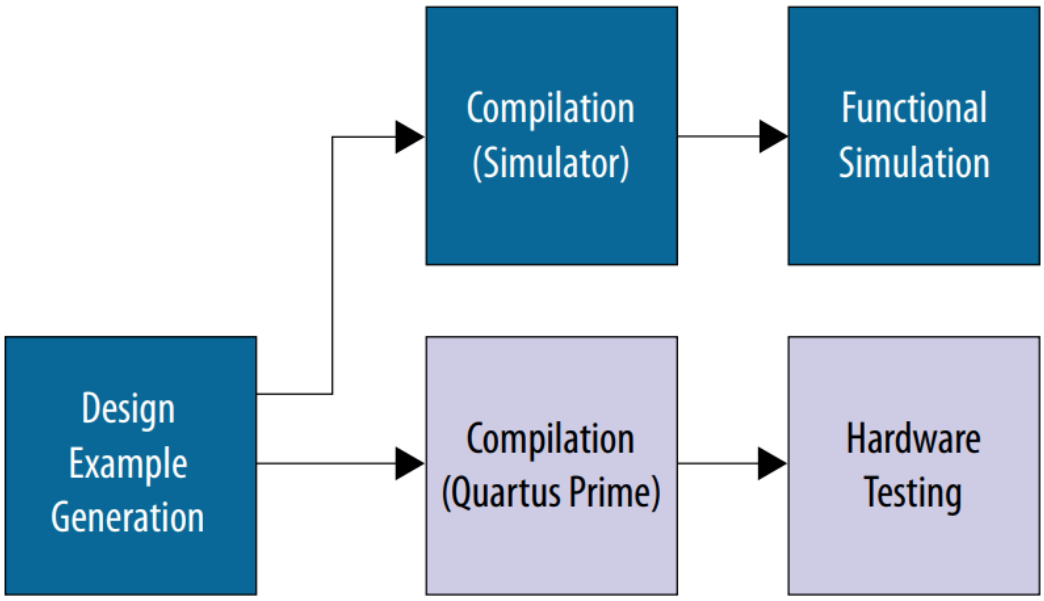
DisplayPort Intel FPGA IP Design Example Quick Start Guide

The DisplayPort Intel® F-tile devices feature a simulating testbench and a hardware design that supports compilation and hardware testing FPGA IP design examples for Intel Agilex™
The DisplayPort Intel FPGA IP offers the following design examples:

- DisplayPort SST parallel loopback without a Pixel Clock Recovery (PCR) module
- DisplayPort SST parallel loopback with AXIS Video Interface

When you generate a design example, the parameter editor automatically creates the files necessary to simulate, compile, and test the design in hardware.

Figure 1. Development Stages



Related Information

- DisplayPort Intel FPGA IP User Guide
- Migrating to Intel Quartus Prime Pro Edition

1.1. Directory Structure

Figure 2. Directory Structure

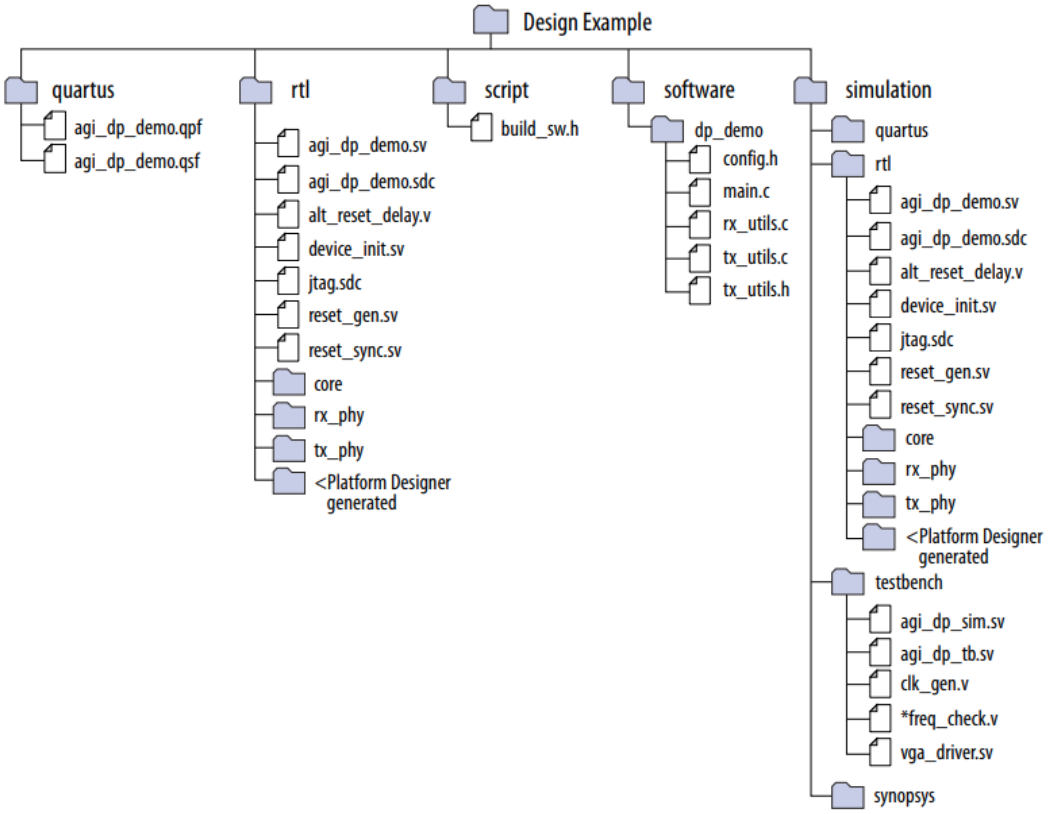


Table 1. Design Example Components

Folders	Files
rtl/core	dp_core.ip
	dp_rx . ip
	dp_tx . ip
rtl/rx_phy	dp_gxb_rx/ ((DP PMA UX building block)
	dp_rx_data_fifo . ip
	rx_top_phy . sv
rtl/tx_phy	dp_gxb_rx/ ((DP PMA UX building block)
	dp_tx_data_fifo.ip
	dp_tx_data_fifo.ip

1.2. Hardware and Software Requirements

Intel uses the following hardware and software to test the design example:

Hardware

- Intel Agilex I-Series Development Kit
- DisplayPort Source GPU
- DisplayPort Sink (Monitor)
- Bitec DisplayPort FMC daughter card Revision 8C
- DisplayPort cables

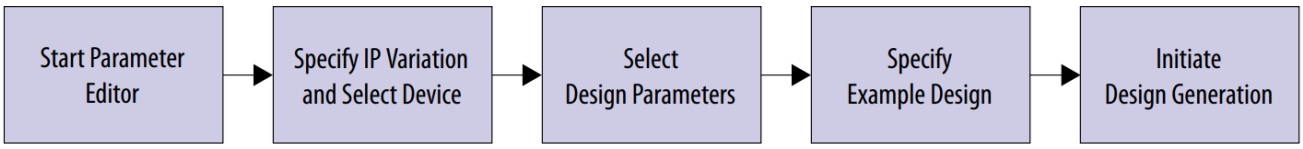
Software

- Intel Quartus® Prime
- Synopsys* VCS Simulator

1.3. Generating the Design

Use the DisplayPort Intel FPGA IP parameter editor in Intel Quartus Prime software to generate the design example.

Figure 3. Generating the Design Flow

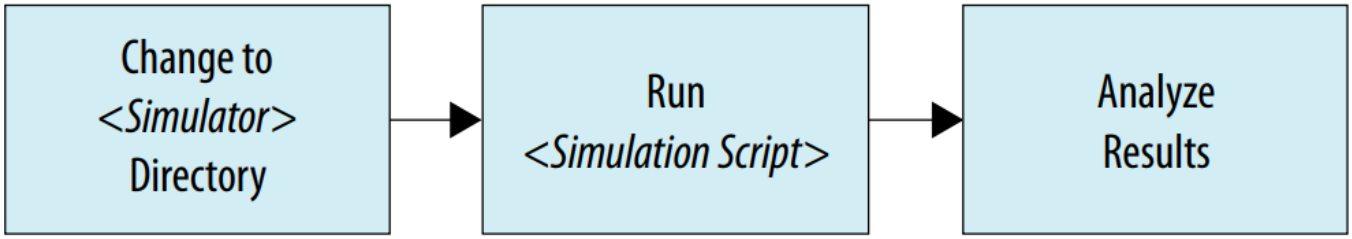


1. Select Tools ➤ IP Catalog, and select Intel Agilex F-tile as the target device family.
   Note: The design example only supports Intel Agilex F-tile devices.
2. In the IP Catalog, locate and double-click DisplayPort Intel FPGA IP. The New IP Variation window appears.
3. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file named <your_ip>.ip.
4. Select an Intel Agilex F-tile device in the Device field, or keep the default Intel Quartus Prime software device selection.
5. Click OK. The parameter editor appears.
6. Configure the desired parameters for both TX and RX.
7. Under the Design Example tab, select DisplayPort SST Parallel Loopback Without PCR.
8. Select Simulation to generate the testbench, and select Synthesis to generate the hardware design example. You must select at least one of these options to generate the design example files. If you select both, the generation time becomes longer.
9. For Target Development Kit, select Intel Agilex I-Series SOC Development Kit. This causes the target device selected in step 4 to change to match the device on the development kit. For Intel Agilex I-Series SOC Development Kit, the default device is AGIB027R31B1E2VR0.
10. Click Generate Example Design.

1.4. Simulating the Design

The DisplayPort Intel FPGA IP design example testbench simulates a serial loopback design from a TX instance to an RX instance. An internal video pattern generator module drives the DisplayPort TX instance and the RX instance video output connects to CRC checkers in the testbench.

Figure 4. Design Simulation Flow



1. Go to Synopsys simulator folder and select VCS.
2. Run simulation script.
   Source vcs_sim.sh

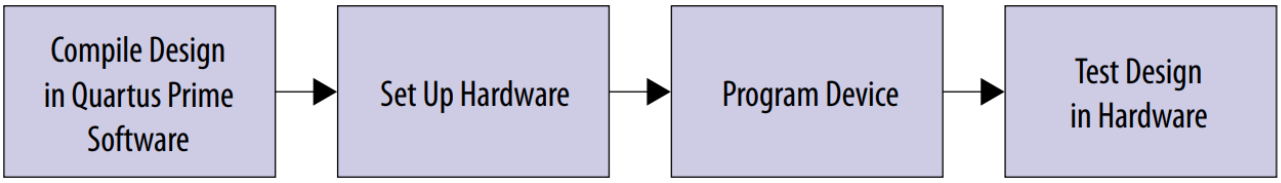
3. The script performs Quartus TLG, compiles and run the testbench in the simulator.
4. Analyze the result.

   A successful simulation ends with Source and Sink SRC comparison.

```
# SINK CRC_R = ac9c, CRC_G = ac9c, CRC_B = ac9c,
# SOURCE CRC_R = ac9c, CRC_G = ac9c, CRC_B = ac9c,
# Pass: Test Completed
```

1.5. Compiling and Testing the Design

Figure 5. Compiling and Simulating the Design



To compile and run a demonstration test on the hardware example design, follow these steps:

1. Ensure hardware example design generation is complete.
2. Launch the Intel Quartus Prime Pro Edition software and open <project>/ quartus/agi_dp_demo.qpf.
3. Click Processing ➤ Start Compilation.
4. After successful compilation, the Intel Quartus Prime Pro Edition software generates a .sof file in your specified directory.
5. Connect the DisplayPort RX connector on the Bitec daughter card to an external DisplayPort source, such as the graphics card on a PC.
6. Connect the DisplayPort TX connector on the Bitec daughter card to a DisplayPort sink device, such as a video analyzer or a PC monitor.
7. Ensure all switches on the development board are in default position.
8. Configure the selected Intel Agilex F-Tile device on the development board using the generated .sof file (Tools ➤ Programmer).
9. The DisplayPort sink device displays the video generated from the video source.

Related Information

Intel Agilex I-Series FPGA Development Kit User Guide/

1.5.1. Regenerating ELF File

By default, the ELF file is generated when you generate the dynamic design example.

However, in some cases, you need to regenerate the ELF file if you modify the software file or regenerate the dp_core.qsys file. Regenerating the dp_core.qsys file updates the .sopcinfo file, which requires you to regenerate the ELF file.

1. Go to <project directory>/software and edit the code if necessary.
2. Go to <project directory>/script and execute the following build script: source build_sw.sh

   • On Windows, search and open Nios II Command Shell. In the Nios II Command Shell, go to <project directory>/script and execute source build_sw.sh.

   Note: To execute build script on Windows 10, your system requires Windows Subsystems for Linux (WSL). For more information about WSL installation steps, refer to the Nios II Software Developer Handbook.

   • On Linux, launch the Platform Designer, and open Tools ➤ Nios II Command Shell. In the Nios II Command Shell, go to <project directory>/script and execute source build_sw.sh.
3. Make sure an .elf file is generated in <project directory>/software/ dp_demo.

4. Download the generated .elf file into the FPGA without recompiling the .sof file by running the following script:
   nios2-download <project directory>/software/dp_demo/*.elf
5. Push the reset button on the FPGA board for the new software to take effect.

1.6. DisplayPort Intel FPGA IP Design Example Parameters

Table 2. DisplayPort Intel FPGA IP Design Example QSF constraint for Intel Agilex Ftile Device

QSF Constraint	Description
set_global_assignment -name VERILOG_MACRO "__DISPLAYPORT_support__=1"	From Quartus 22.2 onwards, this QSF constraint is needed to enable DisplayPort custom SRC (Soft Reset Controller) flow

Table 3. DisplayPort Intel FPGA IP Design Example Parameters for Intel Agilex F-tile Device

Parameter	Value	Description
Available Design Example		
Select Design	•None •DisplayPort SST Parallel Loopback without PCR •DisplayPort SST Parallel Loopback with AXIS Video Interface	Select the design example to be generated. •None: No design example is available for the current parameter selection. •DisplayPort SST Parallel Loopback without PCR: This design example demonstrates parallel loopback from DisplayPort sink to DisplayPort source without a Pixel Clock Recovery (PCR) module when you turn on the Enable Video Input Image Port parameter. •DisplayPort SST Parallel Loopback with AXIS Video Interface: This design example demonstrates parallel loopback from DisplayPort sink to DisplayPort source with AXIS Video interface when Enable Active Video Data Protocols is set to AXIS-VVP Full.
Design Example Files		
Simulation	On, Off	Turn on this option to generate the necessary files for the simulation testbench.
Synthesis	On, Off	Turn on this option to generate the necessary files for Intel Quartus Prime compilation and hardware design.
Generated HDL Format		
Generate File Format	Verilog, VHDL	Select your preferred HDL format for the generated design example fileset. Note: This option only determines the format for the generated top level IP files. All other files (e.g. example testbenches and top level files for hardware demonstration) are in Verilog HDL format.
Target Development Kit		
Select Board	•No Development Kit •Intel Agilex I-Series Development Kit	Select the board for the targeted design example.

Parameter	Value	Description
		•No Development Kit: This option excludes all hardware aspects for the design example. The P core sets all pin assignments to virtual pins. •Intel Agilex I-Series FPGA Development Kit: This option automatically selects the project's target device to match the device on this development kit. You may change the target device using the Change Target Device parameter if your board revision has a different device variant. The IP core sets all pin assignments according to the development kit. Note: Preliminary Design Example is not functionally verified on hardware in this Quartus release. •Custom Development Kit: This option allows the design example to be tested on a third-party development kit with an Intel FPGA. You may need to set the pin assignments on your own.
Target Device		
Change Target Device	On, Off	Turn on this option and select the preferred device variant for the development kit.

Parallel Loopback Design Examples

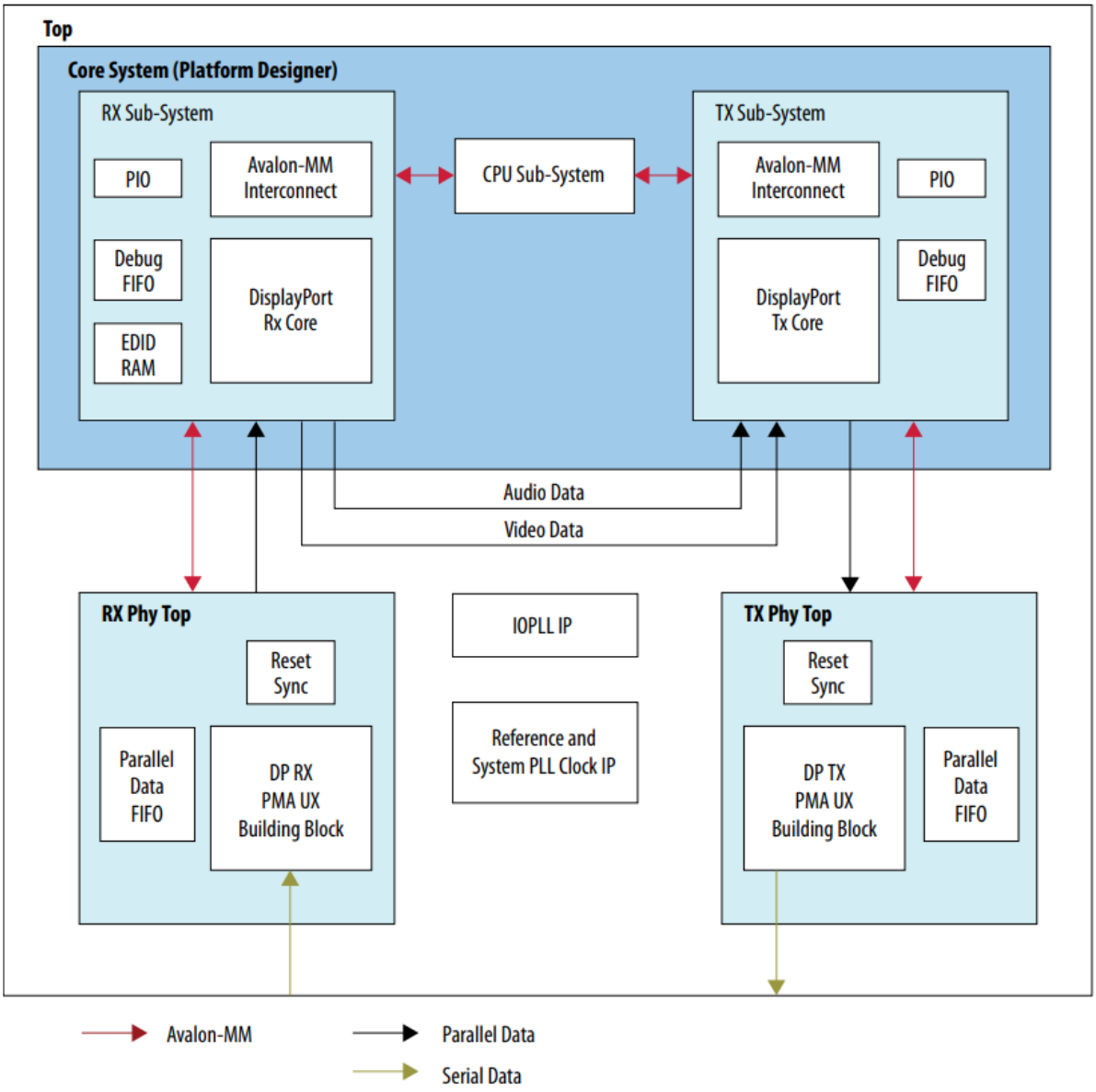
The DisplayPort Intel FPGA IP design examples demonstrate parallel loopback from DisplayPort RX instance to DisplayPort TX instance without a Pixel Clock Recovery (PCR) module.
Table 4. DisplayPort Intel FPGA IP Design Example for Intel Agilex F-tile Device

Design Example	Designation	Data Rate	Channel Mode	Loopback Type
DisplayPort SST parallel loopback without PCR	DisplayPort SST	RBR, HRB, HRB2, HBR3	Simplex	Parallel without PCR
DisplayPort SST parallel loopback with AXIS Video Interface	DisplayPort SST	RBR, HRB, HRB2, HBR3	Simplex	Parallel with AXIS Video Interface

2.1. Intel Agilex F-tile DisplayPort SST Parallel Loopback Design Features

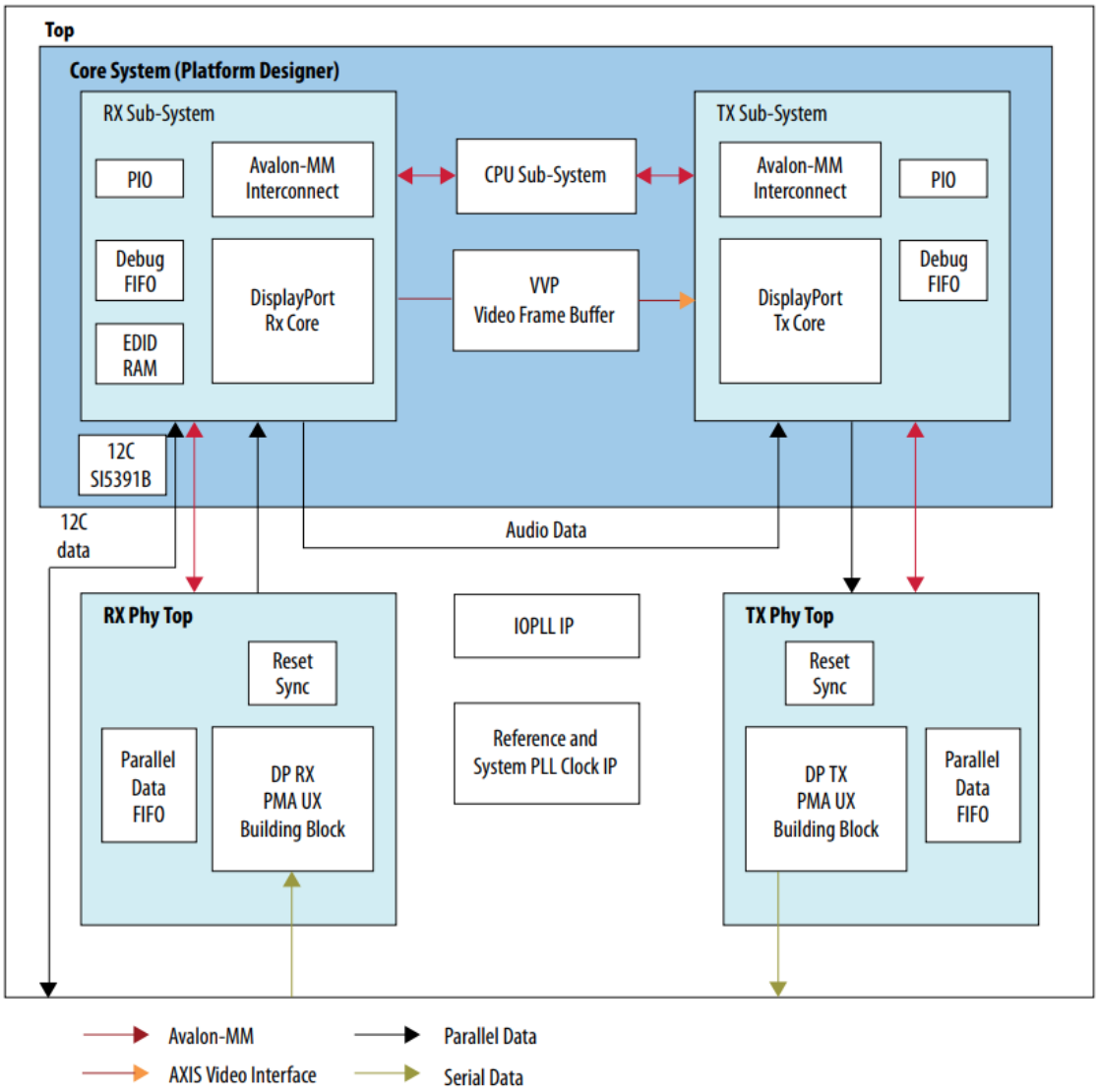
The SST parallel loopback design examples demonstrate the transmission of a single video stream from DisplayPort sink to DisplayPort source.

Figure 6. Intel Agilex F-tile DisplayPort SST Parallel Loopback without PCR



- In this variant, the DisplayPort source's parameter, TX_SUPPORT_IM_ENABLE, is turned on and the video image interface is used.
- The DisplayPort sink receives video and or audio streaming from external video source such as GPU and decodes it into parallel video interface.
- The DisplayPort sink video output directly drives the DisplayPort source video interface and encodes to the DisplayPort main link before transmitting to the monitor.
- The IOPLL drives both the DisplayPort sink and source video clocks at a fixed frequency.
- If DisplayPort sink and source's MAX_LINK_RATE parameter is configured to HBR3 and PIXELS_PER_CLOCK is configured to Quad, the video clock runs at 300 MHz to support 8Kp30 pixel rate (1188/4 = 297 MHz).

Figure 7. Intel Agilex F-tile DisplayPort SST Parallel Loopback with AXIS Video Interface



- In this variant, the DisplayPort source and sink parameter, select AXIS-VVP FULL in ENABLE ACTIVE VIDEO DATA PROTOCOLS to enable Axis Video Data Interface.
- The DisplayPort sink receives video and or audio streaming from external video source such as GPU and decodes it into parallel video interface.
- The DisplayPort Sink converts video data stream into axis video data and drives the DisplayPort source axis video data interface through VVP Video Frame Buffer. DisplayPort Source converts axis video data into DisplayPort main link before transmitting to the monitor.
- In this design variant, there are three main video clocks, namely rx/tx_axi4s_clk, rx_vid_clk, and tx_vid_clk. axi4s_clk runs at 300 MHz for both AXIS modules in Source and Sink. rx_vid_clk runsDP Sink Video pipeline at 300 MHz (to support any resolution up to 8Kp30 4PIPs), while tx_vid_clk runs DP Source Video pipeline at the actual Pixel Clock frequency (divided by PIPs).
- This design variant auto configures the tx_vid_clk frequency through I2C programming to on-board SI5391B OSC when the design detects a switch in the resolution.
- This design variant only demonstrates a fixed number of resolutions as predefined in the DisplayPort software, namely:
  — 720p60, RGB
  — 1080p60, RGB
  — 4K30, RGB
  — 4K60, RGB

2.2. Clocking Scheme

The clocking scheme illustrates the clock domains in the DisplayPort Intel FPGA IP design example.

Figure 8. Intel Agilex F-tile DisplayPort Transceiver clocking scheme

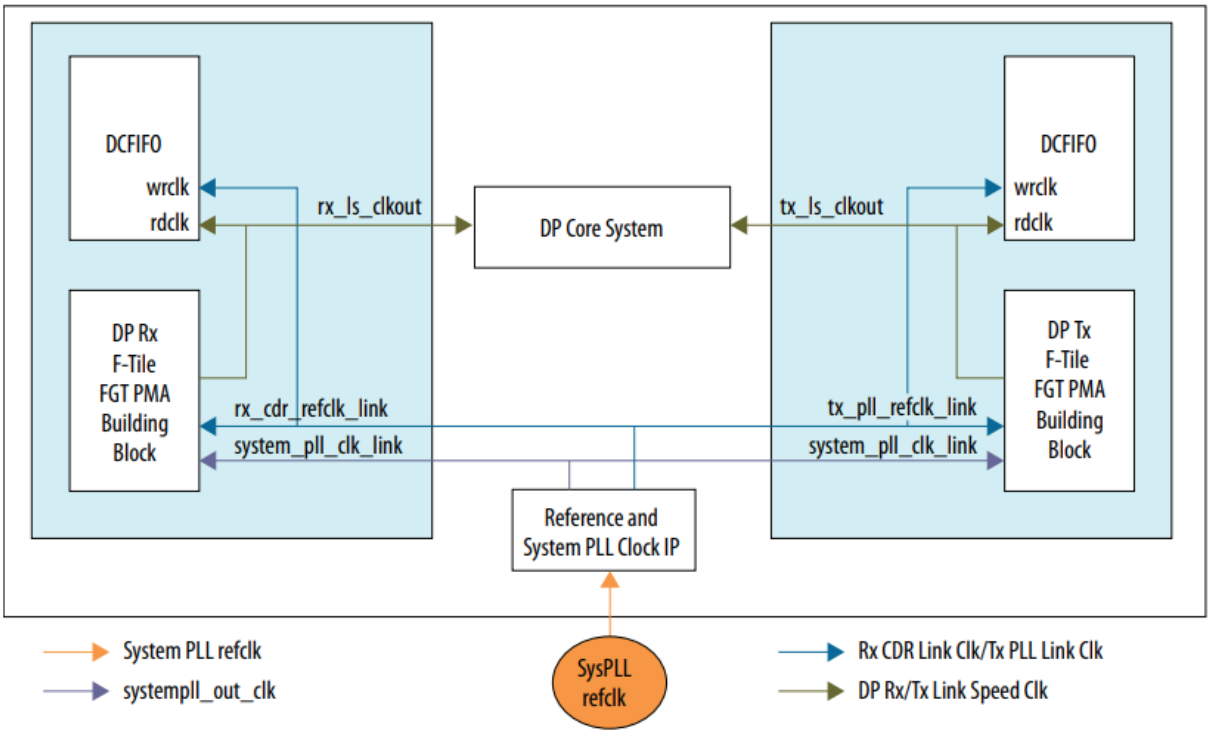


Table 5. Clocking Scheme Signals

Clock in diagram	Description
SysPLL refclk	F-tile System PLL reference clock which can be any clock frequency that is divi dable by System PLL for that output frequency. In this design example, system_pll_clk_link and rx/tx refclk_link share the sam e 150 MHz SysPLL refclk.

Clock in diagram	Description
	It must be a free running clock which is connected from a dedicated transceiver reference clock pin to the input clock port of Reference and System PLL Clocks IP, before connecting the corresponding output port to DisplayPort Phy Top. Note: For this design example, configure Clock Controller GUI Si5391A OUT6 to 150 MHz.
system pll clk link	The minimum System PLL output frequency to support all DisplayPort rate is 320 MHz. This design example uses a 900 MHz (highest) output frequency so that SysPLL refclk can be shared with rx/tx refclk_link which is 150 MHz.
rx_cdr_refclk_link / tx_pll_refclk_link	Rx CDR and Tx PLL Link refclk which fixed to 150 MHz to support all DisplayPort data rate.
rx_ls_clkout / tx_ls_clkout	DisplayPort Link Speed Clock to clock DisplayPort IP core. Frequency equivalent to Data Rate divide by parallel data width. Example: Frequency = data rate / data width = 8.1G (HBR3) / 40 bits = 202.5 MHz

2.3. Simulation Testbench

The simulation testbench simulates the DisplayPort TX serial loopback to RX.

Figure 9. DisplayPort Intel FPGA IP Simplex Mode Simulation Testbench Block Diagram

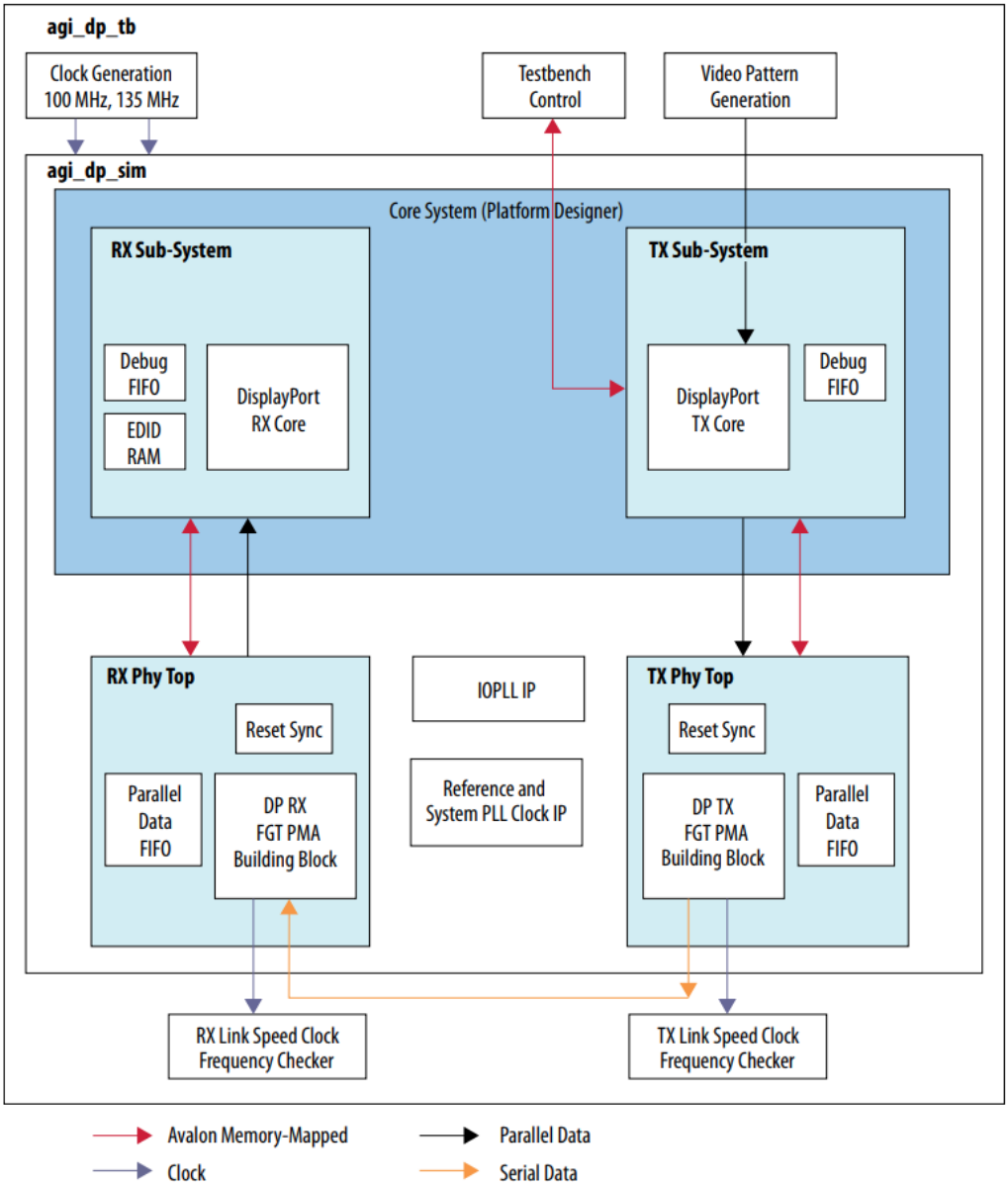


Table 6. Testbench Components

Component	Description
Video Pattern Generator	This generator produces color bar patterns that you can configure. You c an parameterize the video format timing.
Testbench Control	This block controls the test sequence of the simulation and generates the necessary stimulus signals to the TX core. The testbench control block al so reads the CRC value from both source and sink to make comparisons.
RX Link Speed Clock Frequency C hecker	This checker verifies if the RX transceiver recovered clock frequency mat ches the desired data rate.
TX Link Speed Clock Frequency Ch ecker	This checker verifies if the TX transceiver recovered clock frequency mat ches the desired data rate.

The simulation testbench does the following verifications:

Table 7. Testbench Verifications

Test Criteria	Verification
• Link Training at Data Rate HBR3 • Read the DPCD registers to check if the DP St atus sets and measures both TX and RX Link Sp eed frequency.	Integrates Frequency Checker to measure the Link Speed clock's frequency output from the TX and RX transceiver.
• Run video pattern from TX to RX. • Verify the CRC for both source and sink to chec k if they match	• Connects video pattern generator to the DisplayPort Sourc e to generate the video pattern. • Testbench control next reads out both Source and Sink CR C from DPTX and DPRX registers and compares to ensure both CRC values are identical. Note: To ensure CRC is calculated, you must enable the Su pport CTS test automation parameter.

Document Revision History for F-Tile DisplayPort Intel FPGA IP Design Example User Guide

Document Version	Intel Quartus Prime Version	IP Version	Changes
2022.09.02	22.	20.0.1	•Changed document title from DisplayPort Intel A gilex F-Tile FPGA IP Design Example User Guide to F-Tile DisplayPort Intel FPGA IP Design Example User Guide. •Enabled AXIS Video Design Example variant. •Removed Static Rate design and replaced it with Multi Rate Design Example. •Removed the note in the DisplayPort Intel FPGA IP Design Example Quick Start Guide that says I ntel Quartus Prime 21.4 software version only su pports Preliminary Design Examples. •Replaced the Directory Structure figure with the correct figure. •Added a section Regenerating ELF File under C ompiling and Testing the Design. •Updated the Hardware and Software Requireme nts section to include additional hardware requirements.
2021.12.13	21.	20.0.0	Initial release.

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