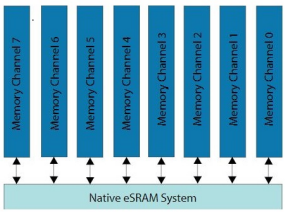

eSRAM Intel FPGA IP User Guide

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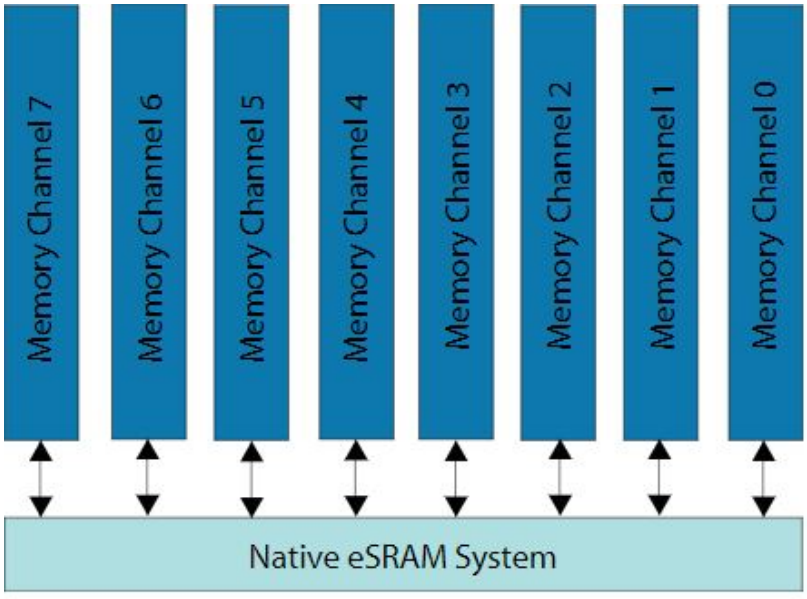

Product Information

The product is the Intel FPGA IP, which is compatible with the Intel Quartus Prime Design Suite software. The IP has different versions that match the software versions until v19.1. Starting from software version 19.2, a new versioning scheme is introduced for the Intel FPGA IP.

The IP versions are as follows:

Version	Date	Intel Quartus Prime Version	Description	Impact
v20.1.0	2022.09.26	22.3	Enabled Intel AgilexTM eSRAM IP system component connection support in Platform Designer tool.	ISO 9001:2015 Registered
v20.0.0	2021.10.04	21.3	Updated the ch{0-7}_ecc_dec_eccmode and ch{0-7}_ecc_enc_eccmode parameters to ECC_DISABLED for unused ports.	IP upgrade is required to obtain the design pass compilation with Intel Quartus Prime Pro Edition software version 21.3.
v19.2.1	2021.06.29	21.2	Fixed the hold violation by adding (* altera_attribute = -name HYPER_REGISTER_DELAY_CHAIN 100 *) to the eSRAM Intel Agilex FPGA IP.	The change is optional. An IP upgrade is required if your IP cannot meet the maximum performance specification due to a hold violation.
v19.2.0	2020.12.14	19.4	Removed the dynamic ECC encoder and decoder — bypass feature.	N/A
v19.1.1	2019.07.01	19.2	Initial release for Intel Agilex devices.	N/A

If a release note is not available for a specific IP version, it means there are no changes in that version.

Note: The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version.

Product Usage Instructions

To use the Intel FPGA IP, follow these steps:

1. Ensure you have the compatible Intel Quartus Prime Design Suite software installed on your system.
2. Download the corresponding Intel FPGA IP version that matches your software version.
3. Extract the downloaded IP files to a suitable location on your computer.
4. Open the Intel Quartus Prime software and create a new project or open an existing project.
5. In the project settings or IP catalog, locate and add the Intel FPGA IP to your project.
6. Configure the IP parameters according to your requirements.
7. Connect the IP to other components or modules in your design using the Platform Designer tool.
8. Ensure any necessary IP upgrades are performed if specified in the product information.
9. Compile and verify your design using the Intel Quartus Prime software.
10. Proceed with further steps as per your design requirements and project goals.

eSRAM Intel® Agilex™ FPGA IP

Release Notes
If a release note is not available for a specific IP version, the IP has no changes in that version. For information on

IP update releases up to v18.1, refer to the Intel® Quartus® Prime Design Suite Update Release Notes.
Intel FPGA IP versions match the Intel Quartus Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.
The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version.

A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Intel Agilex™ Embedded Memory User Guide
- Errata for the eSRAM Intel Agilex™ FPGA IP in the Knowledge Base

eSRAM Intel Agilex™ FPGA IP v20.1.0

Table 1. v20.1.0 2022.09.26

Intel Quartus Prime Version	Description	Impact
22.3	Enabled Intel Agilex™ eSRAM IP system component connection support in Platform Designer tool.	IP upgrade is optional in Intel Quartus Prime Pro Edition software version 22.3. • IP regeneration is only required if customers want to use eSRAM IP in the Platform Designer tool. • There are no changes to the existing eSRAM features.

eSRAM Intel Agilex FPGA IP v20.0.0

Table 2. v20.0.0 2021.10.04

Intel Quartus Prime Version	Description	Impact
21.3	Updated the ch{0-7}_ecc_dec_eccmode and ch{0-7}_ecc_enc_eccmode parameters to ECC_DISABLED for unused ports.	IP upgrade is required to obtain the design pass compilation with Intel Quartus Prime Pro Edition software version 21.3.

eSRAM Intel Agilex FPGA IP v19.2.1

Table 3. v19.2.1 2021.06.29

Intel Quartus Prime Version	Description	Impact
21.2	Fixed the hold violation by adding (* altera_attribute = “-name HYPER_REGISTER_DELAY_CHAIN 100″*) to the eSRAM Intel Agilex FPGA IP.	The change is optional. You are required to perform an IP upgrade if your IP cannot meet the maximum performance specification due to a hold violation.

eSRAM Intel Agilex FPGA IP v19.2.0

Table 4. v19.2.0 2020.12.14

Intel Quartus Prime Version	Description	Impact
19.4	Removed the dynamic ECC encoder and decoder bypass feature.	—

eSRAM Intel Agilex FPGA IP v19.1.1

Table 5. v19.1.1 2019.07.01

Intel Quartus Prime Version	Description	Impact
19.2	Initial release for Intel Agilex devices.	—

eSRAM Intel FPGA IP Release Notes (Intel Stratix® 10 Devices)

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the Intel Quartus Prime Design Suite Update Release Notes.

Intel FPGA IP versions match the Intel Quartus Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.

The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Intel Stratix® 10 Embedded Memory User Guide
- Errata for the eSRAM Intel FPGA IP in the Knowledge Base

eSRAM Intel FPGA IP v19.2.0

Table 6. v19.2.0 2022.09.26

Intel Quartus Prime Version	Description	Impact
22.3	Enabled Intel Stratix® 10 eSRAM IP system component connection support in Platform Designer tool.	IP upgrade is optional in Intel Quartus Prime Pro Edition software version 22.3. • IP regeneration is only required if customers want to use eSRAM IP in the Platform Designer tool. • There are no changes to the existing eSRAM features.

eSRAM Intel FPGA IP v19.1.5

Table 7. v19.1.5 2020.10.12

Intel Quartus Prime Version	Description	Impact
20.3	Updated the description for **Enable Low Power Mode** in the eSRAM Intel FPGA IP parameter editor.	—

eSRAM Intel FPGA IP v19.1.4

Table 8. v19.1.4 2020.08.03

Intel Quartus Prime Version	Description	Impact
20.2	Renamed the I/O PLL filename to waive the warning message from the IOPLL file. If the two eSRAMs have the same PLL parameters (PLL reference clock frequency and PLL desired clock frequency), the warning message can be ignored. If the two eSRAMs have different PLL parameters, after compilation they will be set to the same PLL frequencies taken from one of the eSRAM Intel FPGA IP parameters. Refer to the **Quartus Fitter report ➤ Plan Stage ➤ PLL Usage Summary** to observe the implemented eSRAM IOPLL frequencies. IP update is needed when the PLL parameter for both eSRAM is different.	—

eSRAM Intel FPGA IP v19.1.3

Table 9. v19.1.3 2019.10.11

Intel Quartus Prime Version	Description	Impact
19.3	Updated the description for **PLL Reference Clock Frequency** in the eSRAM Intel FPGA IP parameter editor.	—

eSRAM Intel FPGA IP v18.1

Table 10. v18.1 2018.10.03

Intel Quartus Prime Version	Description	Impact
18.1	Removed the HIPI register for iopll_lock2core_reg.	You may upgrade your IP core.

eSRAM Intel FPGA IP v18.0

Table 11. v18.0 May 2018

Description	Impact
Renamed Native eSRAM IP core to eSRAM Intel FPGA IP as per Intel rebranding.	—
Added a new interface signal: • iopll_lock2core eSRAM IOPLL lock status.	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Embedded Memory User Guide
- Errata for other IP cores in the Knowledge Base

Native eSRAM IP Core v17.1

Table 12. v17.1 November 2017

Description	Impact
Initial release. This IP core is available only in Intel Stratix 10 devices.	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Embedded Memory User Guide
- Errata for other IP cores in the Knowledge Base

Intel Stratix 10 Embedded Memory User Guide Archives
For the latest and previous versions of this user guide, refer to Intel® Stratix® 10 Embedded Memory User Guide. If an IP or software version is not listed, the user guide for the previous IP or software version applies.

eSRAM Intel® FPGA IP Release Notes

Documents / Resources

	intel eSRAM Intel FPGA IP [pdf] User Guide eSRAM Intel FPGA IP, Intel FPGA IP, FPGA IP, IP

References

- intel FPGA Knowledge Base Articles Search

- 1. Introduction to Intel® FPGA IP Cores
- 1. Intel Agilex® 7 Embedded Memory Overview
- 1. Intel® Quartus® Prime Design Suite Version 18.1 Update Release...
- 1. Intel® Stratix® 10 Embedded Memory Overview
- 4.2. eSRAM Intel® FPGA IP
- 1. eSRAM Intel® Agilex™ FPGA IP Release Notes
- FPGA Knowledge Base Articles Search
- Intel ISO 9001:2015 Registrations