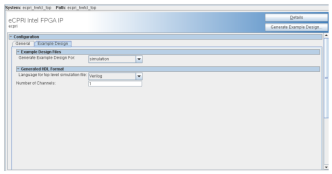

eCPRI Intel FPGA IP User Manual

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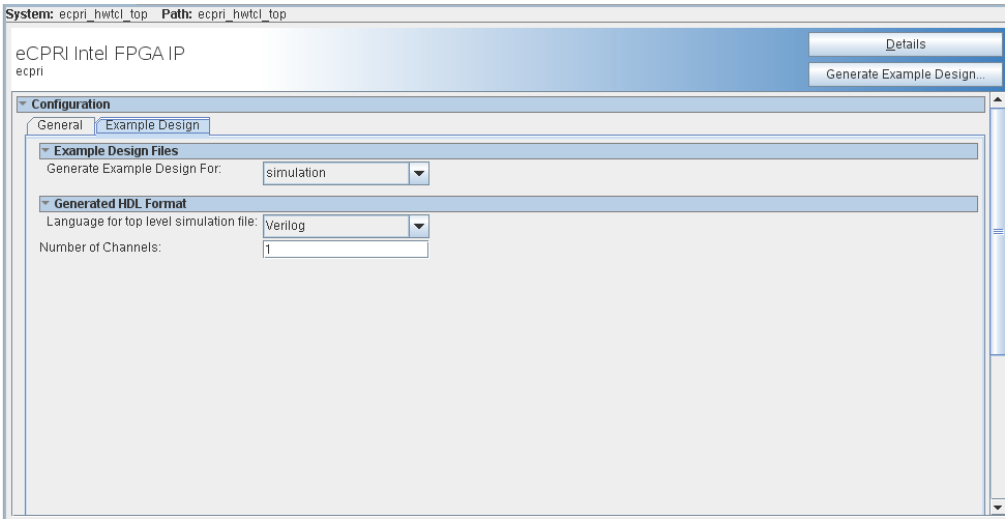

eCPRI Intel® FPGA IP Release Notes

The Intel® FPGA IP version (X.Y.Z) number can change with each Intel Quartus® Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Introduction to Intel FPGA IP Cores
- eCPRI Intel FPGA IP User Guide
- eCPRI Intel FPGA IP Design Example User Guide

eCPRI Intel FPGA IP v2.0.1

Table 1. v2.0.1 2022.11.15

Intel Quartus Prime Version	Description	Impact
22.3	Added support for the following Intel Agilex™ device grade and speed grade: • Device grade: Industrial • Speed grade: -3	—

eCPRI Intel FPGA IP v2.0.0

Table 2. v2.0.0 2022.08.26

Intel Quartus Prime Version	Description	Impact
22.2	Added support for L2 CoS priority packet arbitration scheme based on the O-RAN Control, User and Synchronization Plane Specification 7.01 (ORAN-WG4.CUS.0-v07.01), Section 5.3 Quality of Service.	—
	Added support for Data Flow Identification mechanism based on the O-RAN Control, User and Synchronization Plane Specification 7.01 (ORAN-WG4.CUS.0-v07.01), Section 5.4 Data Flow Identification.	—
	Added new signal:	—

Intel Quartus Prime Version	Description	Impact
	• tx_queue_<*N*>_fifo_full	
	• ext_source_pkt_type	
	• ext_tx_ingress_timestamp_96b_data	
	• ptp_tx_ingress_timestamp_96b_data	
	Added new IP parameters:	
	• **Default VLAN ID**	
	• **Data Flow Maching Mechanism**	
	• **Packets Arbitration Scheme**	
	• **TX Packets Default Priority**	
	• **TX Arbitration Queue 0 Depth**	
	• **TX Arbitration Queue 1 Depth**	—
	• **TX Arbitration Queue 2 Depth**	
	• **TX Arbitration Queue 3 Depth**	
	• **TX Arbitration Queue 4 Depth**	
	• **TX Arbitration Queue 5 Depth**	
	• **TX Arbitration Queue 6 Depth**	
• **TX Arbitration Queue 7 Depth**		

eCPRI Intel FPGA IP v1.4.1

Table 3. v1.4.1 2022.07.01

Intel Quartus Prime Version	Description	Impact
22.1	Added the hardware design example support for Intel Agilex F-tile device variations. The design example supports the following development kits: • Intel Agilex I-Series FPGA Development Kit • Intel Agilex I-Series Transceiver-SoC Development Kit	—
	Added support for QuestaSim* simulator.	—
	Removed support for ModelSim* SE simulator.	—
21.3	Added IP-XACT support.	—
	Issue fixed: Unable to detect list of tiles for a device.	No incorrect tile selection.

eCPRI Intel FPGA IP v1.4.0
Table 4. v1.4.0 2021.10.01

Intel Quartus Prime Version	Description	Impact
21.2	Added support for Intel Agilex F-tile devices.	—
	Added support for multi-channel designs.	—
	Removed support for NCSim* simulator.	—
	Issue fixed: The **Streaming** option was unavailable when you enable the **Pair with ORAN** option in the IP Parameter Editor.	You can enable or disable the **Streaming** option when the **Pair with ORAN** parameter is enabled.

eCPRI Intel FPGA IP v1.3.0
Table 5. v1.3.0 2021.02.26

Intel Quartus Prime Version	Description	Impact
20.4	Added support for Intel Agilex E-tile devices.	—
	Added support for 1588 PTP Fingerprint (8-bit width) as a standard feature.	No backward compatibility with 4-bit PTP Fingerprint Width

eCPRI Intel FPGA IP v1.2.0
Table 6. v1.2.0 2021.01.08

Intel Quartus Prime Version	Description	Impact
	Added support for interworking function (IWF) type 0.	You can connect eCPRI node with one CPRI node.
	Supports pairing of eCPRI Intel FPGA IP with O-RAN Intel FPGA IP.	—
	Added following new IWF related parameters: • **Interworking Function (IWF) Support** • **Interworking Function (IWF) Type** • **Interworking Function (IWF) Number of CPRI**	Using these parameters, you can enable your eCPRI IP for IWF functionality.

20.3	Added following IWF related interfaces: • IWF Type 0 eCPRI Source Interface • IWF Type 0 eCPRI Sink Interface • IWF Type 0 CPRI MAC Interface *Note:* Refer to *eCPRI Intel FPGA IP User Guide* for detailed information on signals related to these interfaces.	—
	Added following clock signals: • iwf_gmii_rxclk[N] • iwf_gmii_txclk[N] • gmii_rxclk[N] • gmii_txclk[N]	—
	Added following reset signals: • iwf_rst_tx_n • iwf_rst_rx_n • rst_tx_n_sync • rst_rx_n_sync • iwf_gmii_rxreset_n[N] • iwf_gmii_txreset_n[N] • gmii_rxreset_n[N] • gmii_txreset_n[N]	—
	The eCPRI IP design example for Intel Arria® 10 device is n ow available.	—

eCPRI Intel FPGA IP v1.1.0
Table 7. v1.1.0 2020.05.18

Intel Quartus Prime Version	Description	Impact
20.1	Added support for Intel Arria 10 devices.	—
	The IP supports 10G data rate for Intel Stratix® 10 and Intel Arria 10 devices.	—
	Added following new parameters: • **Streaming** • **Pair with ORAN** • **One-way Delay Measurement Timer Bitwidth** • **Remote Memory Access Timer Bit-width** • **Remote Reset Timer Bit-width**	—

eCPRI Intel FPGA IP v1.0.0
Table 8. v1.0.0 2020.04.13

Intel Quartus Prime Version	Description	Impact
19.4	Initial release.	—

eCPRI Intel FPGA IP User Guide Archives

For the latest and previous versions of this user guide, refer to the eCPRI Intel FPGA IP User Guide HTML version. Select the version and click Download. If an IP or software version is not listed, the user guide for the previous IP or software version applies.

eCPRI Intel FPGA IP Design Example User Guide Archives

For the latest and previous versions of this user guide, refer to the eCPRI Intel FPGA IP Design Example User Guide HTML version. Select the version and click Download. If an IP or software version is not listed, the user guide for the previous IP or software version applies.

Documents / Resources

	intel eCPRI Intel FPGA IP [pdf] User Manual eCPRI Intel FPGA IP, eCPRI Intel, FPGA IP

References

- 1. Introduction to Intel® FPGA IP Cores
- 1. eCPRI Intel® FPGA IP Release Notes
- 1. Introduction
- 1. Quick Start Guide
- 1. Quick Start Guide
- 1. Introduction
- Intel ISO 9001:2015 Registrations