intel Cyclone 10 LP Device Family Pin Connection User Guide

Intel® Cyclone® 10 LP Device Family Pin Connection Guidelines

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Contents

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Clock and PLL Pins

Note: Intel® recommends that you create an Intel Quartus® Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 1. Clock and PLL Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
CLK[0,2,4,6,9,11,13,15], DIFFCLK_ [0 .. 7)p (Note 7)	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.	Connect unused CLK or DIFFCLK pins to GND.
CLK[1,3,5,7,8,10,12,14], DIFFCLK_ [0 ..7) n (Note 7)	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.	Connect unused CLK or DIFFCLK pins to GND.
PLL [1 . . 4)_CLKOUTp (Note 8)	I/O, Output	Optional positive terminal for external clock outputs from PLL [1..4]. Each pin can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.	When not using this pin as a clock output, this pin may be used as a user I/O. When not using these pins, connect them as defined in Intel Quartus Prime software.
PLL [1 .. 4]_CLKOUTn (Note 8)	I/O, Output	Optional negative terminal for external clock outputs from PLL [1..4]. Each pin can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.	When not using this pin as a clock output, this pin may be used as a user I/O. When not using these pins, connect them as defined in Intel Quartus Prime software.
DPCLK [0.11]	DPCLK	Dual-purpose DPCLK pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets, and clock enables.	When these I/O pins are not used, they can be tied to GND.

CDPCLK [0 .. 7]	CDPCLK	Dual-purpose CDPCLK pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets, and clock enables. Only one of the two CDPCLK in each corner can feed the clock control block at a time. The other pin can be used as general-purpose I/O pin. The CDPCLK signals incure more delay to the clock control block because they are multiplexed before driving into the clock control block.	When these I/O pins are not used, they can be tied to GND.

Configuration/JTAG Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 2. Configuration/JTAG Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
MSEL(0..3)	Input	Configuration input pins that set the configuration scheme. Some of the smaller Intel Cyclone® 10 LP devices or package options do not support AS configuration with fast delay (3.0V/2.5V) and do not have the MSEL[3] pin.	These pins are internally connected through a 9-Kf2 resistor to GND. Do not leave these pins floating. When these pins are unused, connect them to GND. Depending on the configuration scheme used, these pins should be tied to VCCA or GND. Refer to the “Configuration and Remote System Upgrades in Intel Cyclone 10 LP Devices” chapter in the Intel Cyclone 10 LP Handbook. If only)TAG configuration is used, connect these pins to GND.

nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In a multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration and JTAG programming, nCE should be connected to GND.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user- mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.	If you are using PS configuration scheme with a download cable, connect this pin through a 10-Kf2 resistor to VCCA. For other configuration schemes, if this pin is not used, this pin must be connected directly or through a 10-K4 resistor to VCCIO.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode.	This pin is not available as a user I/O pin. CONF_DONE should be pulled high by an external 10-Kf2 pull-up resistor.
nCEO	I/O, Output (open-drain)	Output that drives low when device configuration is complete. This pin can be used as a regular I/O if not used for device configuration.	When not using this pin, you can leave it unconnected. During multi-device configuration, this pin feeds the nCE pin of a subsequent device. In this case, tie the 10-Kf2 pull-up resistor to an acceptable voltage for all devices in the chain which satisfies the input voltage of the receiving device. During single device configuration, this pin can be used as a regular I/O.

nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization.	This pin is not available as a user I/O pin. nSTATUS should be pulled high by an external 10-K52 pull-up resistor.
TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin through a 1-K52 pull-down resistor to GND. To disable the JTAG circuitry, connect TCK to GND.
TMS	Input	Dedicated JTAG test mode select input pin.	When interfacing with 2.5 V, 3.0 V, or 3.3 V configuration voltage standard, connect this pin through a 10-kg/ resistor to VCCA. For configuration voltage of 1.5 V and 1.8 V, connect this pin through a 10-kf2 resistor to VCCIO supply instead.
TDI	Input	Dedicated JTAG test data input pin.	When interfacing with 2.5 V, 3.0 V, or 3.3 V configuration voltage standard, connect this pin through a 10-1(52 resistor to VCCA. For configuration voltage of 1.5 V and 1.8 V, connect this pin through a 10-kfl resistor to VCCIO supply instead.
TDO	Output	Dedicated JTAG test data output pin.	If the TDO pin is not used, leave this pin unconnected.
r.CSO	I/O, Output (AS)	This pin functions as nCSO in AS mode. nCSO: Output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.	When not programming the device in AS mode, nCSO is not used. If the pin is not used as an I/O, you should leave the pin unconnected.

DATA1, ASDO	Input (FPP), Output (AS)	This pin functions as DATA1 in PS and FPP modes, and as ASDO in AS mode. DATA1: Data input in non-AS mode. Byte-wide configuration data is presented to the target device on DATA[0..7]. In PS configuration scheme, DATA1 functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin and the state of this pin depends on the Dual- Purpose Pin settings. ASDO: Control signal from the FPGA to the serial configuration device in AS mode that is used to read out configuration data.	When not programming the device in AS mode, this pin is available as a user I/O pin. If the pin is not used as an I/O, then you should leave the pin unconnected.
DATA [2 ..	Input (FPP)	Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA[0..7]. In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA [2..7] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings.	When not programming the device in FPP mode, these pins are available as user I/O pins. If the pin is not used as an I/O you should leave the pin unconnected.
DCLK	Input (PS, FPP), Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLX is an output from the FPGA that provides timing for the configuration interface.	Do not leave this pin floating. Drive this pin either high or low. You can configure DCLX as a user I/O only after active serial configuration.
CRC_ERROR (Notes 13 and 15)	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. This pin can be used as regular I/O if not used for CRC error detection. The CRC_ERROR pin is a dedicated output by default. Optionally, you can enable the CRC_ERROR pin as an open-drain output in the Device & Pin option dialog box in the Intel Quartus Prime software.	When using this pin, connect it through an external 10-Kf2 pull-up resistor to an acceptable voltage for all devices in the chain that satisfies the input voltage of the receiving device. When not using this pin, it can be left floating.

DEV_CLRn	I/O (when option off), Input (when option on)	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Intel Quartus Prime software.	When the dedicated input DEV_CLRn is not used and this pin is not used as an I/O, tie this pin to GND.
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Intel Quartus Prime software.	When the dedicated input DEV_OE is not used and this pin is not used as an I/O, then you should tie this pin to GND.
DATAO	Input (PS, FPP, AS)	Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. After AS configuration, DATAO is a dedicated input pin with optional user control. After PS or FPP configuration, DATAO is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings.	If you are using a serial configuration device in AS configuration mode, you must connect a 25-0 series resistor at the near end of the serial configuration device for the DATAO. When the dedicated input for DATAO is not used and this pin is not used as an I/O, then you must leave this pin unconnected.
IN:T_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Intel Quartus Prime software.	When using this pin, connect it through an external 10-K4 pull-up resistor to an acceptable voltage for all devices in the chain that satisfies the input voltage of the receiving device. When not using this pin, it can be left floating or tied to GND.

CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Intel Quartus Prime software.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O, then you should connect this pin to GND.

Differential I/O Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 3. Differential I/O Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DIFFIO_[L,R, T, B] [0 .. 61] [p, n] (Note 11)	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS compatible signals. Pins with a “p” suffix carry the positive signal for the differential channel. Pins with an “n” suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in the Intel Quartus Prime software.

Reference Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 4. Reference Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
RUP[1..4]	I/O, Input	Reference pins for OCT block in I/O banks 2, 4, 5, and 7. The external precision resistor RUP must be connected to the designated RUP pin within the same bank when used. If the RUP pin is not used, this pin can function as a regular I/O pin.	When using OCT tie these pins to the required banks VCCIO through either a 25 Q or 50 Q resistor, depending on the desired I/O standard. When the device does not use this dedicated input for the external precision resistor or as an I/O, it is recommended that the pin be connected to VCCIO of the bank in which the RUP pin resides or GND.
RDN[1..4]	I/O, Input	Reference pins for OCT block in I/O banks 2, 4, 5, and 7. The external precision resistor RDN must be connected to the designated RDN pin within the same bank when used. If the RDN pin is not used, this pin can function as a regular I/O pin.	When using OCT tie these pins to GND through either a 25 Q or 50 0 resistor depending on the desired I/O standard. When the device does not use this dedicated input for the external precision resistor or as an I/O, it is recommended that the pin be connected to GND.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration, these pins may be connected to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern, leave these pins floating.

Supply Pins

(See Note 12)
Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 5. Supply Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines

VCCINT	Power	These are internal logic array voltage supply pins.	All VCCINT pins must be connected to either a 1.0 V supply or a 1.2 V supply. Intel Cyclone 10 LP devi ces with VCCINT 1.0V, and Intel Cyclone 10 LP dev ices with VCCINT 1.2V, have different ordering cod es. See Note 15. You have the option to share VCCD_PLL with VCCI NT with a proper isolation filter. Decoupling depend s on the design decoupling requirements of the spe cific board. See Notes 2 and 4.
VCCD_PLL [1. .41	Power	Digital power for Pas[1..4]. Y ou must power up these pins, even if the PLL is not used.	You are required to connect these pins to either 1.0 V (if VCCINT 1.0 V) or 1.2 V (if VCCINT 1.2 V), eve n if the PLL is not used. Intel Cyclone 10 LP devices with VCCINT 1.0 V, and Intel Cyclone 10 L P devices with VCCINT 1.2 V, have different orderin g codes. See Note 15. With a proper isolation filter, these pins can be sour ced from the same regulator as VCCINT. Use an iso lated switching power supply with 1 3% maximum v oltage ripple. See Note 11. Decoupling for these pins depends on the design d ecoupling requirements of the specific board. See Notes 2, 4, and 6.
VCCA [1..4]	Power	Analog power for Plis[1..4]. A ll VCCA pins must be powere d and all VCCA pins must be powered up and powered do wn at the same time even if n ot all the PLLS are used. Des igner is advised to keep this pin isolated from other VCC p ins for better jitter performanc e.	You are required to connect these pins to 2.5 V, even if the PLL is not used. Use an isolated linear o r switching power supply with 1 3% maximum volta ge ripple. See Note 11. Intel recommends you to keep this pin isolated from other VCC for better jitter performance.
VCCIO 11..8)	Power	These are I/O supply voltage pins for banks 1 through 8. E ach bank can support a differ ent voltage level. VCCIO sup plies power to the input and o utput buffers for all I/O standa rds.	Connect these pins to 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V supplies, depending on the I/O standard assigned to the I/O bank. Decoupling depends on t he design decoupling requirements of the specific b oard. See Notes 2 and 4.

GND	Ground	Device ground pins.	All GND pins should be connected to the board GN D plane.
GNDA[1..4]	Ground	Ground for PLLs[1..4] and ot her analog circuits in the devi ce.	You can consider connecting the GNDA pins to the GND plane without isolating the analog ground plan e on the board provided that the digital GND planes are stable, quiet, and with no ground bounce effect.
VREFB[1..8]N[0..2]	I/O	Input reference voltage for ea ch I/O bank. If a bank uses a voltage-referenced I/O stand ard, then these pins are used as t he voltagereference pins for t he bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.	If VREF pins are not used, you should connect the m to either the VCCIO in the bank in which the pin r esides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note 2.

Notes to Intel Cyclone 10 LP Pin Connection Guidelines

1. FPP configuration is supported in most devices, except for the E144 package.
2. Capacitance values for the power supply decoupling capacitors should be selected after consideration of the amount of power needed to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage drop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To assist in decoupling analysis, Power Distribution Network (PDN) Design Tool serves as an excellent decoupling analysis tool.
3. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
4. Use the Intel Cyclone 10 LP Early Power Estimator to determine the current requirements for VCCINT and other power supplies.
5. These supplies may share power planes across multiple Intel Cyclone 10 LP devices.
6. Use separate power regulators for VCCA and VCCD_PLL. PLL power supply may originate from another plane

on the board but must be isolated using a ferrite bead or other equivalent methods. If using a ferrite bead, choose an 0402 package with low DC resistance, higher current rating than the maximum steady state current for the supply it is connected to (VCCA or VCCD_PLL) and high impedance at 100 MHz.

7. The number of dedicated global clocks for each device density is different. Please refer to the “Clock Networks and PLLs in Intel Cyclone 10 LP Devices” chapter in the Intel Cyclone 10 LP Device Handbook.
8. The number of PLLs consisting of GPLLs and MPLLs for each device density is different. 10CL006 and 10CL010 support 2 PLLs. 10CL016 and other larger Intel Cyclone 10 LP densities support 4 PLLs.
9. VCCA may use a switching regulator with a voltage ripple of ± 3% maximum. VCCD_PLL may use a switching power supply with a voltage ripple of ± 3 % maximum.
10. You must follow specific requirements when interfacing Intel Cyclone 10 LP device with 2.5 V/3.0 V/3.3 V configuration voltage standards. All I/O inputs must maintain a maximum AC voltage of 4.1 V. Refer to Configuration and JTAG Pin I/O Requirements of the “Configuration and Remote System Upgrades in Intel Cyclone 10 LP Devices” chapter.
11. The differential TX/RX channels for each device density and package is different. Please refer to the “I/O Features in Intel Cyclone 10 LP Devices” chapter in the Intel Cyclone 10 LP Device Handbook.
12. Intel highly recommends using an independent PCB via for each independent power or ground ball on the package. Sharing power or ground pin vias on the PCB could lead to noise coupling into the device and result in reduced jitter performance.
13. CRC error detection is only supported in Intel Cyclone 10 LP devices with VCCINT 1.2 V, and not in Intel Cyclone 10 LP devices with VCCINT 1.0 V.
14. The Intel Quartus Prime*.pin file created after compiling the design project in the Intel Quartus Prime software lists unused clock input pins as GND+ (unused input clocks and PLLs). Verify that any pins listed as such in the Intel Quartus Prime*.pin file are connected to the board as indicated in these recommendations.
15. There are two variants of Intel Cyclone 10 LP devices; one powered with core voltage VCCINT 1.0 V, and another powered with core voltage VCCINT 1.2 V. Each variant has different ordering codes.
16. The number of optional high speed differential reference clock input for each device density is different.

Related Information

http://www.altera.com/technology/signal/power-distribution-network/sgl-pdn.html

Power Supply Sharing Guidelines

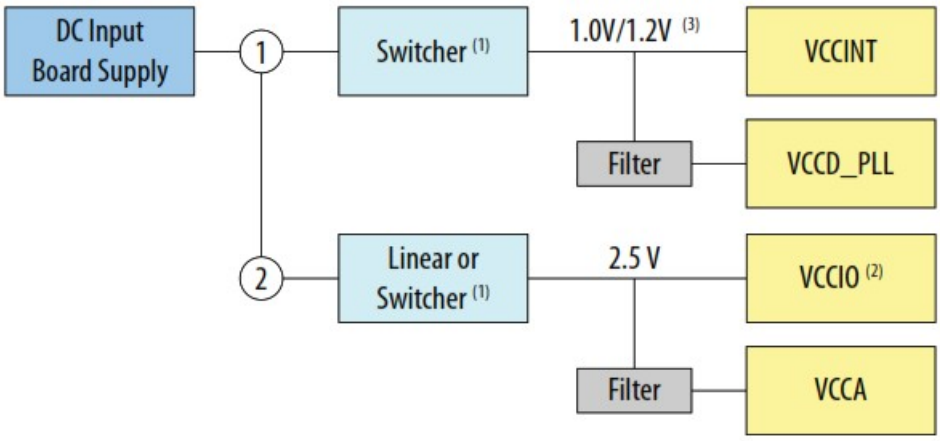
Table 6. Power Supply Sharing Guidelines for Intel Cyclone 10 LP Devices
Example Requiring 2 Power Regulators

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Switching	Notes

VCCINT	1	1.0/1.2	± 30 mV/ ± 50 mV	Switcher (*)	Share	You have the option to share VCCD_PLL with VCCINT using a proper isolation filter. With proper isolation filter, limit the VCCD_PLL power supply to ±3% maximum ripple voltage. Depending on the regulator capabilities, this supply may be shared with multiple Intel Cyclone 10 LP devices. Use the Early Power Estimation (EPE) tool within the Intel Quartus Prime software to assist in determining the power required for your specific design.
VCCD_PLL					Isolate	
vccio	2	Varies	± 5 %	Linear or Switcher (*)	Share if 2.5 V	If VCCIO requires 2.5 V, you have the option to share VCCA with VCCIO using a proper isolation filter. However, for any other VCCIO voltage, you will require a 2.5 V regulator for VCCA. Use the Early Power Estimation (EPE) tool within the Intel Quartus Prime software to assist in determining the power required for your specific design.
VCCA		3.			Isolate	You have the option to share VCCA with VCCIO using a proper isolation filter. With proper isolation filter, limit the VCCA power supply to ±3% maximum ripple voltage. Depending on the regulator capabilities, this supply may be shared with multiple Intel Cyclone 10 LP devices. Use the Early Power Estimation (EPE) tool within the Intel Quartus Prime software to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements.

Figure 1. Example Power Supply Sharing Guidelines for Intel Cyclone 10 LP Devices



Note:

1. When using a switcher power supply for VCCA, limit this supply to ±3% maximum ripple voltage. When using a switcher power supply for VCCD_PLL, limit this supply to ±3% maximum ripple voltage.
2. Connect VCCIO pins on banks 4, 5, 6, 7, and 8 to 1.2 V/ 1.5 V/ 1.8 V/ 2.5 V/ 3.0 V/ 3.3 V supplies, depending on the I/O standard connected to the specified bank.
3. There are two variants of Intel Cyclone 10 LP devices; one powered with core voltage VCCINT 1.0 V, and another powered with core voltage VCCINT 1.2 V. Each variant has different ordering codes.

Document Revision History for the Intel Cyclone 10 LP Device Family Pin Connection Guidelines

Document Version	Changes
2020.11.09	Added DPCLK[0.11] and CDPCLK[0..7] pins in the Clock and PLL Pins table.
2019.11.06	Updated note 2 in the Example Power Supply Sharing Guidelines for Intel Cyclone 10 LP Devices figure.
2019.07.03	Updated the connection guidelines of the TMS and TDI pins.

Date	Version	Description of Changes
Nov-17	2017.11.06	• The document is no longer preliminary. • Updated the note reference for the VCCINT and VCCD_PLL[1..4] pins. • Updated the note reference for the TDI pin.
Jun-17	2017.06.02	Updated the supported configuration schemes.
Feb-17	2017.02.13	Initial release.

Send Feedback

Documents / Resources

	intel Cyclone 10 LP Device Family Pin Connection [pdf] User Guide Cyclone 10 LP Device Family Pin Connection, Cyclone 10 LP, Device Family Pin Connection, Family Pin Connection, Pin Connection

References

- intel Power Distribution Network (PDN) | Intel
- intel Intel® Cyclone® 10 LP Device Family Pin Connection Guidelines
- intel Intel ISO 9001:2015 Registrations