intel Cyclone 10 GX Device Errata User Guide

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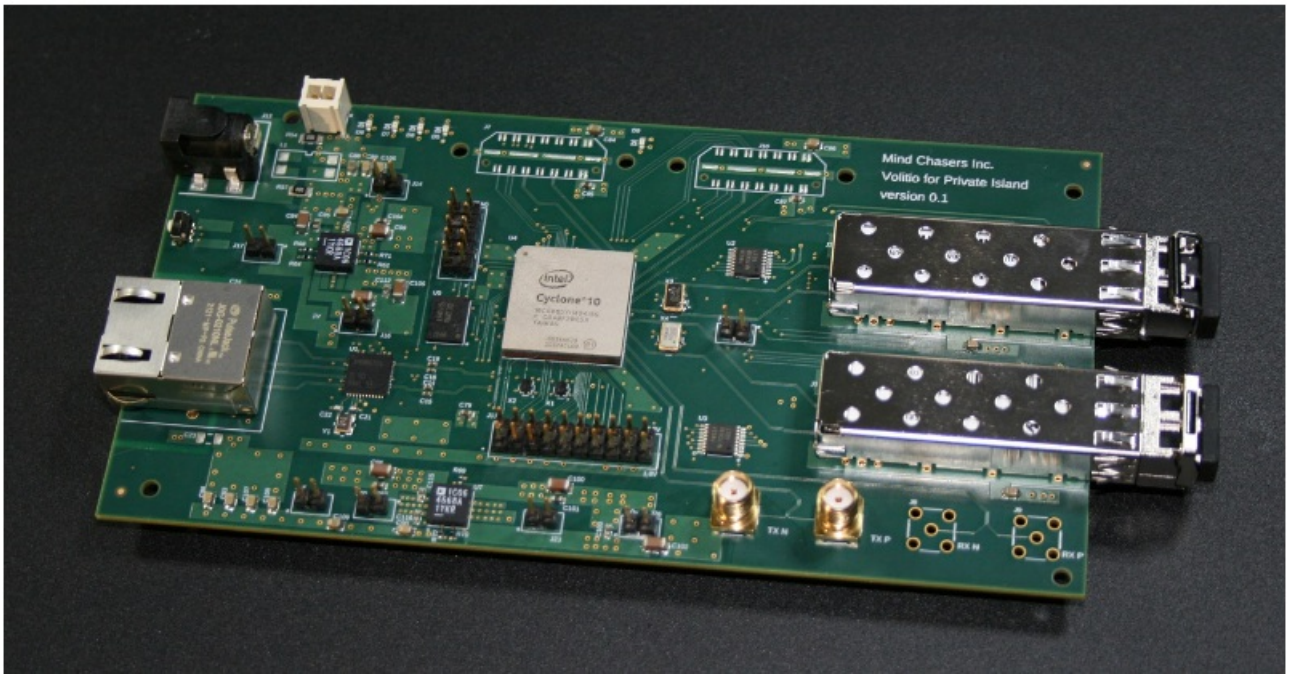

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Intel® Cyclone® 10 GX Device Errata

This errata sheet provides information about known device issues affecting Intel® Cyclone® 10 GX devices. The table below lists specific device issues and affected Intel Cyclone 10 GX devices.

Table 1. Device Issues

Issue	Affected Devices	Planned Fix
Automatic Lane Polarity Inversion for PCIe Hard IP on page 4	All Intel Cyclone 10 GX devices	No planned fix
High VCCBAT Current when VCC is Powered Down on page 5	All Intel Cyclone 10 GX devices	No planned fix
Failure on Row Y59 When Using the Error Detection Cyclic Redundancy Check (EDCRC) or Partial Reconfiguration (PR) on page 6	All Intel Cyclone 10 GX devices	No planned fix
GPIO Output may not meet the On-Chip Series Termination (Rs OCT) without Calibration Resistance Tolerance Specification or Current Strength Expectation on page 7	All Intel Cyclone 10 GX devices	No planned fix

Automatic Lane Polarity Inversion for PCIe Hard IP

For Intel Cyclone 10 GX PCIe Hard IP open systems where you do not control both ends of the PCIe link, Intel does not guarantee automatic lane polarity inversion with the Gen1x1 configuration, Configuration via Protocol (CvP), or Autonomous Hard IP mode. The link may not train successfully, or it may train to a smaller width than expected. There is no planned workaround or fix.

For all other configurations, refer to the following workaround.

Workaround

Refer to the Knowledge Database in the related links below for details to workaround this issue.

Status

Affects: All Intel Cyclone 10 GX devices.
Status: No planned fix.

Related Information
Knowledge Database

High VCCBAT Current when VCC is Powered Down

If you power off VCC when VCCBAT remains powered on, VCCBAT may draw higher current than expected.

If you use the battery to maintain volatile security keys when the system is not powered up, VCCBAT current could be up to 120 µA, resulting in shortened battery life.

Workaround

Contact your battery provider to evaluate the impact to the retention period of the battery used on your board.

There is no impact if you connect the VCCBAT to the on-board power rail.

Status

Affects: All Intel Cyclone 10 GX devices

Status: No planned fix.

Failure on Row Y59 When Using the Error Detection Cyclic Redundancy Check (EDCRC) or Partial Reconfiguration (PR)

When the error detection cyclic redundancy check (EDCRC) or partial reconfiguration (PR) feature is enabled, you may encounter unexpected output from clocked components such as flip-flop or DSP or M20K or LUTRAM that are placed at row 59 in Intel Cyclone 10 GX devices.

This failure is sensitive to temperature and voltage.

Intel Quartus® Prime software version 18.1.1 and later displays the following error message:

- In Intel Quartus Prime Standard Edition:
  - Info (20411): EDCRC usage detected. To ensure reliable operation of these features on the targeted device, certain device resources must be disabled.
  - Error (20412): You must create a floorplan assignment to block out the device resources at row Y=59 and ensure reliable operation with EDCRC. Use the Logic Lock (Standard) Regions Window to create an empty reserved region with origin X0_Y59, height = 1 and width = <#>. Also, review any existing Logic Lock (Standard) regions that overlap that row and ensure if they account for the unused device resources.
- In Intel Quartus Prime Pro Edition:
  - Info (20411): PR and/or EDCRC usage detected. To ensure reliable operation of these features on the targeted device, certain device resources must be disabled.
  - Error (20412): You must create a floorplan assignment to block out the device resources at row Y59 and ensure reliable operation with PR and/or EDCRC.
    Use the Logic Lock Regions Window to create an empty reserved region, or add set_instance_assignment -name EMPTY_PLACE_REGION “X0 Y59 X<#> Y59-R:C-empty_region” -to | directly to your Quartus Settings File (.qsf). Also, review any existing Logic Lock regions that overlap that row and ensure if they account for the unused device resources.

Note: Intel Quartus Prime software versions 18.1 and earlier do not report these errors.

Workaround

Apply the empty logic lock region instance in the Quartus Prime Settings File (.qsf) to avoid use of row Y59. For more information, refer to the corresponding knowledge base.

Status

Affects: All Intel Cyclone 10 GX devices

Status: No planned fix.

GPIO Output may not meet the On-Chip Series Termination (Rs OCT) without Calibration Resistance Tolerance Specification or Current Strength Expectation

Description

The GPIO pull-up impedance may not meet the on-chip series termination (Rs OCT) without calibration resistance tolerance specification mentioned in the Intel Cyclone 10 GX device datasheet. While using the current strength selection, the GPIO output buffer may not meet expected current strength at VOH voltage level when driving HIGH.

Workaround

Enable the on-chip series termination (Rs OCT) with calibration in your design.

Status

Affects: All Intel Cyclone 10 GX devices

Status: No planned fix.

Document Revision History for Intel Cyclone 10 GX Device Errata and Design Guidelines

Document Version	Changes
2022.08.03	Added a new erratum: GPIO Output may not meet the On-Chip Series Termination (Rs OCT) without Calibration Resistance Tolerance Specification or Current Strengt h Expectation.
2020.01.10	Added a new erratum: Failure on Row Y59 When Using the Error Detection Cyclic Redundancy Check (EDCRC) or Partial Reconfiguration (PR).
2017.11.06	Initial release.

are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
Other names and brands may be claimed as the property of others.

Documents / Resources

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