

Intel AN 988 22.4 Quartus Prime Pro Edition Software User Guide

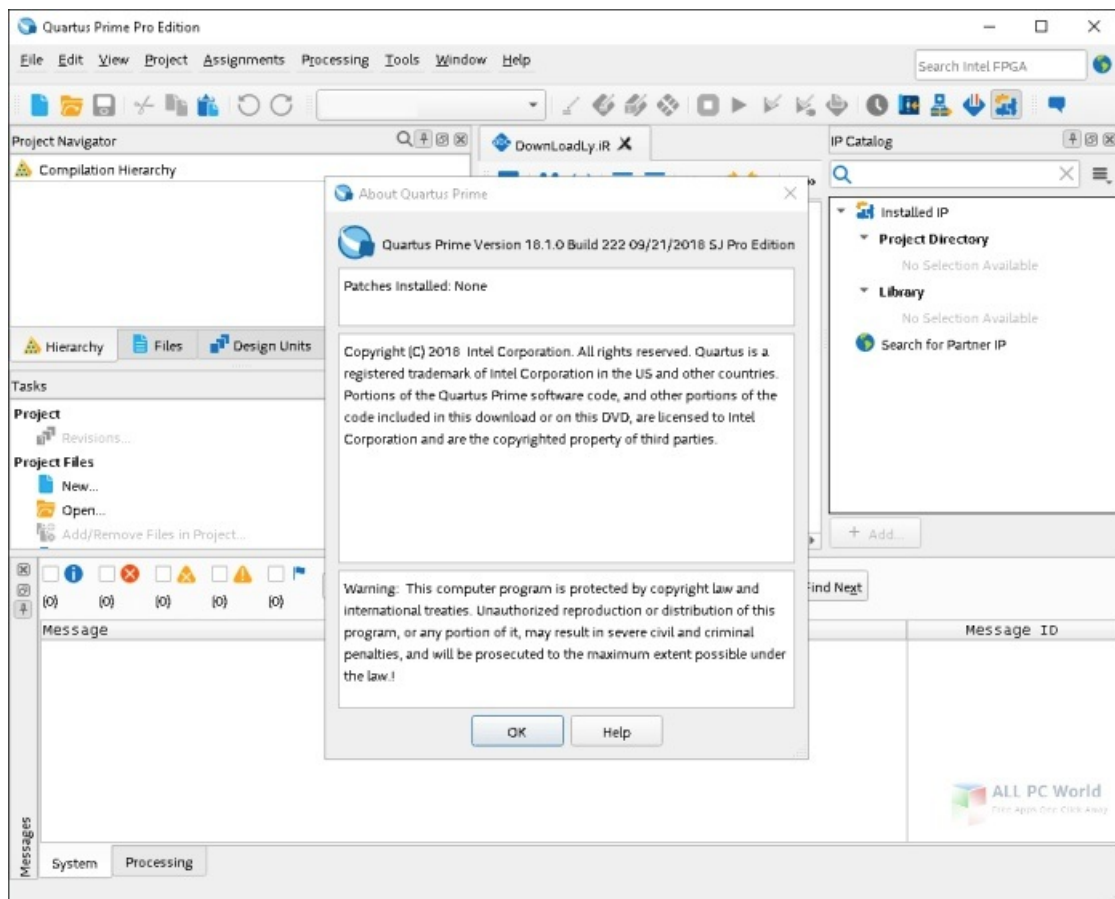
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Intel AN 988 22.4 Quartus Prime Pro Edition Software



FAQs

Answers to Top FAQs

- **Q:** What is the board-aware flow?
- **A:** What Is the Board-Aware Flow on page 3
- **Q:** What do I need for this application note?
- **A:** Document Prerequisites on page 4
- **Q:** Where can I get the support files?
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- **Q:** How do I create a new board file?
- **A:** Step 2: Create a New Board File on page 13
- **Q:** How do I create IP presets?
- **A:** Step 3: Create IP Presets for the Board on page 15
- **Q:** How do I use board files?
- **A:** Step 4: Using Boards and Presets on page 17 Online Version

Using the Board-Aware Flow in the Intel® Quartus® Prime Pro Edition Software

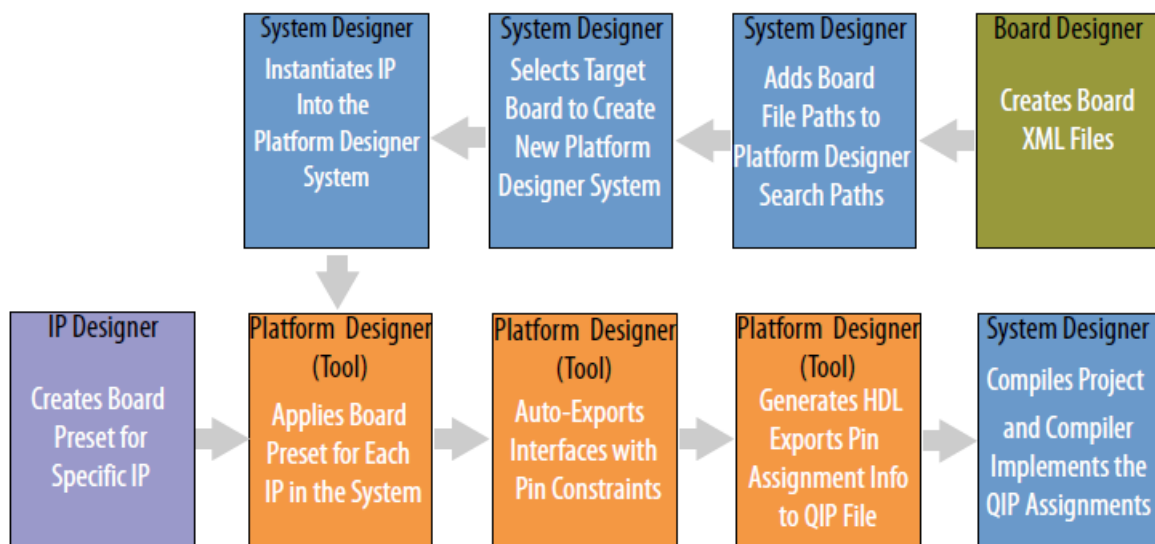
This application note demonstrates using the Intel® Quartus® Prime software board aware flow. You can use the board-aware flow to accelerate the process of appropriately configuring, connecting, and validating IP for a target board.

What is the Intel Quartus Prime Software Board-Aware Flow?

The board-aware flow simplifies the application of appropriate parameters and pin assignments for the instantiated IP in your project, thereby reducing the chance of configuration errors. You can also save your preferred and verified board and IP configurations for reuse in other projects that target the same IP or board. In the board-aware flow, you can optionally start your project from a pre-verified design example and target a specific Intel FPGA development board, rather than just a specific device. You can then create IP presets targeting the specific board. The Intel Quartus Prime Platform Designer system integration tool is also board-aware, allowing you to automatically set pin assignments and export appropriate system interfaces for the target board. The complete process of configuring, connecting, and validating IP for a target board is typically implemented by multiple developers performing specialized tasks. For example:

- An IP designer that creates board presets for specific IPs.
- A system designer that combines individual IP components into a system.
- A board designer creates the XML board files defining the target board.

Board-Aware Flow Typical Tasks and Roles



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The board-aware flow helps to ensure the proper hand-off, consistency, and reuse of configuration options across multiple projects, developers, and boards.

This application note guides you through the following steps in the board-aware flow:

- Step 1: Specify a Target Board for the Project
- Step 2: Create a New Board File
- Step 3: Create IP Presets for the Board

- Step 4: Create a Design Using Board and Preset Files
- Step 5: Compile and Verify the Design
- Step 6: Configure the Board with Software

Document Prerequisites

Use of this application note requires that you already have the following:

- Installation of Intel Quartus Prime Pro Edition version 22.4, with Intel Agilex™ device support.
- Download and extract supporting design example files, as Downloading and Extracting Supporting Files on page 4 describes.
- Basic familiarity with the Intel Quartus Prime Pro Edition FPGA implementation flow and use of the Platform Designer tool.
- Connection to the internet for optional download of online Intel Quartus Prime FPGA design examples.

Related Information

- Intel Quartus Prime Pro Edition User Guide: Getting Started
- Intel Quartus Prime Pro Edition User Guide: Platform Designer

Downloading and Extracting Supporting Files

1. Download and extract the Board-Aware Design Example Supporting Files to a directory on your computer. Do not use spaces in the directory path name.
2. View the extracted tutorial design files and directory structure. board_aware_example_agilex.zip contains the following files:

Table 1. Supporting Design Example Files

File	Description
pin_pio.tcl	Tcl pin constraints file that contains appropriate pin assignments for the system. You can optionally load this file rather than manual entry.
pio_led.out.sd	Synopsys Design Constraints file that contains appropriate timing constraints for the completed design.
esp.ip	Represents the In-System Sources and Probes Intel FPGA IP in the design for use in debugging the design.
reset_release.ip	Represents the Reset Release Intel FPGA IP in the design. This IP outputs nINIT_DONE after finishing device initialization. User mode initialization can begin as soon as the nINIT_DONE signal asserts.

AN 988: Using the Board-Aware Flow: in the Intel Quartus Prime Pro Edition Software.

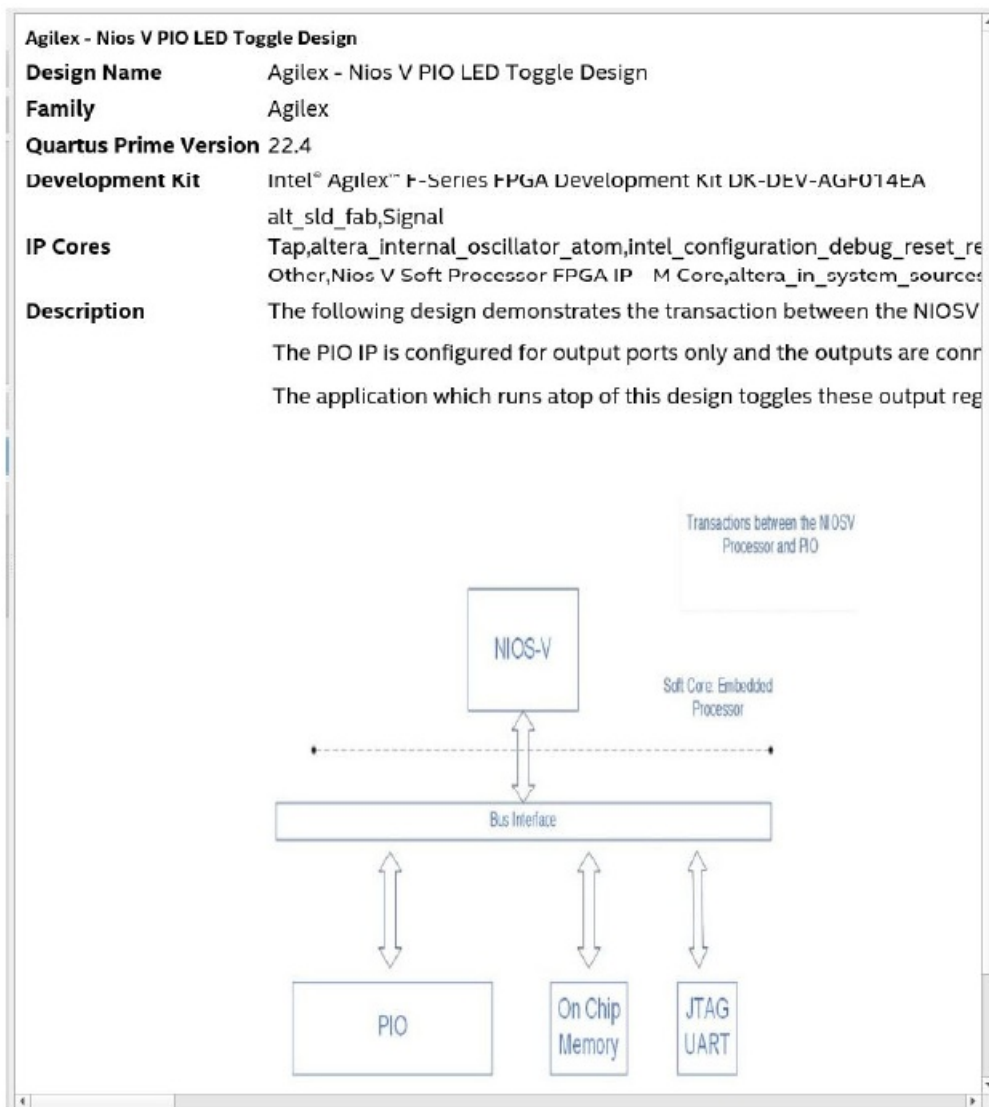
Using the Board-Aware Flow in the Intel® Quartus® Prime Pro Edition Software

Accessing Intel FPGA Design Examples

You can optionally base your design project on a pre-verified Intel FPGA design example that targets a specific Intel FPGA board or development kit, or you can start with an empty project. Access available design examples using any of the following methods:

- Pre-installed design examples—you can immediately access the design examples that install along with the Intel Quartus Prime software installation at: <quartus>\acds\quartus\common\board_designs.
- Online design examples—you can access design examples hosted online, which include designs from the Intel FPGA Design Store.
- Downloaded design examples—you can access previously downloaded design examples or any design example that you store in a local drive, under downloaded design examples.
- The steps in this application note use the pre-installed Agilex – Nios V PIO LED Toggle Design to illustrate the board-aware flow.

Agilex – Nios V PIO LED Toggle Design Description



Accessing Pre-Installed Design Examples

The Intel Quartus Prime software installation includes design examples for your immediate use. You can create a new project based on one of the available Intel FPGA design examples. You can access the pre-installed design examples from the Intel Quartus Prime software Home page, from the New Project Wizard, or with the File ► Open Example Project menu command.

To create a new project based on a pre-installed design example, follow these steps:

1. Start the Intel Quartus Prime Pro Edition software.
2. Click File ► Open Example Project. The Design Example page of the New Project Wizard opens.
3. Under What is the working directory for this project? specify the directory location to store your project files.
4. Under Find Options, specify the following settings to filter the list of design examples for the target device and board:
 - In Load from, select Pre-Installed design examples.
 - In Family, select Agilex.
 - In the Intel Quartus Prime version, select 22.4.
 - In the Development kit, select Intel Agilex F-Series FPGA Development Kit DK-DEV-AGF014EA.

Location of Pre-Installed Design Examples

Find Options

Load from: Pre-installed design examples

Family: Agilex

Intel Quartus Prime version: 22.4

Development kit: Intel® Agilex™ F-Series FPGA Development Kit DK-DEV-AGF014EA

More settings... Reset

Legend

Q <<Filter>>

	Load From	Design Name
✓	Pre-installed	Agilex - Nios V PIO LED Toggle Design
✓	Pre-installed	Agilex - NiosV EMIF data mover Design
✓	Pre-installed	Agilex - NIOS2-EMIF-PIO Design

- Under Design name, select the Agilex – Nios V PIO LED Toggle Design design.
- Click Next, and then click Finish. The Agilex – Nios V PIO LED Toggle Design extracts to the working directory and opens in the Intel Quartus Prime software.

Using the Board-Aware Flow in the Intel® Quartus® Prime Pro Edition Software 757339 | 2023.01.09

Accessing Downloaded Design Examples

You can create a new project based on a design example that you have previously downloaded. To test this method, you can download a design example .par file from the Intel FPGA Design Store, or from another online repository that stores design examples in .par format, into your working directory. Platform Designer also classifies designs that you create yourself and store in a local drive as downloaded examples. To create a new project based on a downloaded design example, follow these steps:

1. Start the Intel Quartus Prime Pro Edition software.
2. Click File ► Open Example Project. The Design Example page of the New Project Wizard opens.
3. Under What is the working directory for this project?, specify the directory location to store your project files.
4. Click the Design Store button. The Design Store web page displays an unfiltered list of available design examples.

Design Store Listing Available Design Examples

Intel® Stratix® (55)

Intel® Agilex™ FPGAs and SoC FPGAs (7)

Intel Quartus Prime Version ^

CLEAR

Intel® Quartus® Prime Pro Edition (7)

Agilex - Design Example: Achieving Timing Closure When Using Top I/O Sub Bank

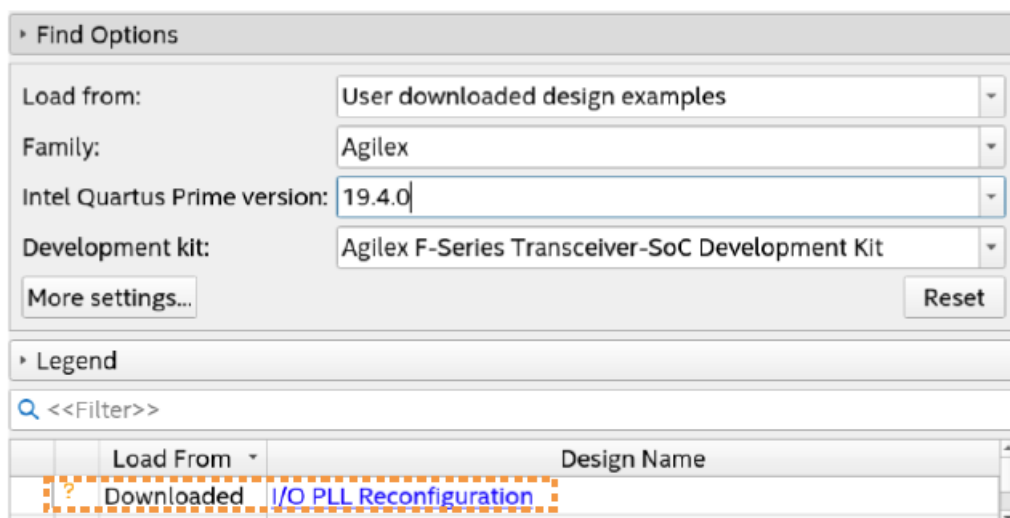
Agilex - Intel P-tile CvP Example Design for Initialization mode

Agilex - I/O PLL Reconfiguration

- From the left navigation menu, click on Agilex FPGAs and SOC FPGAs to filter the list of design examples.
- Click the I/O PLL Reconfiguration design example.
- Download the .par file for the I/O PLL Reconfiguration design example to your working directory. Accept the license agreement when prompted.

- On the Design Example page, click the More Settings button.
- Click the Design Examples Search Locations tab.
- In the Design examples search directories box, specify the working directory to store your downloaded design example .par file from step 3.
- Under Find Options, specify the following settings:
- In Load from, select Downloaded design examples.
- In Family, select Agilex.
- In Intel Quartus Prime version, select 19.4.
- In the Development kit, select Agilex F-series Transceiver-SoC Development Kit.
- In the design example list, select the I/O PLL Reconfiguration design. The ? symbol indicates that the design is not yet validated for the current Intel Quartus Prime software version.

Downloaded Agilex I/O PLL Reconfiguration Design



Click Next, and then click Finish. The I/O PLL Reconfiguration design extracts to the working directory and opens in the Intel Quartus Prime software.

Accessing Online Design Examples

You can create a new project based on a design example that you access from an online repository. To use this method, you may need to specify a proxy server for access and the download path.

To create a new project based on an online design example, follow these steps:

1. Start the Intel Quartus Prime Pro Edition software.
2. Click File ► Open Example Project. The Design Example page of the New Project Wizard opens.
3. Under What is the working directory for this project?, specify the directory location to store your project files.
4. Click the More Settings button. The Options dialog box opens with the Internet Connectivity tab open by default.

Internet Connectivity

Web browser

☐ Use custom web browser instead of system default

Path:

Proxy server

☒ Access online design examples using a proxy server

Address:

Port:

User name:

Password:

5. If your internet connection requires a proxy server (using VPN), turn on the Access online design examples using a proxy server option, and then specify your proxy Address, Port, User name, and Password. If your internet connection does not require a proxy server, skip this step.
6. On the Design Example Search Locations tab, specify the Download path for download of the design example .par file.
7. Click OK.
8. Under Find Options, specify the following settings:
 - In Load from, select Online design examples.
 - In Family, select Agilex.
 - In the Intel Quartus Prime version, select 22.4.
 - In the Development kit, select Intel Agilex F-Series FPGA Development Kit DK-DEV-AGF014EA.
9. In the design example list, select the Agilex -NIOVS OCM to OCM design.

Online Agilex -NIOVS OCM to OCM Design

Find Options

Load from:

Family:

Intel Quartus Prime version:

Development kit:

Legend

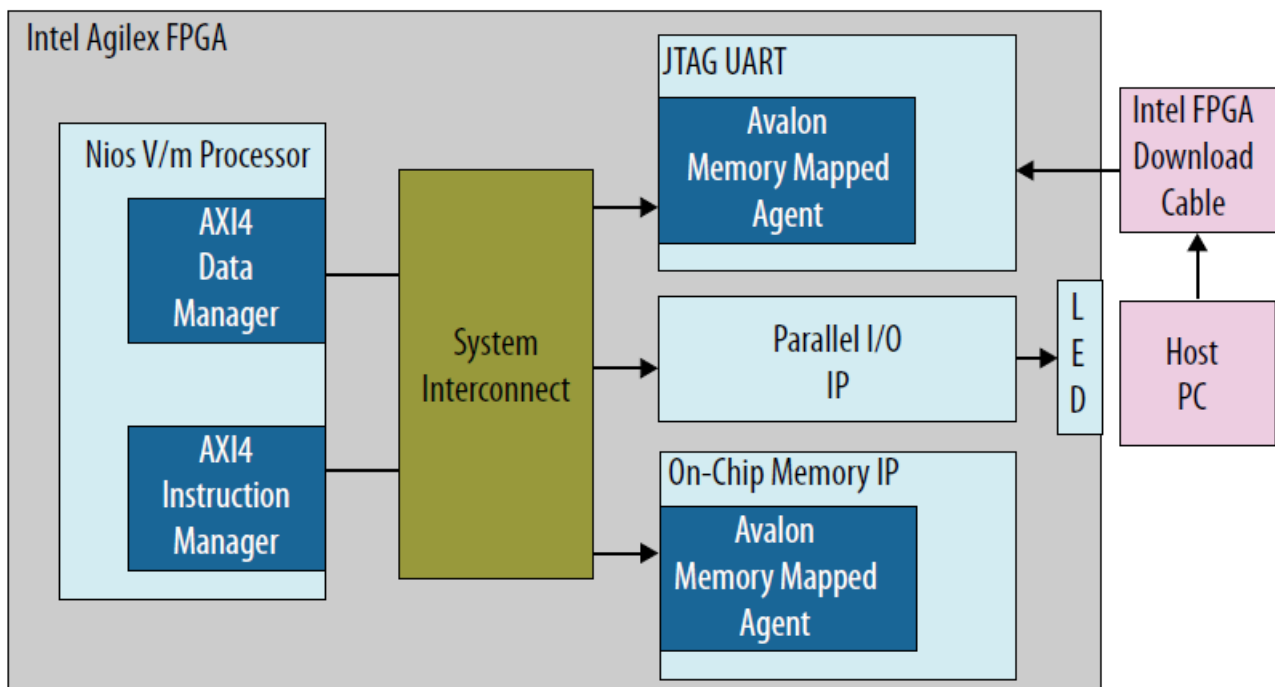
	Load From	Design Name
☒	Online	Agilex - NIOVS OCM to OCM

- Click Next, and then click Finish. The Agilex -NIOVS OCM to OCM design extracts to the working directory and opens in the Intel Quartus Prime software.

Using the Board-Aware Flow in Platform Designer

The board-aware flow is fully integrated within the Platform Designer GUI to simplify and accelerate the process of appropriately configuring IP and systems for a target board. Platform Designer allows you to create a system that targets a specific development board, rather than only targeting a specific FPGA device. When you target a specific development board, Platform Designer is aware of the target board (board-aware) which simplifies the IP parameterization, pin assignments, and export of interfaces for the system. The board-aware flow uses IP presets together with a board definition file that specifies the details of a target board. You can use (and reuse) the board definition and IP presets to automatically include the appropriate IP pin assignments, parameters, and exported interfaces for the target development board during system generation. The following example board-aware flow example creates an LED system based on the PIO Intel FPGA IP design example.

PIO IP-Based LED Design Block Diagram



- **Step 1:** Specify a Target Board for the Project
- **Step 2:** Create a New Board File
- **Step 3:** Create IP Presets for the Board
- **Step 4:** Create a Design Using Board and Preset Files
- **Step 5:** Compile and Verify the Design
- **Step 6:** Configure the Board with Software

Step 1: Specify a Target Board for the Project

To create an Intel Quartus Prime project that targets a specific board containing the target FPGA device, follow these steps:

1. Start the Intel Quartus Prime Pro Edition software.
2. Click File ► New Project Wizard. If the Introduction page appears, click Next.
3. Under Project Settings, enter `pio_led` as the working directory, the name of the project, and the top-level design entity.

New Project Wizard

Project Settings

Select the type of project to create.

☒ Empty project

Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.

☐ Design example

Create a project from an existing design example. You can choose from design examples installed with the Intel Quartus Prime software, or download design examples from the [Design Store](#).

Specify the properties of the project.

What is the working directory for this project?
C:/designs/pio_led

What is the name of this project?
pio_led

What is the name of the top-level design entity for this project? exactly match the entity name in the design file.
pio_led

☐ This project uses a Partition Database (.qdb) file for the root p

[Use Existing Project Settings...](#)

Device

Board

- Click the Board tab below the settings you just specified. The Board tab allows you to target a specific FPGA device board, rather than just a specific FPGA device.
- Under Find Options, specify the following filters:
- Family—select Agilex.
- Development Kit—select Intel Agilex F-Series FPGA Development Kit DK-DEV-AGF014EA.
- Vendor—select Intel.

Board Tab Settings

Device Board

Select the board/development kit you want to target for compilation.

Find Options

Family: Agilex

Development Kit: Intel Agilex F-Series FPGA Development Kit DK-DEV-AGF014EA

Vendor: Intel

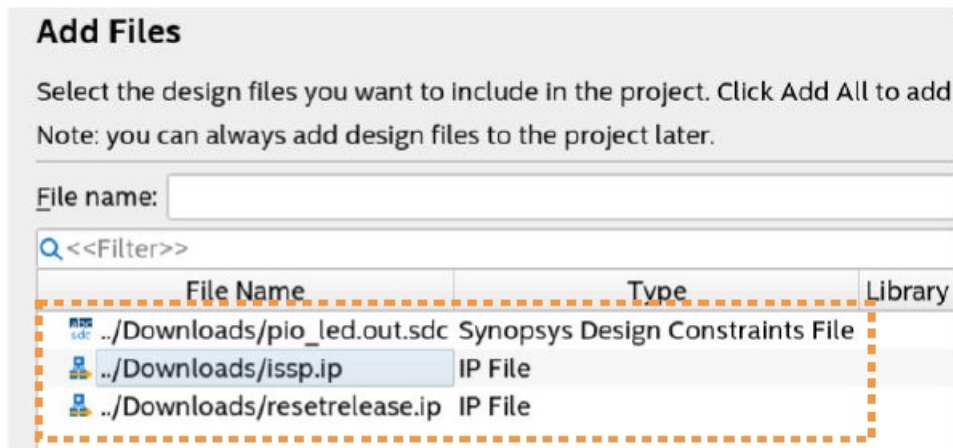
☐ Show only boards/development kits with design examples

Filter: Device

	Development Kit	Family
✓	Intel Agilex F-Series FPGA Development Kit DK-DEV-AGF014EA	Agilex

- Click the Intel Agilex F-Series FPGA Development Kit in the list. The board details appear in the right pane.
- Click Next. The Add Files page appears.
- Next to File name, click browse (...) to add the pio_led.out.dc, issp. ip, and reset-release.ip files that support this application note, as Download Supporting Files describes.

Adding IP and Constraint Files to Project



- Click Next. the EDA page appears. Retain the default settings and click Next again to view the Summary page. The Summary page displays the details of your project based on the board and other options you specified.
- When you are done viewing the Summary, click Finish. The PIO_LED project opens in the Intel Quartus Prime software.

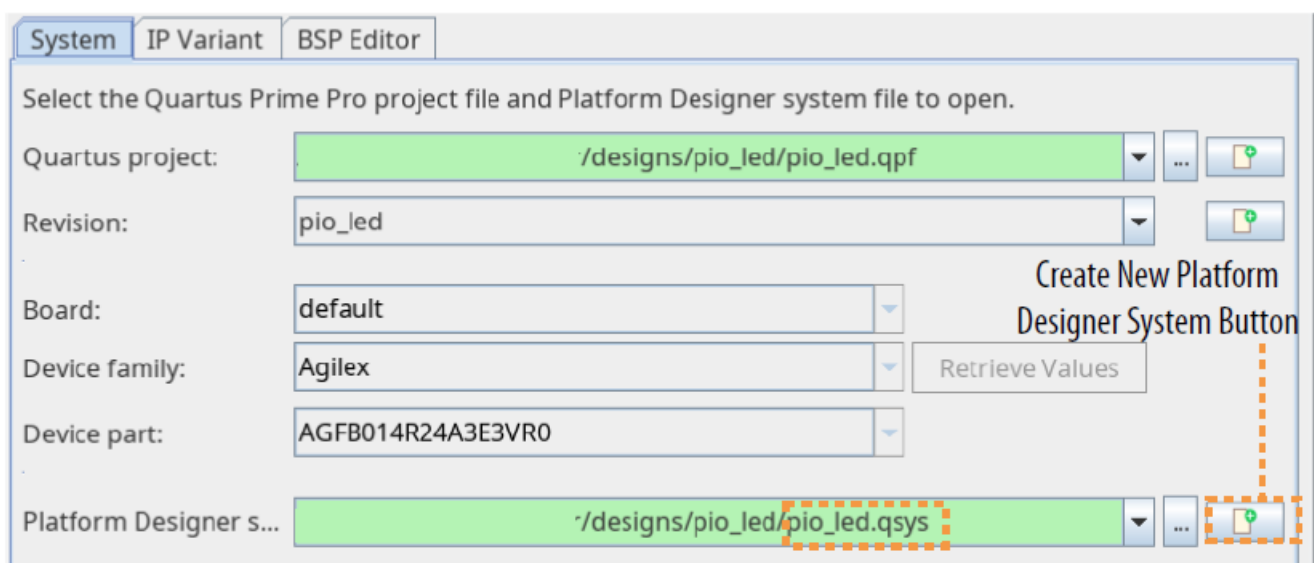
Step 2: Create a New Board File

You can define a board file that specifies the details of the target board. You can reuse this file with other projects that target the same board.

To create a new board file for the target board, follow these steps:

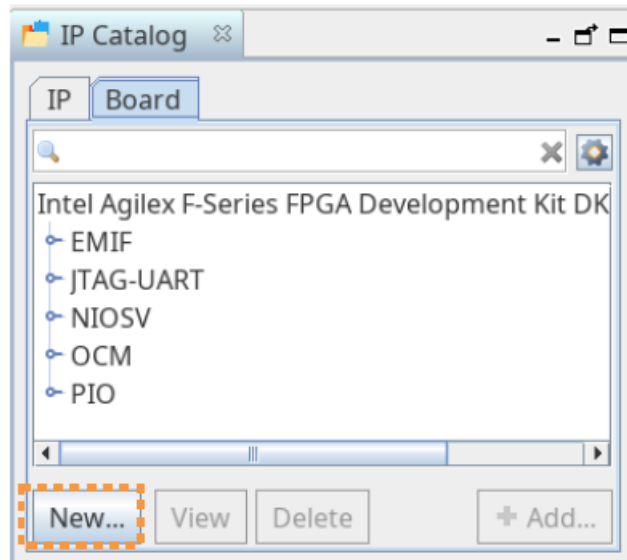
1. Click Tools ► Platform Designer. The Open System dialog box displays the project's name, Revision, Board, Device family, and Device part. Click Retrieve Values if this field requires re-synchronization.
2. For the Platform Designer system setting, click the Create new platform designer system button, specify the pio_led.qsys File Name, and click Create.

Open System Dialog Box



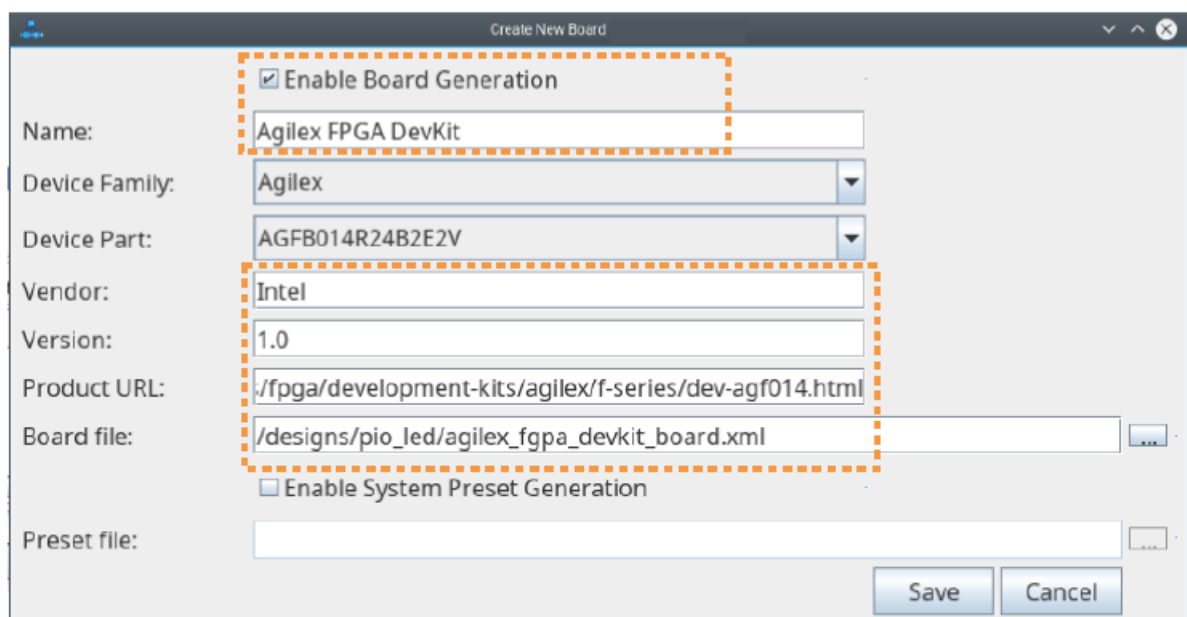
- In IP Catalog, click the Board tab. The Board Catalog lists any existing board files. By default, the preset path is: <quartus>\ip\altera\board_preset_files.

Board Catalog



- Click New. The Create New Board dialog box appears.
- Specify the following settings for the new board definition:
 - Enable Board Generation—retain enabled setting.
 - Name—enter Agilex FPGA DevKit.
 - Device Family—retain the Agilex setting.
 - Device Part—retain the AGFB014R24B2E2V setting.
 - Vendor—enter Intel as the board vendor.
 - Version—enter 1.0 as the board file version.
 - Product URL—Add Agilex F-Series FPGA Development Kit page URL.
 - Enable System Preset Generation—leave disabled.
 - Board file—click browse (...) and enter the name of the new board file as agilex_fpga_devkit_board.xml. Click OK. The _board.xml extension automatically appends to the file name that you specify.

Create New Board Dialog Box

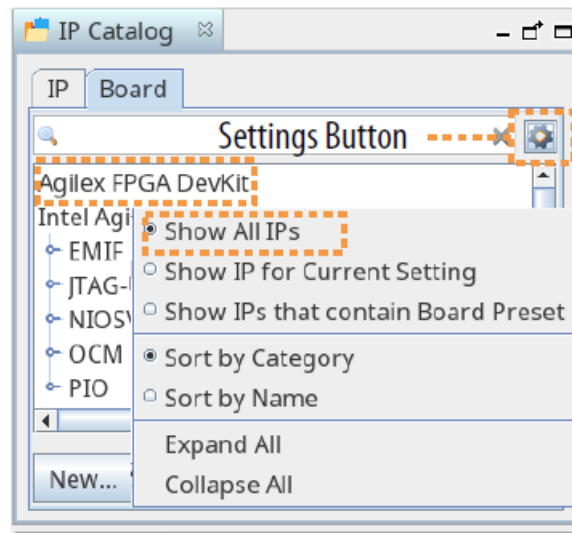


- In the Create New Board dialog box, click Save. The agilex_fpga_devkit_board.xml file saves to the project

directory.

- To view the new board in the Board Catalog, click the Settings button on the right side of the search field, and select Show All IPs. Because there are no IPs associated with the Agilex FPGA DevKit board file, the Board Catalog displays only the board name. This Agilex FPGA DevKit board definition is now available for any projects targeting the same board.

Agilex FPGA DevKit Board Visible in Board Catalog

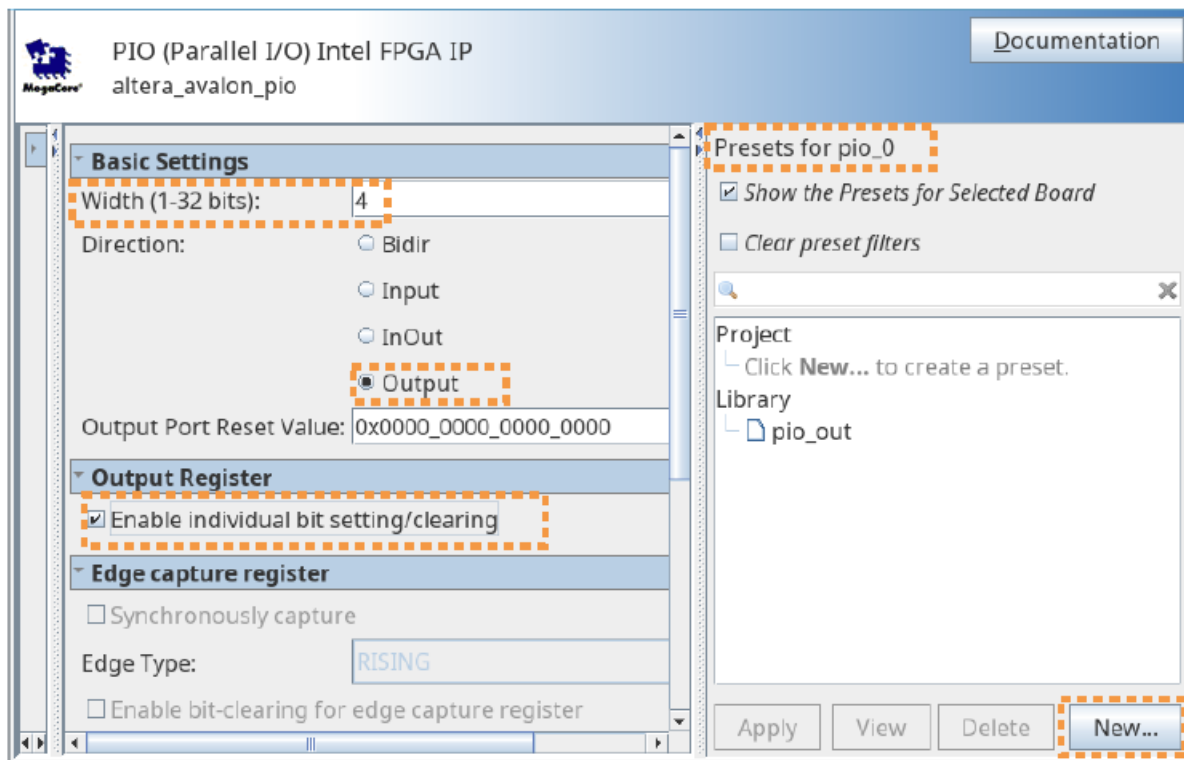


Step 3: Create IP Presets for the Board

To create preset parameter settings that are appropriate for the target board, follow these steps:

1. In Platform Designer IP Catalog, click the IP tab and type pio to search for the PIO (Parallel I/O) Intel FPGA IP.
2. Double-click the PIO (Parallel I/O) Intel FPGA IP name in IP Catalog. The IP parameter editor appears.
3. Specify the following parameter values in the PIO (Parallel I/O) Intel FPGA IP parameter editor:
 - Width (1-32 bits)—enter 4.
 - Direction—select Output.
 - Output Register—turn on Enable individual bit setting/clearing.

PIO (Parallel I/O) Intel FPGA IP Parameter Editor



- In the Presets pane, click the New button. The New Preset dialog box appears (alternatively, click View ► Presets).
- Specify the following options to identify the new preset:
- Preset name—enter pio_led.
- Preset description—enter presets for pio outputs.
- Category—enter PIO.
- **Note:** The Board option displays the target board from the project settings.

New Preset Dialog Box



- View the Parameter Settings tab. The parameter values already reflect the parameter values that you set in 3 on page 15.
- To specify pin location and I/O standard assignments for the preset, click the Pin Assignments tab.
- Enable the external_connection interface checkbox and type led in the Exported Name cell. The led_export[n] prefix automatically replaces all port names of the interface.
- For the led_export[n] ports, specify the following Pin Locations and I/O Standard.
- led_export[0]—Pin location PIN_B31, IO standard 1.2V
- led_export[1]—Pin location PIN_D31, IO standard 1.2V

- led_export[2]—Pin location PIN_A30, IO standard 1.2V
- led_export[3]—Pin location PIN_C30, IO standard 1.2V

Pin Assignments Tab of Presets Pane

Parameter Settings | **Pin Assignments**

Select pin assignments to include in the preset:

Pin Constraint File

Signal Name	Exported Name	Pin Location	IO Standard
☐ clk			
☐ reset			
☐ s1			
☒ external_connection	led		
☒ export[4]			
☒ external_connection.export[0]	led_export[0]	PIN_B31	1.2 V
☒ external_connection.export[1]	led_export[1]	PIN_D31	1.2 V
☒ external_connection.export[2]	led_export[2]	PIN_A30	1.2 V
☒ external_connection.export[3]	led_export[3]	PIN_C30	1.2 V

Preset file:

Save

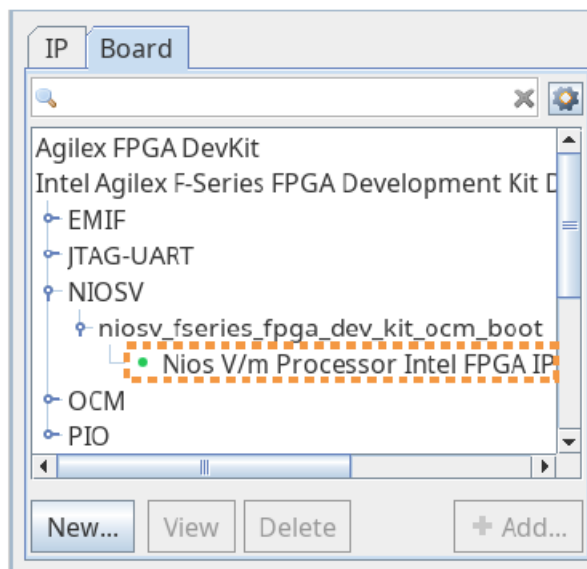
- **Note:** Alternatively, you can populate the pin assignments by specifying the provided pio_pin.tcl file for the Pin Constraint File option.
- Click the Save button to save the IP preset file.
- Click Finish to generate the PIO IP and add to the system.
- **Note:** You can now reuse this preset file for projects targeting this board and IP.

Step 4: Create a Design Using Board and Preset Files

Once you create board and preset files, you can use these files to create a design that is appropriately configured for the target board. The following steps describe adding a new instance of the PIO (Parallel I/O) Intel FPGA that derives parameters from the pio_led preset and targets the same Intel Agilex F-Series Development Kit board.

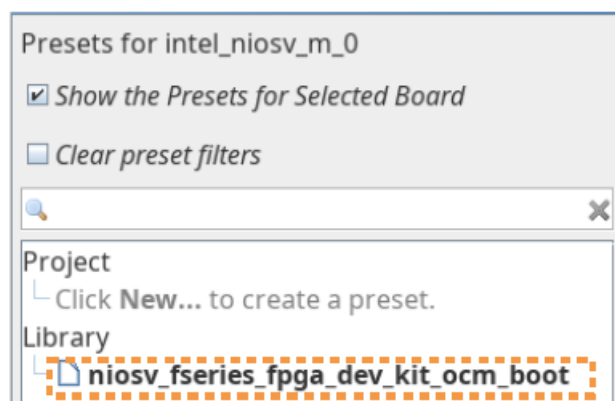
1. View the Clock Bridge Intel FPGA IP, Reset Bridge Intel FPGA IP, and PIO Intel FPGA IP components in Platform Designer's System View.
2. Right-click the PIO Intel FPGA IP (pio_0) in the System View, and then click Remove.
3. In the IP Catalog, click the Board tab.
4. Under the Intel Agilex F-Series FPGA Development Kit DK-DEV-AGF014EA board, click NIOSV to expand the niosv_fseries_fpga_dev_kit_ocm_boot IP preset name. Click the IP preset name to show Nios V/m Processor Intel FPGA IP.

IP and Presets in Board Tab



- Double-click Nios V/m Processor Intel FPGA IP. The IP Parameter Editor opens.
- In the parameter editor Preset tab, double-click the preset name to apply to the selected IP (or click Apply in the Preset tab). The parameter editor displays the Preset tab with the active `niosv_fseries_fpga_dev_kit_ocm_boot` preset in bold.

Active Preset in Bold



- Click Finish to add the preset IP to the system.
- Repeat steps 4 through 6 to add the following IP with presets to the system. For the PIO Intel FPGA IP, the external connection interface exports automatically per the `pio_led` preset.

IP Components with Presets to Add to System

Component Category	IP Name	IP Preset Name
PIO	PIO (Parallel I/O) Intel FPGA IP	<code>pio_led</code>
OCM	On-Chip Memory (RAM or ROM) Intel FPGA IP	<code>ocm_fseries_fpga_dev_kit</code>
JTAG-UART	JTAG UART Intel FPGA IP	<code>juart_fseries_fpga_dev_kit</code>

Make connections between the following component ports in the System View tab by clicking inside an open

connection circle. When you make a connection, Platform Designer changes the connection line to black, and fills the connection circle. Clicking a filled-in circle removes the connection:

System Connections

Source Component/Signal	Target Component/Signal
clock_in.out_clk	intel_niosv_m_0.clk pio_0.clk onchip_memory2_0.clk1 jtag_uart_0.clk
reset_in.out_reset	intel_niosv_m_0.reset pio_0.reset onchip_memory2_0.reset1 jtag_uart_0.reset
jtag_uart_0.irq	intel_niosv_m_0.platform_irq_rx
intel_niosv_m_0.instruction_manager	intel_niosv_m_0.dm_agent onchip_memory2_0.s1
intel_niosv_m_0.data_manager	intel_niosv_m_0.timer_sw_agent intel_niosv_m_0.dm_agent pio_0.s1 onchip_memory2_0.s1 jtag_uart_0.avalon_jtag_slave

Completed System Connections

Use	Connections	Name	Description	Export	Clock
☒		☐ clock_in ▶ in_clk ▶ out_clk	Clock Bridge Intel F... Clock Input Clock Output	clk	exported clock_in...
☒		☐ reset_in ▶ clk ▶ in_reset ▶ out_reset	Reset Bridge Intel ... Clock Input Reset Input Reset Output	Double reset [clk] Double [clk]	clock_i... [clk] [clk]
☒		☐ intel_niosv_m_0 ▶ clk ▶ reset ▶ platform_irq_rx ▶ instruction_manager ▶ data_manager ▶ timer_sw_agent ▶ dm_agent	Nios V/m Processor... Clock Input Reset Input Interrupt Receiver AXI4 Manager AXI4 Manager Avalon Memory Map... Avalon Memory Map...	Double Double Double Double Double Double	clock_i... [clk] [clk] [clk] [clk] [clk] [clk]
☒		☐ pio_0 ▶ clk ▶ reset ▶ s1 ▶ external_connection	PIO (Parallel I/O) I... Clock Input Reset Input Avalon Memory Map... Conduit	Double Double Double led	clock_i... [clk] [clk] led
☒		☐ onchip_memory2_0 ▶ clk1 ▶ s1 ▶ reset1	On-Chip Memory (... Clock Input Avalon Memory Map... Reset Input	Double Double Double	clock_i... [clk1] [clk1]
☒		☐ jtag_uart_0 ▶ clk	JTAG UART Intel FP... Clock Input	Double	clock_i...

- To clear the remaining system warnings, assign the missing base addresses by clicking System ► Assign Base Addresses.
- Click File ► Save to save the system.
- Click the Generate ► Generate HDL and generate the HDL for the system using the default settings in the Generation dialog box.
- When HDL generation completes, close Platform Designer.

Step 5: Compile and Verify the Design

Follow these steps to compile the top-level design that includes the pio_led Platform Designer system.

1. After Platform Designer HDL generation is complete, click Processing ► Start Compilation. The Compiler runs for approximately 15 minutes, depending on your system, and generates the SOF programming file following successful compilation.
2. When the full compilation is complete, click Assignments ► Pin Planner to verify the following appropriate pin assignments are implemented during compilation:

Verifying Location Assignments in Pin Planner

Named: *		Edit: X	
Node Name	Direction	Fitter Location	I/O Standard
in clk_clk	Input	PIN_C40	1.2 V
out led_export[0]	Output	PIN_B31	1.2 V
out led_export[1]	Output	PIN_D31	1.2 V
out led_export[2]	Output	PIN_A30	1.2 V
out led_export[3]	Output	PIN_C30	1.2 V
in reset reset	Input	PIN_P45	1.2 V

Step 6: Configure the Board with Software

In the next phase of the design, you program software to the board and generate the ELF file, the Board Support Package, and the Application Project File. This stage requires the pio.c file. You can then program the board and observe the output from the JTAG terminal. Refer to the Agilex – Nios V PIO LED Toggle Design example design for a complete design containing a board support package, application project file, and ELF file to observe output from the JTAG terminal. For more information about BSP and Application file generation, refer to the Nios V Embedded Processor Design Handbook.

Related Information

Nios V Embedded Processor Design Handbook

Document Revision History of AN 988: Using the Board-Aware Flow in the Intel Quartus Prime Pro Edition Software

Document Version	Intel Quartus Prime Version	Changes
2023.01.09	22.4	Minor revisions throughout for style and clarity.
2022.12.12	22.4	The initial release of the document.

Documents / Resources

	Intel AN 988 22.4 Quartus Prime Pro Edition Software [pdf] User Guide AN 988 22.4 Quartus Prime Pro Edition Software, AN 988, 22.4 Quartus Prime Pro Edition Software, Prime Pro Edition Software, Pro Edition Software, Edition Software, Software
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References

- intel [1. About the Nios® V Embedded Processor](#)
- intel [FPGA Software Download Center](#)
- intel [Supporting Design Example Files for AN 988 using the Board-Aware Flow: in the Intel® Quartus® Prime Pro Edition Software](#)
- intel [1. Answers to Top FAQs](#)
- intel [1. Answers to Top FAQs](#)

- [intel 1. Answers to Top FAQs](#)
- [intel Intel® Agilex™ 7 FPGA F-Series Development Kit](#)
- [intel Intel ISO 9001:2015 Registrations](#)
- [intel FPGA Design Store | Intel](#)

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