intel AN-963 MAX 10 Hitless User Guide

intel AN-963 MAX 10 Hitless

Contents

Intel® MAX® 10 DD Feature Option Devices Hitless Update Implementation Guidelines

Introduction

Intel® MAX® 10 devices offer the hitless update feature, which provides you the capability and flexibility to control the state of the I/O pins during the internal flash image update and reconfiguration of an Intel MAX 10 device. All of the I/O pins can remain stable without any disruption throughout the hitless update process. This feature also

allows the Intel MAX 10 device to behave as a system controller when monitoring and controlling critical signals without interruption.
Intel MAX 10 devices with DD feature option offer an extension of hitless update with internal JTAG interface, in addition to using external JTAG pins. To support internal JTAG interface hitless update, the behavior of nSTATUS, nCONFIG, and CONF_DONE pins behavior are modified from controllable and observable to observable only.
These guidelines help you implement the hitless update using internal JTAG interface.
This feature is only supported by Intel MAX 10 devices with DD feature option. For hitless update using external JTAG pins, refer to AN 904: Intel MAX 10 Hitless Update Implementation Guidelines.

Related Information

- AN 904: Intel MAX 10 Hitless Update Implementation Guidelines
  Provides the hitless update implementation guidelines using external JTAG pins.
- Intel MAX 10 FPGA Device Overview
  Provides the Intel MAX 10 device ordering information.

Hitless Update using Internal JTAG Interface

Create an Intel Quartus® Prime user design that enables internal JTAG interface by including JTAG WYSIWYG atom. All four JTAG signals (TCK, TDI, TMS, and TDO) in the JTAG WYSIWYG atom need to be routed out to ensure the internal JTAG interfaces of Intel MAX 10 devices function correctly. Prior to hitless update, user design must first program the CFM with application image through FPGA core fabric and drive all I/Os to the desired state. Reconfiguration is triggered using user logic with Dual Configuration Intel FPGA IP.
Related Information
Design Store: Intel MAX 10 JTAG Secure Unlock

Stages of Intel MAX 10 Hitless Update using Internal JTAG Interface

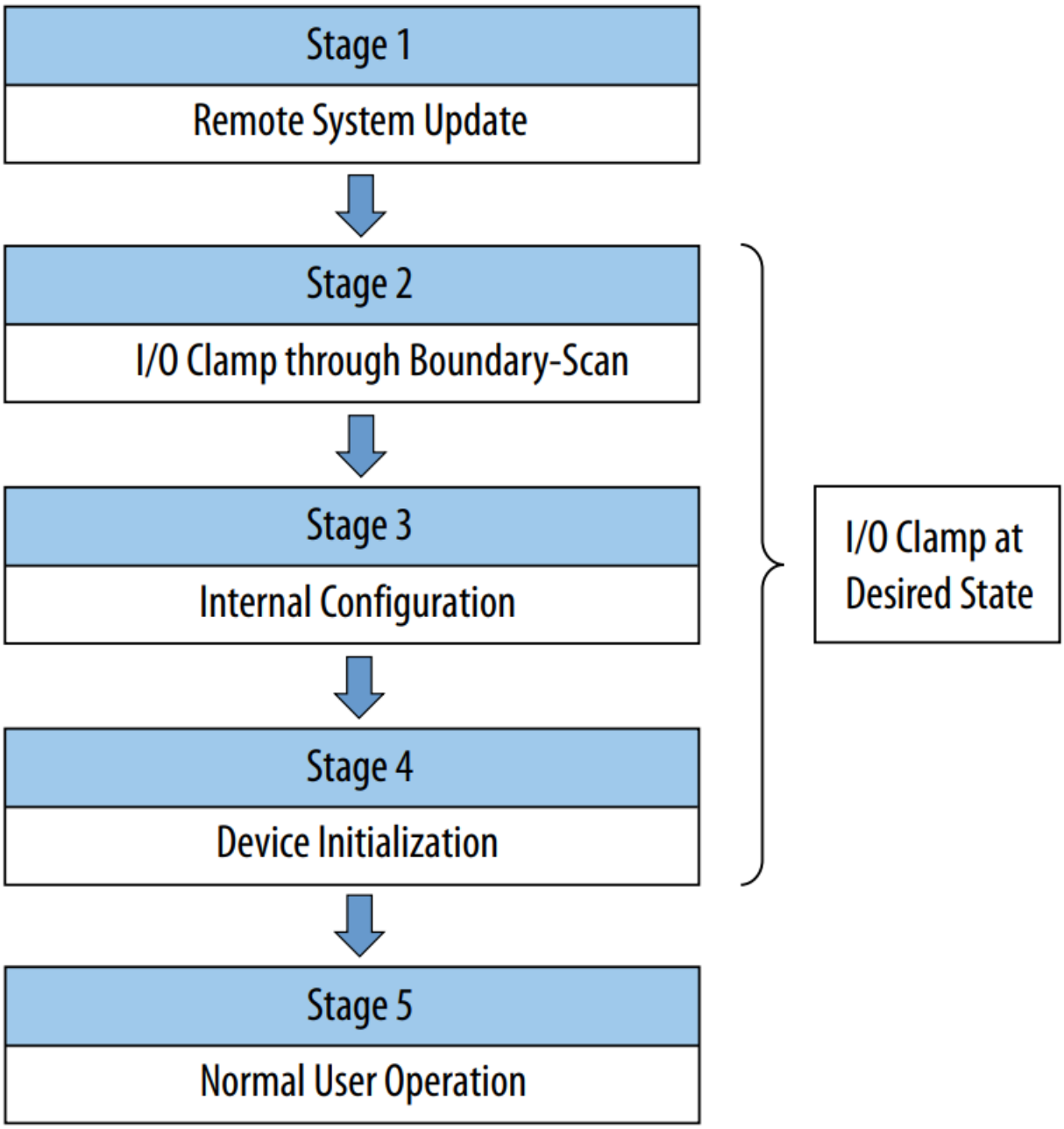
At a high level, the implementation flow for Intel MAX 10 hitless update using internal JTAG interface may be categorized into five stages:

- Stage 1: Remote system update (RSU). Intel MAX 10 device is programmed with RSU image and enter user mode. Intel MAX 10 device internal flash (CFM and UFM) is then updated remotely with new application image while the design is still running.
- Stage 2: I/O clamp through boundary-scan. The I/O state is setup based on realtime I/O state sampling or by shifting in predefined boundary-scan data using internal JTAG interface to perform I/O clamp at the desired state. You may store critical design registers or finite state machine (FSM) values and the desired I/O state values into the UFM before performing Stage 2.
- Stage 3: Internal configuration. The I/Os remain in the desired state while the reconfiguration takes place from the internal flash into CRAM.
- Stage 4: Device initialization. After internal configuration is complete, the I/Os are released after entering user

mode. You can unload the I/O state data, register, or FSM value that previously stored in the user flash memory, force the user design logic into a correct state to output the same desired I/O value as the clamping state, to ensure no disruption to the system.

- Stage 5: Normal user operation.

Figure 1. Stages of Intel MAX 10 Hitless Update using Internal JTAG Interface



Internal JTAG Hitless Update Implementation Flow

To implement the internal JTAG hitless update, perform the following steps on the user design:

1. Execute SAMPLE/PRELOAD JTAG instruction using internal JTAG interface, shift in the desired I/O state or maintain the existing I/O state from the boundary scan.
2. Execute CLAMP instruction using internal JTAG interface.
3. Trigger reconfiguration using user logic with Dual Configuration Intel FPGA IP.
4. Wait for device initialization and internal configuration (refer to the Internal Configuration Time for Intel Devices

(Uncompressed .rbf) and Internal Configuration Time for Intel Devices (Compressed .rbf) tables in the Intel FPGA Device Datasheet for internal configuration time).

5. After entering user mode, you are recommended to perform JTAG TAP RESET to release the I/O clamp. Alternately, you may execute BYPASS instruction using internal JTAG interface to release the I/O clamp.

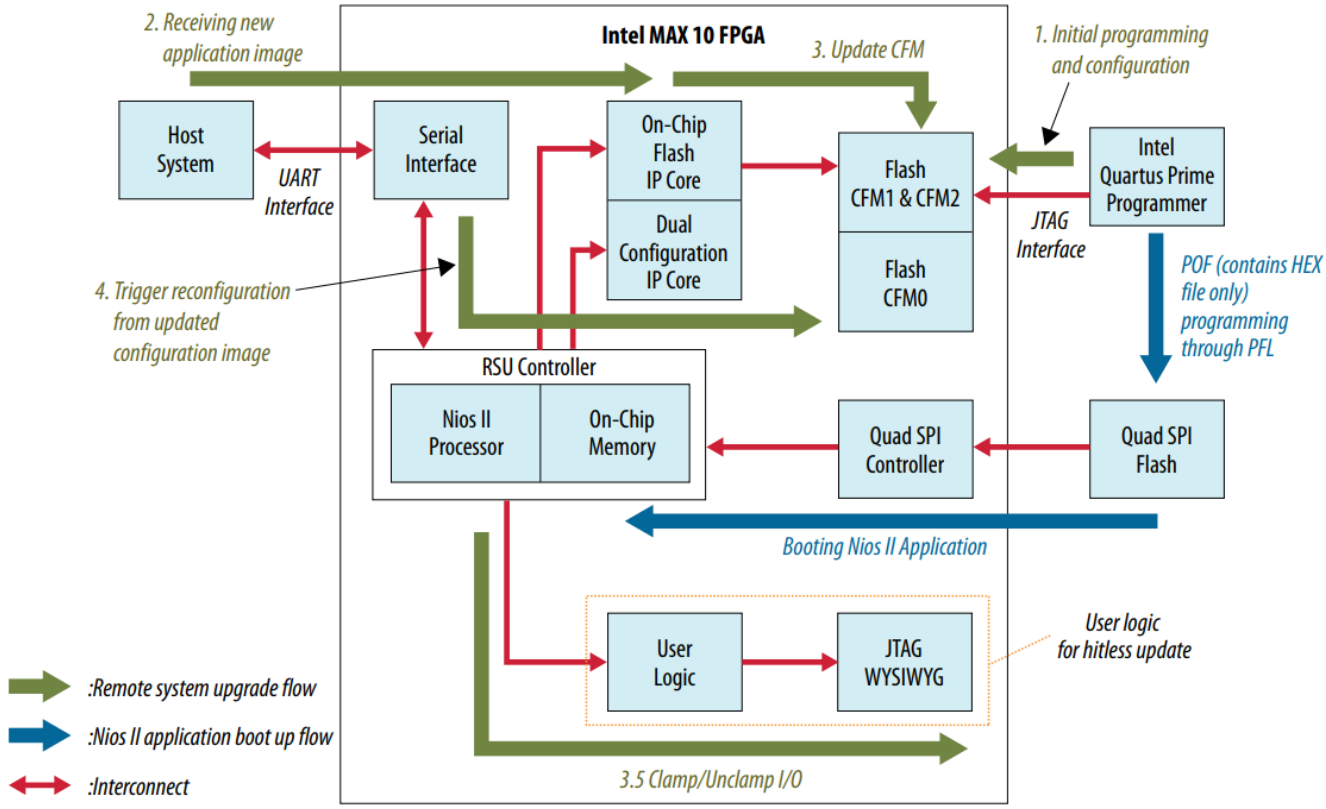
Related Information

- **Intel MAX 10 FPGA Configuration User Guide**
- **Intel MAX 10 FPGA Device Datasheet**

Internal JTAG Hitless Update using Remote System Update Design Example

You may leverage the Intel MAX 10 remote system update (RSU) solution to implement internal JTAG hitless update. On top on the Intel MAX 10 RSU reference design example, you are required to add a user logic that connects to internal JTAG interface to support hitless update.

Figure 2. Intel MAX 10 RSU Reference Design Block Diagram with User Logic for Internal JTAG Hitless Update



Note: You need to prepare your own user logic for hitless update.

The recommended design flow is as follows:

1. Power up Intel MAX 10 device, configure device with remote system update design, and bring the device to user mode.
2. Run Intel MAX 10 RSU to update application image into CFM1 or CFM2 using On Chip Flash Intel FPGA IP.
3. Drive all I/Os to the desired state.
4. Nios® II should interact with user logic to clamp I/Os prior to reconfiguration. The user logic clamps I/Os using internal JTAG interface.

a. Execute SAMPLE/PRELOAD JTAG instruction to capture all output state into capture register of boundary-scan chain.

b. Execute CLAMP instruction to clamp all I/Os in their current state.

c. Nios II reads completion status from user logic, then triggers reconfiguration with Dual Configuration Intel FPGA IP.

d. Wait for reconfiguration to complete.

e. After entering user mode, you are recommended to perform JTAG TAP RESET to release the I/O clamp. Alternately, you may execute BYPASS instruction using internal JTAG interface to release the I/O clamp.

Note: JTAG TAP RESET can be performed by putting the test access port (TAP) controller in reset state by driving the TDI and TMS pins high and toggle the TCK pin for at least 5 clock cycles before initialization.

5. At this point, the new application image is updated and I/O is not clamp. You can observe the Intel MAX 10 RSU design LED behavior that indicates the different image loaded into the device.

Related Information

- **AN 741: Remote System Upgrade for Intel MAX 10 FPGA Devices over UART with the Nios II Processor**
- **Intel MAX 10 FPGA Configuration User Guide**
- **AN 904: Intel MAX 10 Hitless Update Implementation Guidelines**
  Provides the hitless update implementation guidelines using external JTAG pins.

JTAG Instructions

Table 1. JTAG Instructions

Instruction Name	Instruction Binary	Description
SAMPLE/ PRELOAD	00 0000 0101	• Permits an initial data pattern to be an output at the device pins. • Allows you to capture and examine a snapshot of signals at the device pins if the device is operating in normal mode.
EXTEST	00 0000 1111	• Forces test pattern at the output pins and capture the test results at the input pins. • Allows you to test the external circuitry and board-level interconnects.
BYPASS	111111 1111	• Places the 1-bit bypass register between the TDI and TDO pins. • Allows the BST data to pass synchronously through target devices to adjacent devices during normal device operation.
CLAMP	000000 1010	• Places the 1-bit bypass register between the TDI and TDO pins. The 1-bit bypass register holds I/O pins to a state defined by the data in the boundary-scan register. • Allows the BST data to pass synchronously through target devices to adjacent devices if device is operating in normal mode.

Related Information

Intel MAX 10 JTAG Boundary-Scan Testing User Guide

Provides the complete reference to the JTAG instructions supported by Intel MAX 10 devices.

Document Revision History for AN 963: Intel MAX 10 Hitless Update Implementation Guidelines Using Internal JTAG Interface

Document Version	Changes
2022.04.21	Added CLAMP in the *JTAG Instructions* table.
2022.01.07	Initial release.

Documents / Resources

	intel AN-963 MAX 10 Hitless [pdf] User Guide MAX 10 Hitless, MAX 10, Hitless, AN-963, 710498, AN-963 MAX 10 Hitless