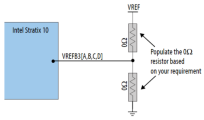
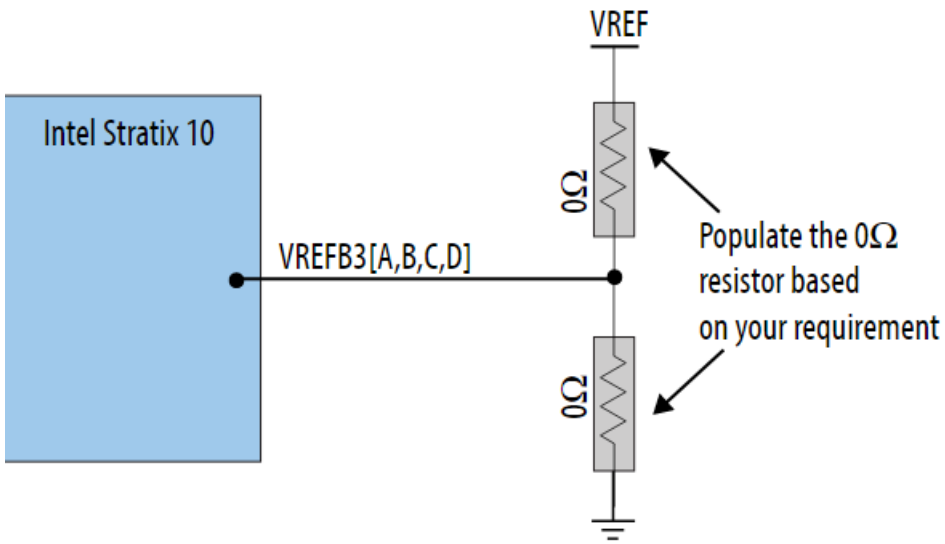


intel AN 921 Device Migration Guidelines for Stratix 10 HF35 Package User Guide

Contents

intel AN 921 Device Migration Guidelines for Stratix 10 HF35 Package



Introduction

This application note will focus on the device migration between the HF35 package of Intel® Stratix® 10 GX 400 and Intel Stratix 10 SX 400 to Intel Stratix 10 GX 650 and Intel Stratix 10 SX 650.You can gain more logic element resources for larger design or reduce the logic element resources for cost saving through device migration. The following sections provide details about the device migration overview, migration considerations, and the pre-design steps for a successful device migration.

Related Information

- Intel Stratix 10 Device Datasheet
- Intel Stratix 10 General Purpose I/O User Guide
- Intel Stratix 10 Device Pin-Out Files
- Intel Stratix 10 Device Family Pin Connection Guidelines

Device Migration Overview

You can perform device migration between the HF35 package of the Intel Stratix 10 GX 400 and Intel Stratix 10 SX 400 to Intel Stratix 10 GX 650 and Intel Stratix 10 SX 650. You must consider the following device migration guidelines during the early board designing stage to ensure the migration compatibility.

- Power rail design
  - VCCIO pins for the devices
  - VREFB3[A,B,C,D]N0
- I/O pin function
  - Pin location and pin function
  - I/O features such as I/O standards and its supported features
- Intel Quartus® Prime design
  - Migratable Intel Quartus Prime design per I/O pin function availability.

The board design must include the features planned for the target device migration to avoid board re-designing. The following table provides an overview of the migratable and non-migratable I/O banks. I/O banks 2K, 2L, 2M, 2N, and 3B are fully compatible and you can freely migrate the design to the target device. However, banks 3A and 3D are partially compatible as only selected I/O standard and I/O pin count are supported.

Table 1. Migratable and Non-Migratable I/O Banks

I/O Bank	Migration Condition
2K	Fully compatible for all single-ended and differential I/O standard.
2L	
2M	
2N	
3A	Partially compatible for single-ended non-voltage reference signals and non-LVDS SERDES differential I/O (LVDS I/O standard works only for a dedicated reference clock pin).
3B	Fully compatible for all single-ended and differential I/O standards.
3C	Incompatible.
3D	Partially compatible for single-ended non-voltage reference signals and non-LVDS SERDES differential I/O (LVDS I/O standard works only for a dedicated reference clock pin). Only 30 I/O pins are available in the HF35 package of the Intel Stratix 10 GX 400 and Intel Stratix 10 SX 400 devices.

The table below shows the supported I/O standard comparison between the HF35 package of Intel Stratix 10 GX 400/Intel Stratix 10 SX 400 and Intel Stratix 10 GX 650/Intel Stratix 10 SX650 devices. The supported feature for each I/O standard is available in the Intel Stratix 10 General Purpose I/O User Guide.

Table 2. The I/O Standard Comparison between the HF35 package of Intel Stratix 10 GX 400/Intel Stratix 10 SX 400 and Intel Stratix 10 GX 650/Intel Stratix 10 SX 650 Devices

Bank	Intel Stratix 10 GX 400/SX 400 (HF35 Package)	Intel Stratix 10 GX 650/SX 650 (HF35 Package)
3A	Supports 1.2V, 1.5V, and 1.8V single-ended and differential I/O standards, except for the EMIF applications and LVDS SERDES functions. The LVDS I/O standard is supported only in a dedicated reference clock pin for the reference clock function.	Supports 1.2V, 1.5V, and 1.8V single-ended and differential I/O standards as stated in the *Intel Stratix 10 General Purpose I/O User Guide*.
3B	Supports 1.2V, 1.5V, and 1.8V single-ended and differential I/O standards as stated in the *Intel Stratix 10 General Purpose I/O User Guide*.	Supports 1.2V, 1.5V, and 1.8V single-ended and differential I/O standards as stated in the *Intel Stratix 10 General Purpose I/O User Guide*.
3C	Supports 3.0V and 3.3V single-ended I/O standard only.	Supports 1.2V, 1.5V, and 1.8V single-ended and differential I/O standards as stated in the *Intel Stratix 10 General Purpose I/O User Guide*.
3D	Supports 1.8V single-ended I/O and differential I/O standards, except for the EMIF and LVDS functions. The LVDS I/O standard is supported only in a dedicated reference clock pin for the reference clock function.	Supports 1.2V, 1.5V, and 1.8V single-ended and differential I/O standards as stated in the *Intel Stratix 10 General Purpose I/O User Guide*.

There are a total of 30 pins in bank 3D of the HF35 package in the Intel Stratix 10 GX 400/SX400 which are fanned out to package. The following table shows the pin location comparison for the HF35 package of the Intel Stratix 10 GX 400/SX 400 and Intel Stratix 10 GX 650/SX 650 devices. You must fully understand the compatibility of the I/O pins for migration before deciding which pin to use in your design.

Table 3. Pin Location Comparison for the HF35 package of the Intel Stratix 10 GX 400/SX 400 and Intel Stratix 10 GX 650/SX 650 Devices

Intel Stratix 10 GX 400/SX 400 (HF35 Package)		Intel Stratix 10 GX 650/SX 650 (HF35 Package)	
Pin Name/Function	**Pin Location**	**Pin Name/Function**	**Pin Location**
IO	M5	IO	M5
IO	M6	IO	M6
IO	L8	IO	L8
IO	K7	IO	K7
IO	M3	IO	M3
IO	N3	IO	N3
IO	L7	IO	L7
IO	M7	IO	M7
IO	N1	IO	N1
IO	M1	IO	M1
IO	H5	IO	H5
IO	G5	IO	G5
continued...			

Intel Stratix 10 GX 400/SX 400 (HF35 Package)		Intel Stratix 10 GX 650/SX 650 (HF35 Package)	
IO	N5	IO	N5
IO	N4	IO	N4
IO	J6	IO	J6
IO	K5	IO	K5
IO	P1	IO	P1
IO	P2	IO	P2
IO	K6	IO	K6
IO	L5	IO	L5
IO	P3	IO	P3
IO	P4	IO	P4
IO	H4	IO	H4
IO	H3	IO	H3
IO	R1	IO	R1
IO	R2	IO	R2

IO	K4	IO	K4
IO	J4	IO	J4
IO	R4	IO	R4
IO	R5	IO	R5
VREFB3DN0	M8	VREFB3DN0	M8
NC	J1	IO	J1
NC	H1	IO	H1
NC	T2	IO	T2
NC	T3	IO	T3
NC	L3	IO	L3
NC	L4	IO	L4
NC	T4	IO	T4
NC	T5	IO	T5
NC	J3	IO	J3
NC	J2	IO	J2
NC	U1	IO	U1
NC	U2	IO	U2
NC	L2	IO	L2
NC	M2	IO	M2
NC	V1	IO	V1
continued...			

Intel Stratix 10 GX 400/SX 400 (HF35 Package)		**Intel Stratix 10 GX 650/SX 650 (HF35 Package)**	
NC	W1	IO	W1
NC	K2	IO	K2
NC	K1	IO	K1

Related Information
Intel Stratix 10 General Purpose I/O User Guide

Hardware Design Guidelines

This section provides the hardware design guidelines with consideration of the device migration compatibilities covered in the previous section. As mentioned earlier, the I/O banks for 2K, 2L, 2M, 2N, and 3B are fully compatible for device migration. Similarly, power pins such as VCC, VCCPT, and VCCA_PLL are fully compatible and migratable between these devices. For more information, refer to the guidelines listed in Intel Stratix 10 Device Family Pin Connection Guidelines.
Related Information

Power Pin Migration Guidelines

The following table describes the power pin design guidelines for the design migration. The focused power pins are VCCIO I/O banks 3A, 3B, 3C, and 3D which require predesign consideration.

Table 4. Power Pin Board Design Guidelines

Pin	I/O Bank	Board Design Guidelines
Power Pin (VCCIO)	3A	The bank 3A can support the equivalent VCCIO voltage level from the migration device. Therefore, the power rail connection can remain. You may power down the unused I/O banks by connecting their VCCIO pin to GND.
	3B	The bank 3B can support the equivalent VCCIO voltage level from the migration device. Therefore, the power rail connection can remain. You may power down the unused I/O banks by connecting their VCCIO pin to GND.
	3C	The supported VCCIO voltage level of the HF35 package of the Intel Stratix 10 GX 400 and SX 400 is 3.0V or 3.3V. It is not migratable to the HF35 package of the Intel Stratix 10 GX650 or SX650 device, as it supports only 1.2V, 1.5V, and 1.8V. The same conditions apply when migrating from the HF35 package of the Intel Stratix 10 GX650 or SX650 device to the HF35 package of the Intel Stratix 10 GX400 or SX400 device. Your board design must have an option to connect the VCCIO to GND when the I/O bank is not in use after the migration or the power rail changes to the desired VCCIO voltage level after the migration. You must pre-design the power rail by changing the 0Ω resistor options for the voltage selection as shown in Figure 1 on page 9.
	3D	The VCCIO3D for the HF35 package of the Intel Stratix 10 GX400 or SX400 device supports only 1.8V. If the target migration device is also using the same voltage level, it is directly migratable. Otherwise, you must pre-design the power rails by changing the 0Ω resistor options for the voltage selection as shown in Figure 2 on page 9.

Figure 1. VCCIO Pin for Bank 3C

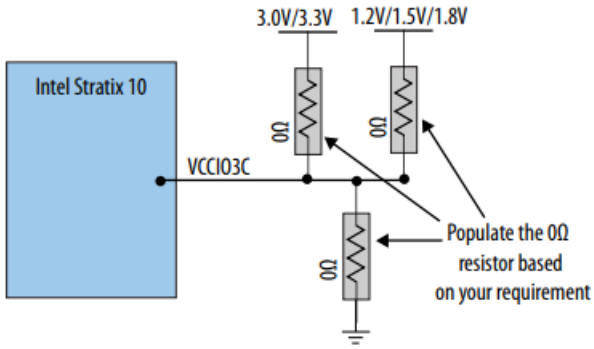
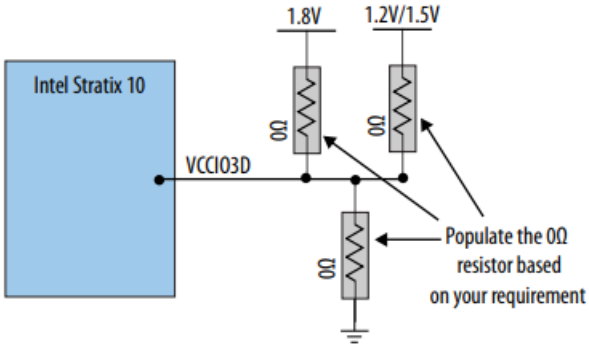


Figure 2. VCCIO Pin for Bank 3D



I/O Pins Migration Guidelines

The following table lists the design guidelines for GPIO pins for banks 3A, 3B, 3C, and 3D.

Table 5. I/O Pin Board Design Guidelines

Pin	I/O Bank	Board Design Guidelines
GPIO Pin	3A	The GPIO pins for bank 3A in the HF35 package of the Intel Stratix 10 GX400 or SX400 device supports single-ended differential I/O standard at 1.2V, 1.5V, and 1.8V. The mini-LVDS, RSDS, and LVDS I/O standards are supported only in dedicated clock pins, for reference clock purpose only. The pin and its function can be migrated to the HF35 package of the Intel Stratix 10 GX650 or SX650 device. If the bank 3A in the HF35 package of the Intel Stratix 10 GX650 or SX650 device is used for EMIF or LVDS SERDES in GPIO, then it is not migratable to the HF35 package of the Intel Stratix 10 GX400 or SX400 device. Leave these pins as NC. For more information, refer to Figure 3 on page 10.
	3B	The GPIO pins for bank 3B support the same features between the HF35 package of the Intel Stratix 10 GX400 or SX400 device and the HF35 package of the Intel Stratix 10 GX650 or SX650 device. The design is fully compatible and migratable.
	3C	The bank 3C of the HF35 package of the Intel Stratix 10 GX400 or SX400 device supports only 3.0V or 3.3V. Therefore, it is not a direct migration to the HF35 package of the Intel Stratix 10 GX650 or SX650 device and vice versa. Leave the GPIO pin as NC when it is not migratable after device migration. Consider to place a 0Ω resistor for the ease to disconnect the connection or remove the interface component. For more information, refer to the Figure 3 on page 10.
continued...		

Pin	I/O Bank	Board Design Guidelines
		However, if you need to keep the I/O pin in your design after the device migration, you can design it as per Figure 4 on page 10. Place a level shifter which can level shift to the same voltage level as required by the GPIO pin. By implementing this design, you will be able to migrate those single-ended non-reference voltage I/O to the new target device.
	3D	The bank 3D of the HF35 package of the Intel Stratix 10 GX400 or SX400 device supports only 30 GPIO pins. Please refer to the Table 3 on page 5 to identify the migratable I/O pins if your design starts with the HF35 package of the Intel Stratix 10 GX650 or SX650 device. For the non-migratable pins, leave the pins as NC when your design starts with the HF35 package of the Intel Stratix 10 GX650 or SX650 device. For more information, refer to Figure 3 on page 10 . The GPIO pins for bank 3D in the HF35 package of the Intel Stratix 10 GX400 or SX400 device supports single-ended and differential I/O standards at 1.2V, 1.5V, and 1.8V. Mini-LVDS, RSDS, and LVDS I/O standards are only supported as a dedicated clock pin for the reference clock purpose only. These pins and their functions can be migrated directly or indirectly to the HF35 package of the Intel Stratix 10 GX650 or SX650 device. If the bank 3D in the HF35 package of the Intel Stratix 10 GX650 or SX650 device is used for EMIF or LVDS SERDES in GPIO, it is not migratable to the HF35 package of the Intel Stratix 10 GX400 or SX400 device. Leave these pins as NC. If you need to migrate the non-reference single-ended I/O from the HF35 package of the Intel Stratix 10 GX650 or SX650 device to the HF35 package of the Intel Stratix 10 GX400 or SX400 device as compatible pins with different voltage level, you may design the board as shown in Figure 5 on page 10.

Figure 3. GPIO Pin for Bank 3A

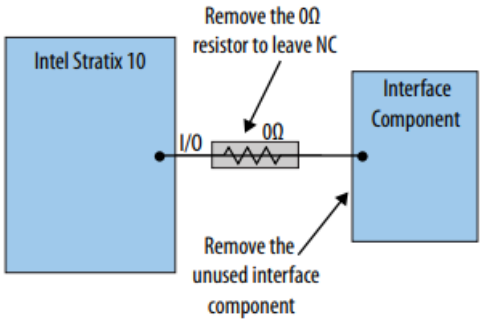


Figure 4. GPIO Pin for Bank 3C

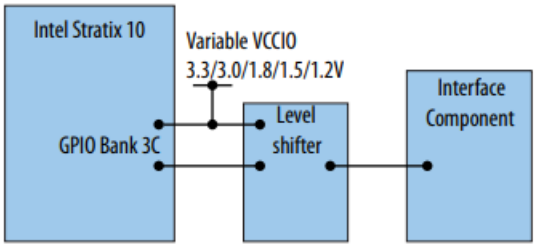
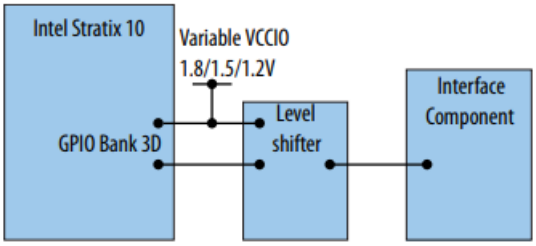


Figure 5. GPIO Pin for Bank 3D

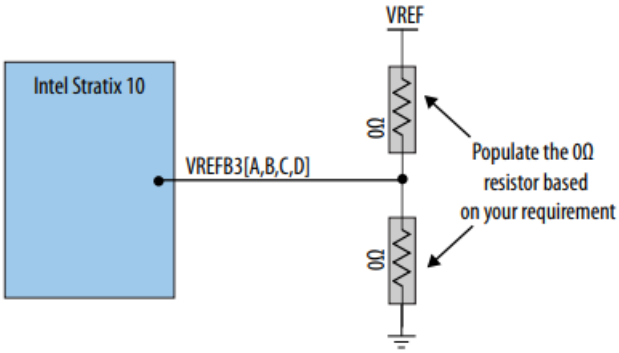


VREF Pin Migration Guidelines
This table describes the design migration guidelines for the VREF pins.

Table 6. VREF Pin Board Design Guidelines

Pin	I/O Bank	Board Design Guidelines
VREF Pin	3A	The VREF pin is compatible for migration. If VREF pins are not used, connect t hem either to the VCCIO in the bank where the pins reside or to GND.
	3B	The VREF pin is compatible for migration. If VREF pins are not used, connect t hem either to the VCCIO in the bank where the pins reside or to GND.
	3C	The VREFB3CN0 pin at the HF35 package of the Intel Stratix 10 GX400 or SX4 00 device must always be connected to GND, it is not migratable to the HF35 p ackage of the Intel Stratix 10 GX650 or SX650 device. If the VREF pin in the original board design uses the HF35 package of the Intel Stratix 10 GX650 or SX650 device, then you need to connect the pin to GND w hen migrating to the HF35 package of the Intel Stratix 10 GX400 or SX400 devi ce. You may design your board trace design with changeable resistor options a s shown in Figure 6 on page 11.
	3D	The VCCIO3D pin for the HF35 package of the Intel Stratix 10 GX400 or SX400 device only supports 1.8V. The other VCCIO voltage level such as 1.2V and 1.5 V are not supported. The VREF power rail must follow the I/O standard used. If VREF pins are not used, then connect them either to the VCCIO in the bank wh ere the pins reside or to GND.

Figure 6. VREF Pin Bank 3C

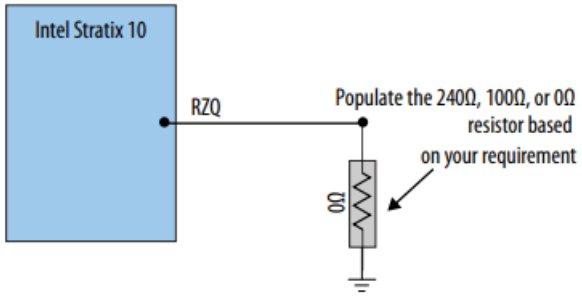


RZQ Pin Migration Guidelines
This table describes the design migration guidelines for the RZQ pin for banks 3[A, B, C, D].
Table 7. RZQ Pin Board Design Guidelines

Pin	I/O Bank	Board Design Guidelines
RZQ pin	3A	The RZQ pin for the bank 3C at the HF35 package of the Intel Stratix 10 GX400 or SX400 device must always be connected to GND, and it in not migratable to the HF35 package of the Intel Stratix 10 GX650 or SX650 device or vice versa. When using OCT for the banks 3A, 3B, and 3C, connect these pins to GND through either a 240-Ω or 100-Ω resistor, depending on the desired OCT impedance. For more information about the OCT schemes, refer to the *Intel Stratix 10 General Purpose I/O User Guide*.
	3B	
	3C	
	3D	
continued...		

Pin	I/O Bank	Board Design Guidelines
		When you do not use these pins as dedicated input for the external precision resistor or as I/O pins, leave these pins unconnected as recommended in the *Intel Stratix 10 Device Family Pin Connection Guidelines*.

Figure 7. RZQ Pin for Banks 3[A, B, C, D]



Related Information

- Intel Stratix 10 General Purpose I/O User Guide
- Intel Stratix 10 Device Family Pin Connection Guidelines

Intel Quartus Prime Software Design Migration

This section describes the migration of the Intel Quartus Prime design between the HF35 package of the Intel Stratix 10 GX400 or SX400 device and the HF35 package of the Intel Stratix 10 GX650 or SX650 device. This is achievable through the following methods:

- Method 1- Change the device OPN

In this method, you have the flexibility to change the location and pin assignments. From the pop-up window as shown in Figure 8 on page 13, select the YES button and the Intel Quartus Prime software will automatically assign the location assignments and ensure successful migration. If you intend to keep the existing assignments, select the NO button in the pop-up window and you can do the assignments manually later.

Figure 8. Removing Location Assignments

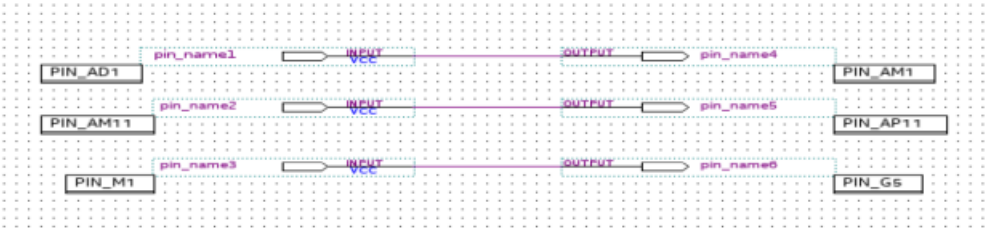
- Method 2 – Use the Migration UI

If the design is not flexible for assigned changes, using the Migration UI helps in checking the compatibility of the devices listed. You can assign the best device listed from the Compatible Migration Device List in the Migration Devices dialog box to the Selected Migration Devices list and compile the design until you can determine which device works best. You can also access the Pin Migration window from the Pin Planner. If you use this GUI, you can check the comparison table with the migration results between the devices chosen for migration which in return will provide ease in location assignments. In the application note, we will be focusing on the usage of the Migration UI and how to address the incompatibility issues between the two devices.

Migration via Migration GUI for 1SG040HH2F3512VG-1SG065HH3F3512VG Devices

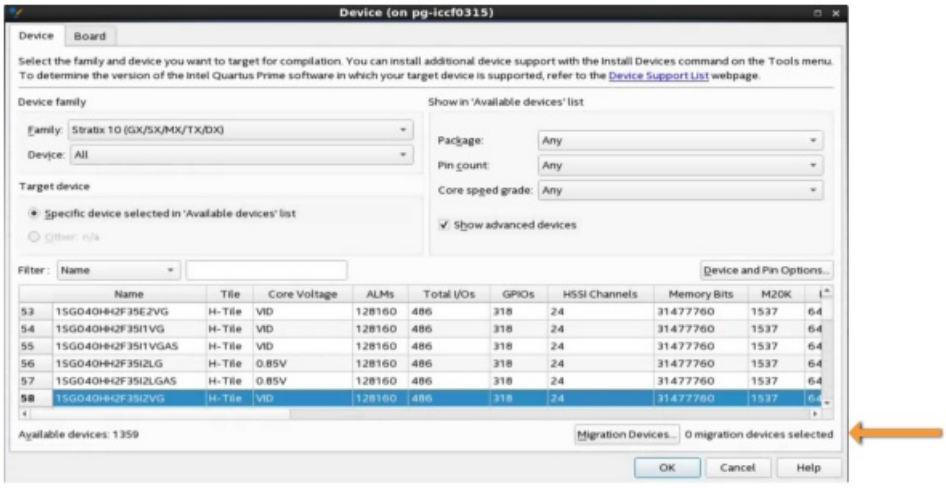
The designs used in this application note are basic designs to address the assignment issues. Figure 9 on page 14 is the snapshot of the design with the pin assignments.

Figure 9. Example Design with Pin Assignments



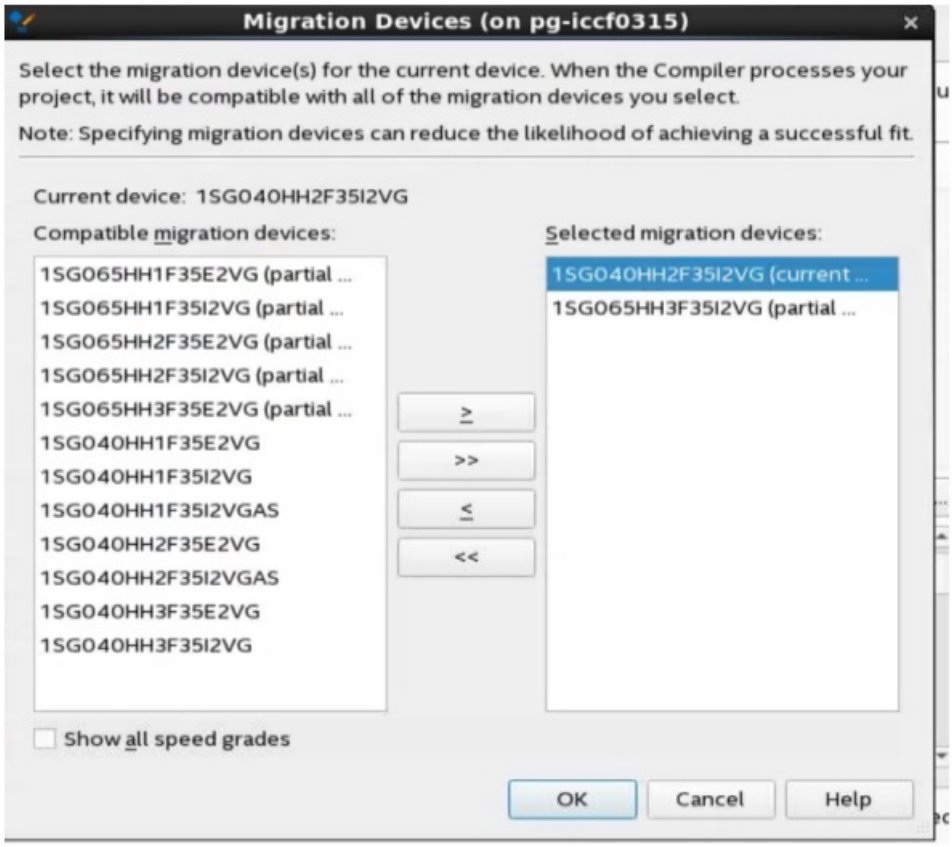
1. To start the device migration (1SG040HH2F3512VG-1SG065HH3F3512VG), right click on the device tab in the Project Navigator window. This will navigate you to a pop-up window as shown in the Figure 10 on page 14.

   Figure 10. Device Page



2. Instead of changing the device directly (which will allow the Intel Quartus Prime software to migrate to a new device by removing all the location assignments), select the Migration Devices tab located at the bottom right of Figure 10 on page 14. When you select the Migration Devices tab, a window will pop up as shown in Figure 11 on page 15.

Figure 11. Migration Devices



3. In the Migration Devices dialog box, click on >, >>, <, and << to move the migration devices between the Compatible migration devices list and the Selected migration devices list. A device name in the Selected migration devices list that is followed by the text (current device) indicates that the device is currently specified in the Available devices list in the Device dialog box.Compatible devices are listed in the Compatible migration devices list as partially or fully. Note: Partially migratable device list will be shown in the Intel Quartus Prime software version 20.2 onwards. If you want the Intel Quartus Prime software to display all compatible migration devices in the Compatible migration devices list regardless of a migration device's speed grade, then turn on the Show All Speed Grades option. If you want the Intel Quartus Prime software to display only the Compatible migration devices that have the same speed grade as the target device in the Compatible migration devices list, then turn off the Show all speed grades option.
4. After choosing the device for migration (1SG065HH3F3512VG), click OK and then you can check the assignment in the .qsf file too. If you do not specify at least one migration device in the Migration Devices dialog box, then the field displays 0 migration devices selected.

Figure 12. Set Global Assignment

5. After specifying the device to use as a migration device, compile the design. However, the device migration may cause additional constraints. Compilation may fail due to the additional constraints, and shows the error message as shown in Figure 13 on page 16. The errors appear because the devices are partially migratable. These errors prompt you to check the pin assignment in the Pin Planner as shown in Figure 14 on page 16.

Figure 13. Error Message

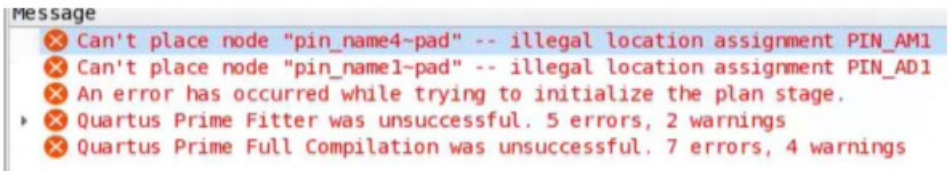


Figure 14. Pin Planner

	Node Name	Direction	Location	I/O Bank	Fitter Location	I/O Standard	Reserved
out	pin_name6	Output	PIN_G5	3D	PIN_G5	1.8 V	
in	pin_name1	Input	PIN_AD1	3C	PIN_AD1	1.8 V	
in	pin_name2	Input	PIN_AM11	3A	PIN_AM11	1.2 V	
in	pin_name3	Input	PIN_M1	3D	PIN_M1	1.8 V	
out	pin_name4	Output	PIN_AM1	3C	PIN_AM1	1.8 V	
out	pin_name5	Output	PIN_AP11	3A	PIN_AP11	1.2 V	
	<<new node>>						

6. For the non-migratable I/O pins, leave them as NC. You can set the unused I/O pins as input tri-state in the Intel Quartus Prime software. Go to the Device from the Project Navigator window and click on the Devices and Pin Options as shown in Figure 15 on page 16. In the Device and Pin Options window, under the Reserve all unused pins drop-down list, select As input tri-stated.

Figure 15. Devices Page

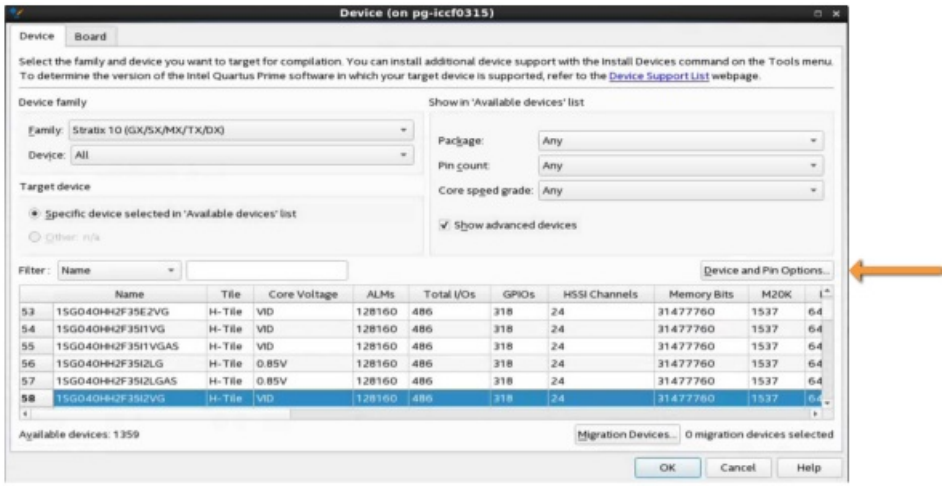
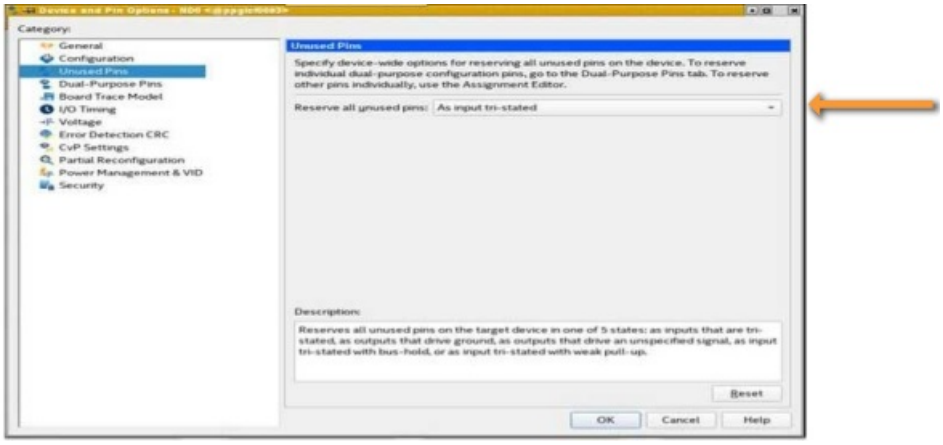


Figure 16. Devices and Pin Options



7. Remove the location assignment of the non-migratable pins as shown in Figure 17 on page 17 and compile the design.

Figure 17. Location Assignment

	Node Name	Direction	Location	I/O Bank	Fitter Location	I/O Standard
in	pin_name2	Input	PI...11	3A	PIN_AM11	1.2 V
in	pin_name3	Input	PIN_M1	3D	PIN_M1	1.8 V
out	pin_name6	Output	PIN_G5	3D	PIN_G5	1.8 V
out	pin_name5	Output	PI...11	3A	PIN_AP11	1.2 V
out	pin_name4	Output			PIN_AP22	1.8 V
in	pin_name1	Input			PIN_AL24	1.8 V
	<<new node>>					

Figure 18. Design Compilation

8. Alternatively, if you have the flexibility of changing the non-migratable pins and their I/O standards, then you can go the Pin Migration View window and check the pins compatibility and assign the pins accordingly.
9. The Pin Migration View window provides information about the suitability of the pins for device migration. You can open this window in the Pin Planner by clicking on View>Pin Migration View window. Select a pin in this view to display the following pin migration information:
   - Pin number
   - Migration devices
   - Pin finder
   - Migration result
   - Show only highlighted pins
   - Show migration differences
   - Export
   - Show commands

   You can access these commands by using a right click on the Pin Migration View window in the Pin Planner. You can see the difference and ease the pin assignment as shown in Figure 19 on page 18. You can look into the pin finder to find the pins according to the requirement as shown in Figure 20 on page 19.

Figure 19. Pin Migration View

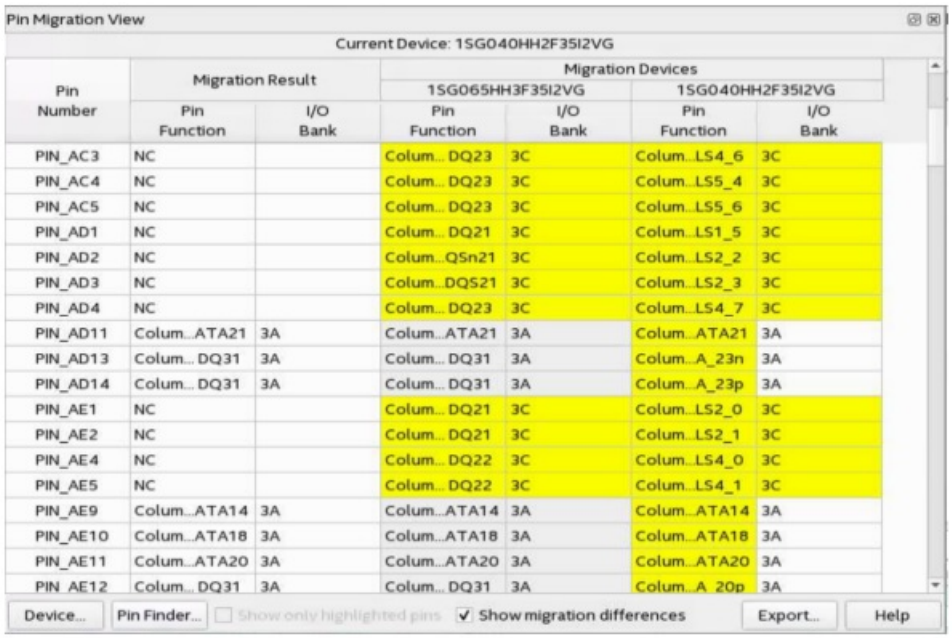
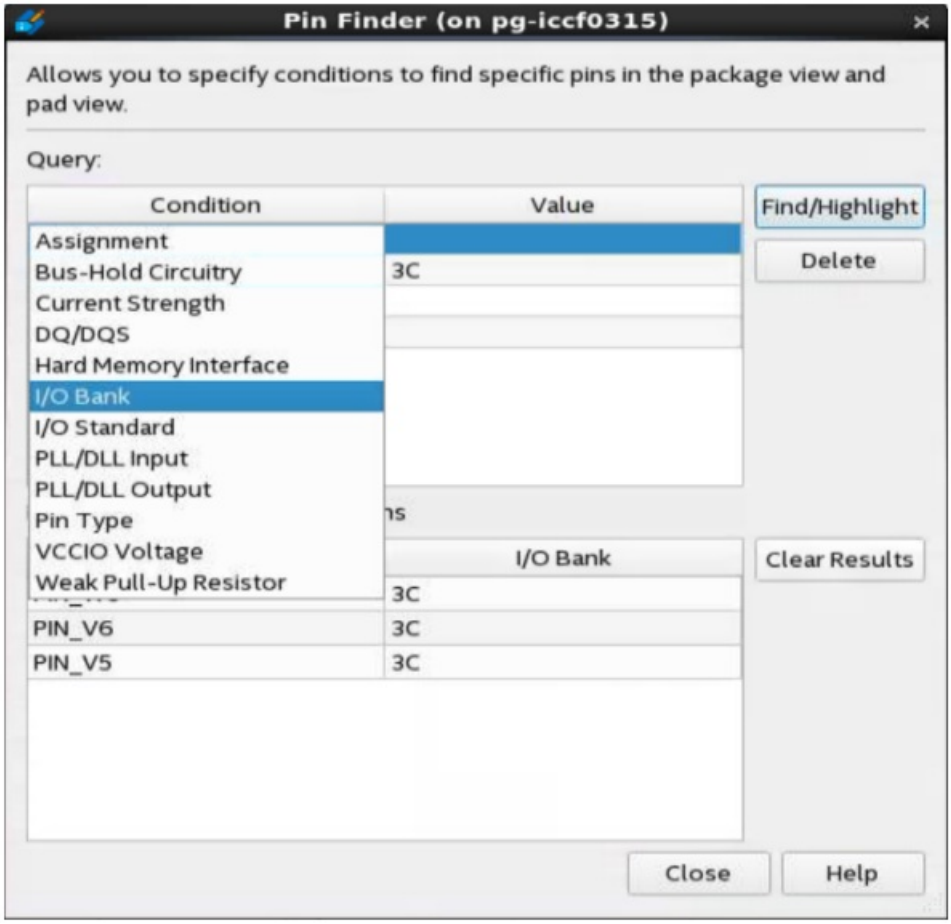


Figure 20. Pin Finder



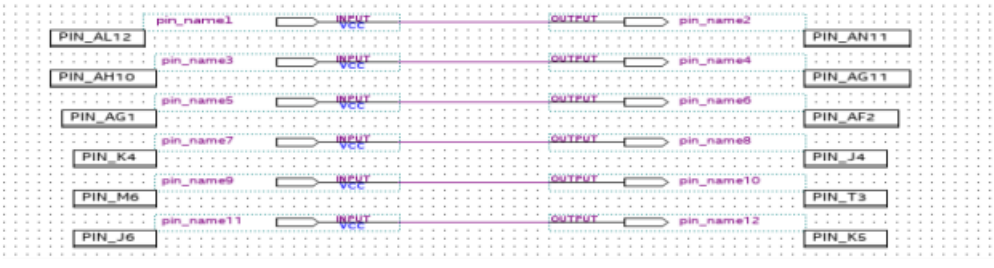
10. Change the pin assignment as shown in the Figure 21 on page 19 in the Pin Planner and compile the design. You will observe a successful compilation.

Figure 21. Pin Assignments

Migration Using Migration UI for 1SX065HH3F3512LG-1SX040HH2F3512LG Devices

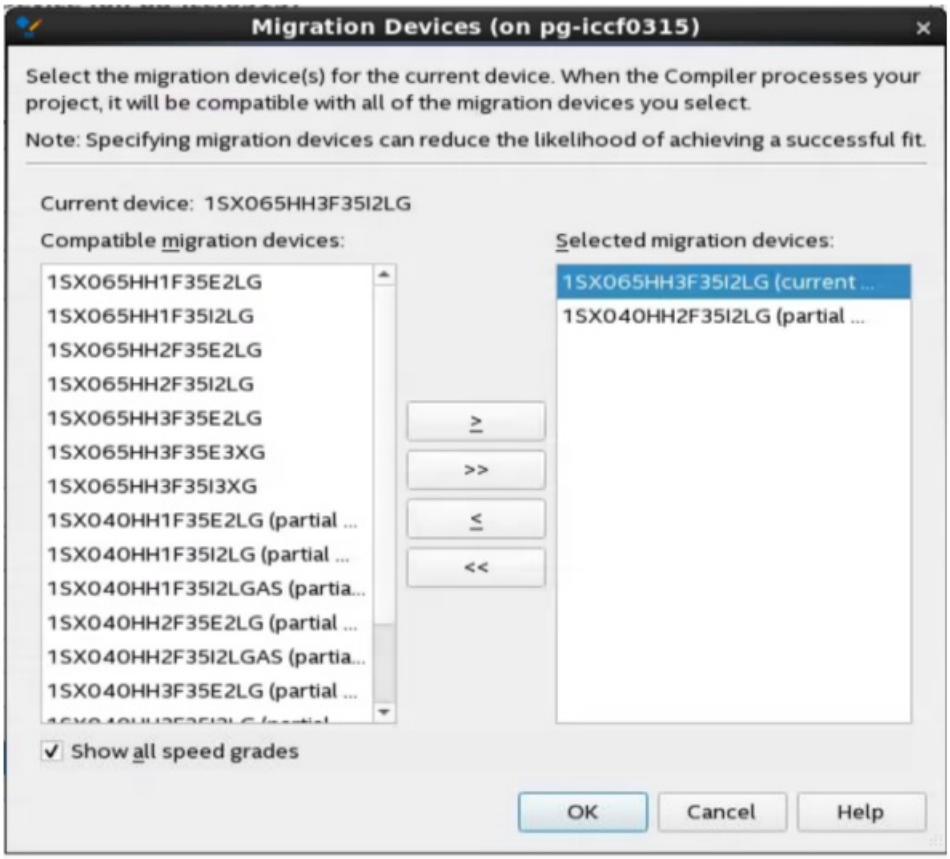
The example design used in this migration is a basic design to address the assignment and the I/O standard issues. The following figure shows the snapshot of the design with pin assignments.

Figure 22. Example Design with Pin Assignments



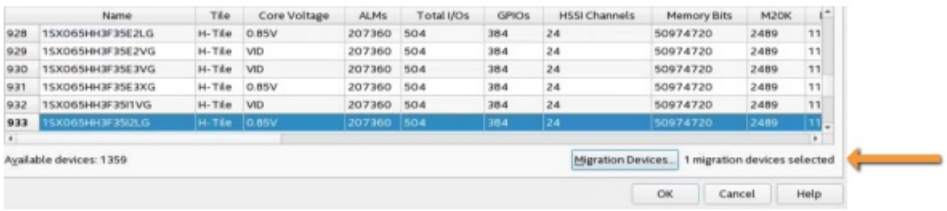
1. To start the migration between 1SX065HH3F3512LG-1SX040HH2F3512LG devices, right click on Device in the project navigator window. The Migration Devices window will pop up.

Figure 23. Migration Devices



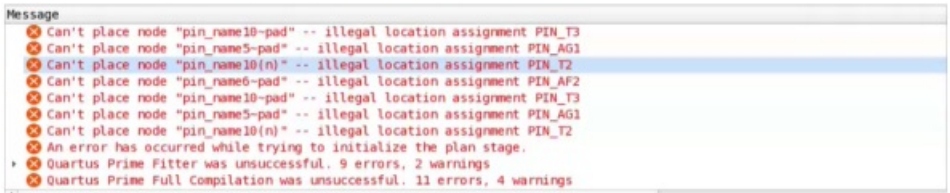
2. After choosing the device for migration (1SX040HH2F3512LG), click OK and then you can check the assignment in the .qsf file. If you do not specify at least one migration device in the Migration Devices dialog box, the field displays 0 Migration Devices Selected.

Figure 24. Set Global Assignment



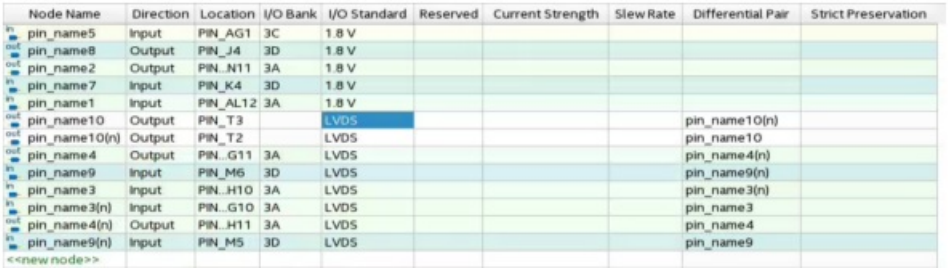
3. After specifying the device to migrate, follow the step mentioned earlier and make the non-migratable I/O as tri-stated and then compile the design.

Figure 25. Error Message



4. The compilation report shows errors related to the pin assignments location. Navigate to the Pin Planner and remove the location assignment of those pins to make them unused pins and they can be tri-stated.

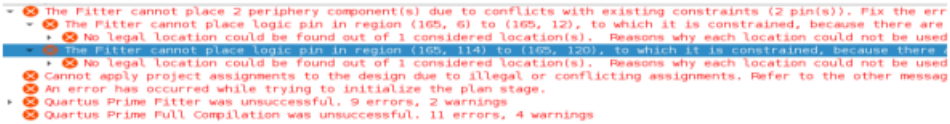
Figure 26. Pin Assignments



5. After removing the assignments, compile the design. You might encounter more compile errors that are

pointing you towards the non-compatibility I/O standard in bank 3A and 3D.

Figure 27. Compilation Error



6. After you have removed the assignments which show incompatibility as shown in Figure 28 on page 22, compiling the design again will give a successful compilation.
   Note: You can remove the unused logic design and disconnect the pins from the Intel Quartus Prime software. If you do not remove these unusable pins from the Intel Quartus Prime design, the software will automatically fit a location for these pins with the design connected.

   Figure 28. Pin Assignments

Node Name	Direction	Location	I/O Bank	Fitter Location	I/O Standard
pin_name6	Output			PIN_M6	1.8 V
pin_name11	Input	PIN_J6	3D	PIN_J6	1.8 V
pin_name1	Input	PIN_AL12	3A	PIN_AL12	1.8 V
pin_name10	Output			PIN_N1	1.8 V
pin_name5	Input			PIN_M5	1.8 V
pin_name4	Output	PIN_AG11	3A	PIN_AG11	1.8 V
pin_name9	Input			PIN_N3	1.8 V
pin_name8	Output	PIN_J4	3D	PIN_J4	1.8 V
pin_name3	Input			PIN_L5	LVDS
pin_name12	Output	PIN_K5	3D	PIN_K5	1.8 V
pin_name2	Output	PIN_AN11	3A	PIN_AN11	1.8 V
pin_name7	Input	PIN_K4	3D	PIN_K4	1.8 V
pin_name3(n)	Input			PIN_K6	LVDS
<<new node>>					

Figure 29. Design Compilation

7. Alternatively, if you have the flexibility of changing the non-migratable pins and their I/O standard, you can check the Pin Migration View window to obtain the information about the suitability of the pins for the device migration. You can change the pins accordingly for a successful compilation.

Document Revision History for AN921: Device Migration Guidelines for Intel Stratix 10 HF35 Package

Document Version	Changes
2020.09.11	Initial release.

Documents / Resources

	intel AN 921 Device Migration Guidelines for Stratix 10 HF35 Package [pdf] User Guide AN 921 Device Migration Guidelines for Stratix 10 HF35 Package, AN 921, Device Migration Guidelines for Stratix 10 HF35 Package, Guidelines for Stratix 10 HF35 Package, Stratix 10 HF35 Package, HF35 Package