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intel AN 769 FPGA Remote Temperature Sensing Diode User Guide

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Introduction

In modern electronic applications, especially applications that require critical temperature control, on-chip temperature measurement is crucial.

High performance systems rely on accurate temperature measurements for indoor and outdoor environments.

- Optimize performance
- Ensure reliable operation
- Prevent damage to components

The Intel® FPGA temperature monitoring system allows you to use third-party chips to monitor the junction temperature (TJ). This external temperature monitoring system works even while the Intel FPGA is powered down or not configured. However, there are several things you must consider when you design the interface between the external chip and the Intel FPGA remote temperature sensing diodes (TSDs).
When you select a temperature sensing chip, you would typically look at the temperature accuracy you want to achieve. However, with the latest process technology and a different remote TSD design, you must also consider the temperature sensing chip's built-in features to meet your design accuracy requirements.

By understanding the workings of the Intel FPGA remote temperature measurement system, you can:

- Discover common issues with temperature sensing applications.
- Select the most appropriate temperature sensing chip that meets your application needs, cost, and design time.

Intel strongly recommends that you measure the on-die temperature using local TSDs, which Intel has validated. Intel cannot validate the accuracy of external temperature sensors under various system conditions. If you want to use the remote TSDs with external temperature sensors, follow the guidelines in this document and validate the accuracy of your temperature measurement setup.

This application note applies to remote TSD implementation for the Intel Stratix® 10 FPGA device family.

Implementation Overview

The external temperature sensing chip connects to the Intel FPGA remote TSD. The remote TSD is a PNP or NPN diode-connected transistor.

- **Figure 1.** Connection Between Temperature Sensing Chip and Intel FPGA Remote TSD (NPN Diode)
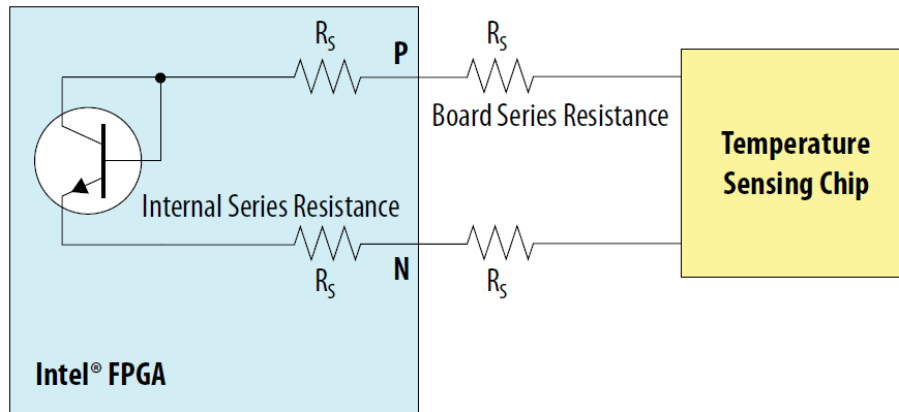
- **Figure 2.** Connection Between Temperature Sensing Chip and Intel FPGA Remote TSD (PNP Diode)
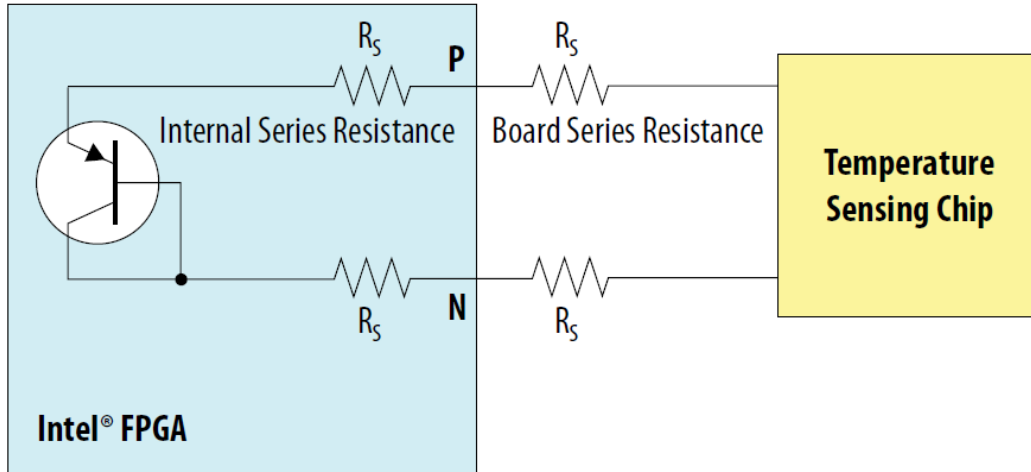
The following equation forms the temperature of a transistor in relation to the base-emitter voltage (VBE).

- **Equation 1.** Relationship Between Temperature of Transistor to Base-Emitter Voltage (VBE)

$$T = \frac{q \cdot V_{BE}}{\eta \cdot k \cdot \ln \frac{I_C}{I_S}}$$

Where:
  - T—Temperature in Kelvin
  - q—the electron charge (1.60 × 10–19 C)
  - VBE—base-emitter voltage
  - k—Boltzmann constant (1.38 × 10–23 J·K–1)
  - IC—the collector current
  - IS—the reverse saturation current
  - η—the ideality factor of the remote diode

  Rearranging Equation 1, you get the following equation.

- **Equation 2. VBE**

$$V_{BE} = \frac{\eta kT}{q} \ln\left(\frac{I_C}{I_S}\right)$$

Typically, the temperature sensing chip forces two consecutive well-controlled currents, I1 and I2 on the P and N pins. The chip then measures and averages the change of the VBE of the diode. The delta in VBE is directly proportional to the temperature, as shown in Equation 3.

- Equation 3. Delta in VBE

$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$

$$= \frac{\eta kT}{q} \ln\left(\frac{I_{C1}}{I_{S1}}\right) - \frac{\eta kT}{q} \ln\left(\frac{I_{C2}}{I_{S2}}\right)$$

$$= \frac{\eta kT}{q} \ln(n) \; ; \; n = \frac{I_{C1}}{I_{C2}}$$

Where:

- n—forced current ratio
- VBE1—base-emitter voltage at I1
- VBE2—base-emitter voltage at I2

Implementation Consideration

Selecting the temperature sensing chip with the appropriate features allows you to optimize the chip to achieve measurement accuracy. Consider the topics in the related information when you select the chip.

Related Information

- Ideality Factor (η-Factor) Mismatch
- Series Resistance Error
- Temperature Diode Beta Variation
- Differential Input Capacitor
- Offset Compensation

Ideality Factor (η-Factor) Mismatch

When you perform junction temperature measurement by using an external temperature diode, the accuracy of the temperature measurement depends on the characteristics of the external diode. The ideality factor is a parameter of a remote diode that measures the deviation of the diode from its ideal behavior.
You can usually find the ideality factor in the data sheet from the diode manufacturer. Different external temperature diodes give you different values because of the different design and process technologies they use. Ideality mismatch can cause a significant temperature measurement error. To avoid the significant error, Intel recommends that you select a temperature sensing chip that features a configurable ideality factor. You can change the ideality factor value in the chip to eliminate the mismatch error.

- **Example 1**. Ideality Factor Contribution to Temperature Measurement Error

This example shows how ideality factor contributes to the temperature measurement error. In the example, the calculation shows the ideality mismatch causing a significant temperature measurement error.

- **Equation 4.** Ideality Factor Relationship to Measured Temperature

$$\frac{\eta_{TSC} T_{TSC}}{\eta_{RTD} T_{RTD}} = 1$$

$$T_{TSC} = \frac{\eta_{RTD} T_{RTD}}{\eta_{TSC}}$$

Where:

- η_{TSC}—ideality factor of the temperature sensing chip
- T_{TSC}—temperature read by the temperature sensing chip
- η_{RTD}—ideality factor of the remote temperature diode
- T_{RTD}—temperature at the remote temperature diode

The following steps estimate temperature measurement (T_{TSC}) by the temperature sensing chip, given the following values:

- Ideality factor of the temperature sensor (η_{TSC}) is 1.005
- Ideality factor of the remote temperature diode (η_{RTD}) is 1.03
- Actual temperature at the remote temperature diode (T_{RTD}) is 80°C

1. Convert the T_{RTD} of 80°C to Kelvin: 80 + 273.15 = 353.15 K.
2. Apply Equation 4. The calculated temperature by the temperature sensing chip is 1.005 × 353.15 = 344.57 K.$T_{TSC} = 1.03$
3. Convert the calculated value to Celsius: T_{TSC} = 344.57 K – 273.15 K = 71.43°C The temperature error (TE) caused by the ideality mismatch:
   TE = 71.43°C – 80.0°C = –8.57°C
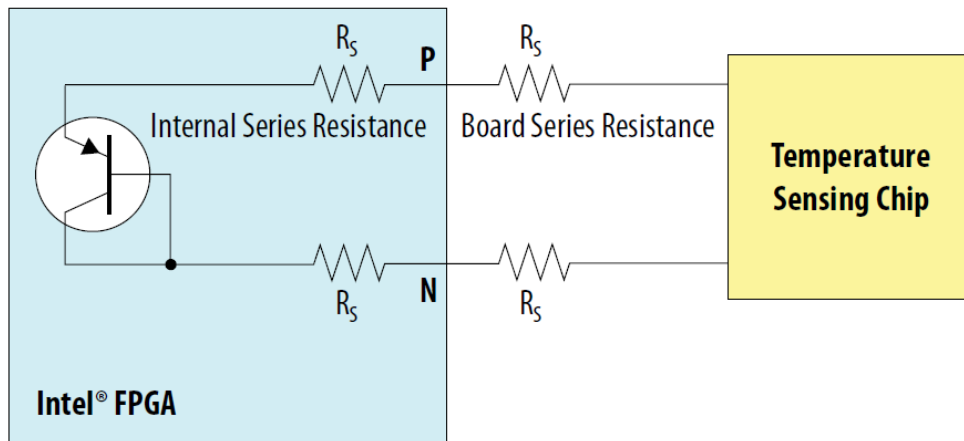
Series Resistance Error

The series resistance on the P and N pins contributes to temperature measurement error.

The series resistance can be from:

- The internal resistance of the P and N pin of the temperature diode.
- The board trace resistance, for example, a long board trace.

The series resistance causes additional voltage to drop at the temperature sensing path and results in measurement error, affecting the accuracy of the temperature measurement. Typically, this situation happens when you perform temperature measurement with a 2-current temperature sensing chip.

Figure 3. Internal and On-Board Series Resistance

To explain the temperature error incurred when the series resistance increases, some temperature sensing chip manufacturer provides the data for the remote diode temperature error versus the resistance.
However, you can eliminate the series resistance error. Some temperature sensing chip has built-in series resistance cancellation feature. The series resistance cancellation feature can eliminate the series resistance from a range of a few hundred Ω to a range exceeding a few thousand Ω.
Intel recommends that you consider the series resistance cancellation feature when you select the temperature sensing chip. The feature automatically eliminates the temperature error caused by the resistance of the routing to the remote transistor.

Temperature Diode Beta Variation

As process technology geometries gets smaller, the Beta(β) value of the PNP or NPN substrate decreases.
As the temperature diode Beta value gets lower, especially if the temperature diode collector is tied to the ground, the Beta value affects the current ratio on Equation 3 on page 5. Therefore, maintaining an accurate current ratio is crucial.
Some temperature sensing chips have built-in Beta compensation feature. The Beta variation of the circuitry senses the base current and adjusts the emitter current to compensate for the variation. The Beta compensation maintains the collector current ratio.

Figure 4. Intel Stratix 10 Core Fabric Temperature Diode with Maxim Integrated*'s MAX31730 Beta Compensation Enabled
This figure shows that the measurement accuracy is achieved with Beta compensation enabled. The measurements were taken during FPGA power down condition—the set and measured temperatures are expected to be close.
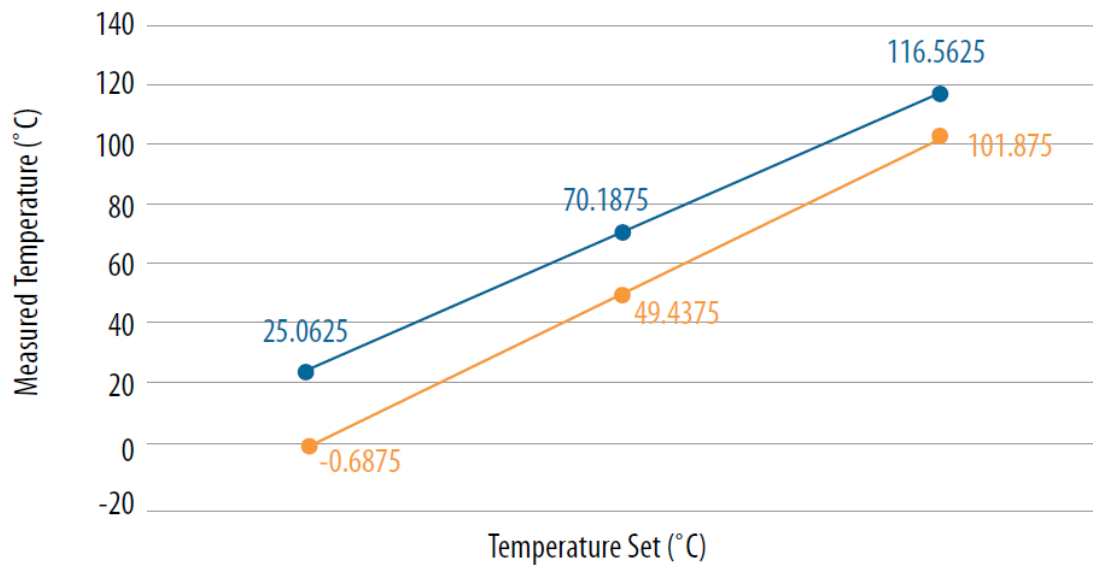
	0°C	50°C	100°C
Beta Compensation Off	25.0625°C	70.1875°C	116.5625°C
Beta Compensation On	-0.6875°C	49.4375°C	101.875°C

Differential Input Capacitor

The capacitor (CF) on P and N pins acts like a low-pass filter that helps to filter the high frequency noise and improve the electromagnetic interference (EMI).
You must be careful during capacitor selection because the large capacitance can affect the rise time of the switched current source and introduce a huge measurement error. Typically, the temperature sensing chip manufacturer provides the recommended capacitance value in their data sheet. Refer to the capacitor manufacturer's design guidelines or recommendation before you decide the capacitance value.

Figure 5. Differential Input Capacitance
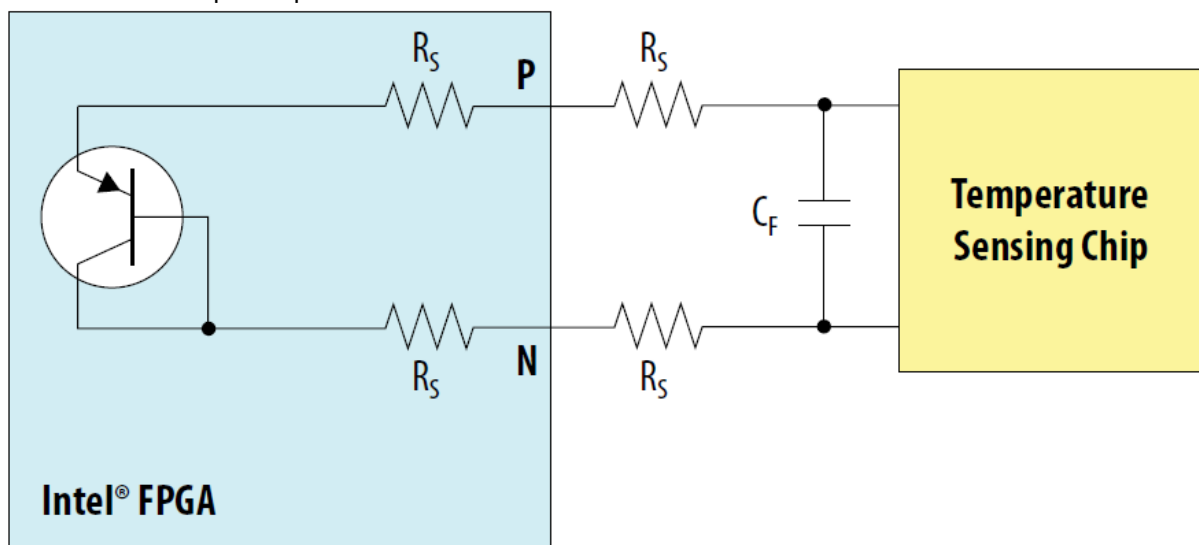
Offset Compensation

Multiple factors can simultaneously contribute to the measurement error. Sometime, applying a single compensation method may not fully resolve the issue. Another method to resolve the measurement error is to apply offset compensation.

Note: Intel recommends that you use a temperature sensing chip with built-in offset compensation. If the temperature sensing chip does not support the feature, you may apply offset compensation during post processing through custom logic or software.

Offset compensation changes the offset register value from the temperature sensing chip to eliminate the calculated error. To use this feature, you must perform a temperature profile study and identify the offset value to apply.

You must collect temperature measurements across the desired temperature range with the default settings of the temperature sensing chip. Afterward, perform data analysis as in the following example to determine the offset value to apply. Intel recommends that you test several temperature sensing chips with several remote temperature diode to ensure that you cover the part-to-part variations. Then, use the measurements average in the analysis to determine the settings to apply.

You can select the temperature points to test based on your system operation condition.

Equation 5. Offset Factor

$$\text{Offset factor} = \frac{T_{measure\_high} - T_{measure\_low}}{T_{set\_high} - T_{set\_low}}$$

Example 2. Application of Offset CompensationIn this example, a set of temperature measurements was collected with three temperature points. Apply Equation 5 to the values and calculate the offset factor.

Table 1. Data Collected Before Applying Offset Compensation

Set Temperature		Measured Temperature	
100°C	373.15 K	111.06°C	384.21 K
50°C	323.15 K	61.38°C	334.53 K
0°C	273.15 K	11.31°C	284.46 K

$$= \frac{T_{measure\_high} - T_{measure\_low}}{T_{set\_high} - T_{set\_low}}$$

$$= \frac{384.21 - 284.46}{373.15 - 273.15}$$

$$= 0.9975$$

Use the middle point of the temperature range to calculate the offset temperature. In this example, the middle point is the 50°C set temperature.

Offset temperature

- = Offset factor × (Measured temperature–Set temperature)
- = 0.9975 × (334.53 – 323.15)

- = 11.35

Apply the offset temperature value and other compensation factors, if required, into the temperature sensing chip and retake the measurement.

Table 2. Data Collected After Applying Offset Compensation

Set Temperature	Measured Temperature	Error
100°C	101.06°C	1.06°C
50°C	50.13°C	0.13°C
0°C	0.25°C	0.25°C

Related Information
Evaluation Results
Provides a review of the evaluation results of offset compensation method with Maxim Integrated* and Texas Instruments* temperature sensing chips.

Evaluation Results

In the evaluation, the Maxim Integrated*'s MAX31730 and Texas Instruments*'s TMP468 evaluation kits were modified to interface with the remote temperature diodes of several blocks in the Intel FPGA.

Table 3. Evaluated Blocks and Board Models

Block	Temperature Sensing Chip Evaluation Board	
	Texas Instruments' TMP468	Maxim Integrate d's MAX31730
Intel Stratix 10 core fabric	Yes	Yes
H-tile or L-tile	Yes	Yes
E-tile	Yes	Yes
P-tile	Yes	Yes

The following figures show the setup of the Intel FPGA board with the Maxim Integrated and Texas Instruments evaluation boards.

Figure 6. Setup with Maxim Integrate d's MAX31730 Evaluation Board
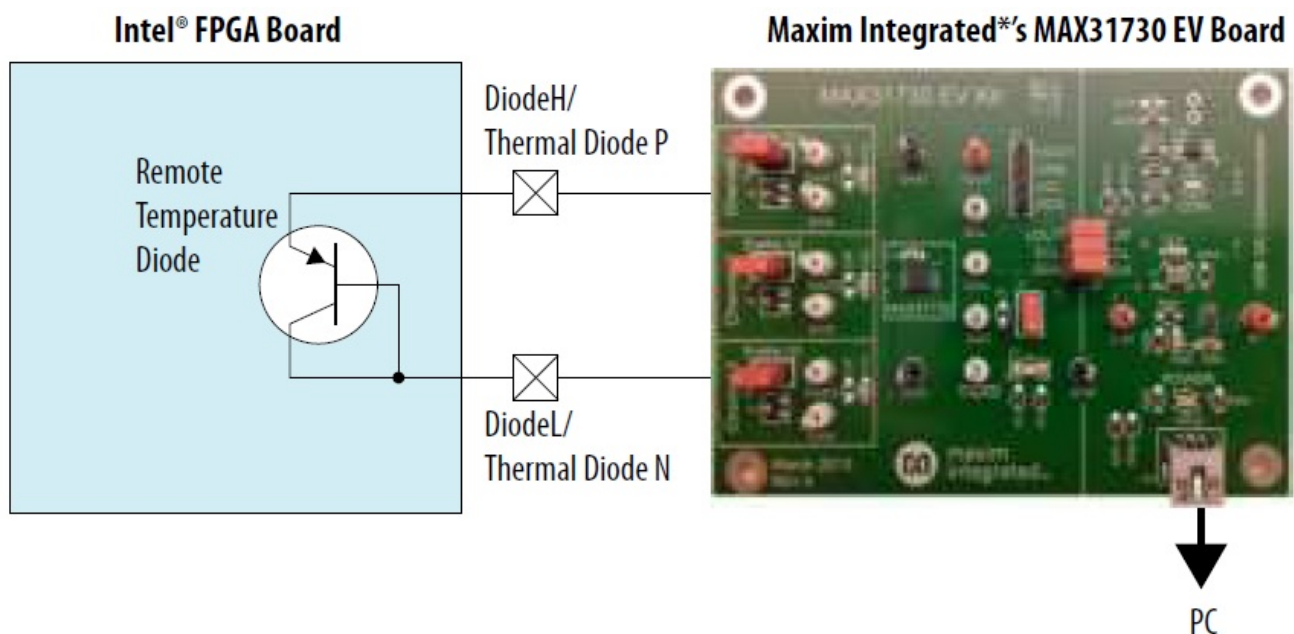
**Figure 7.** Setup with the Texas Instruments' TMP468 Evaluation Board
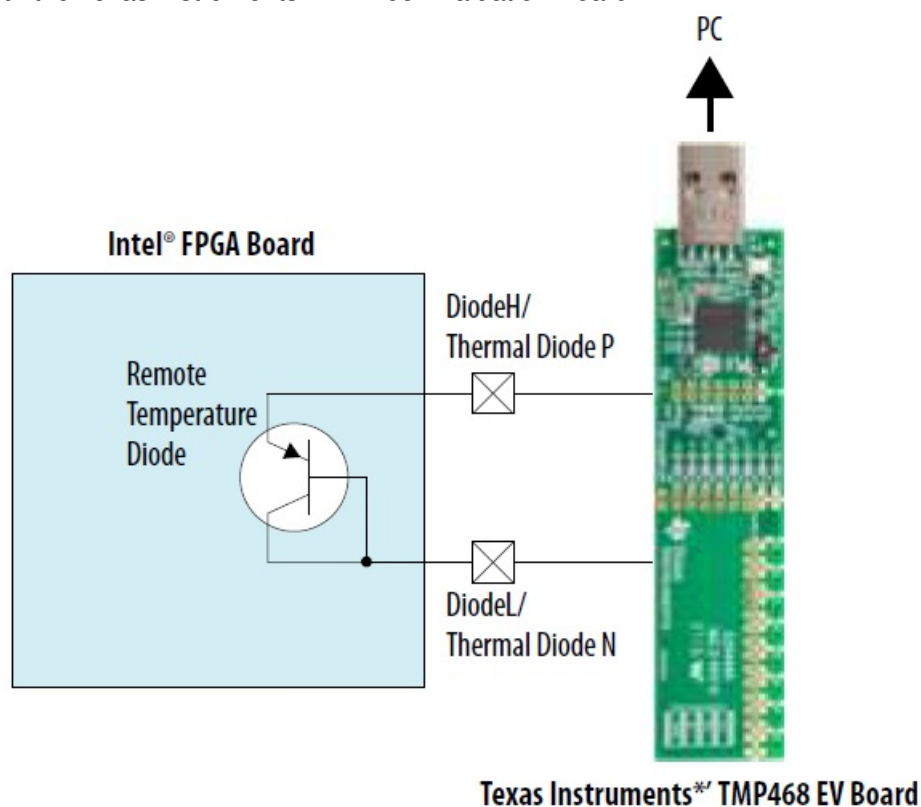
- A thermal forcer—or alternatively, you can use a temperature chamber—covered and sealed the FPGA and forced the temperature as per the set temperature point.
- During this test, the FPGA remained in unpowered condition to avoid it from generating heat.
- The soak time for each temperature test point was 30 minutes.
- The settings on the evaluation kits used the default settings from the manufacturers.
- After the setup, steps in Offset Compensation on page 10 were followed for data collection and analysis.

Evaluation with Maxim Integrated's MAX31730 Temperature Sensing Chip Evaluation Board

This evaluation was conducted with setup steps as described in Offset Compensation .
The data was collected before and after applying the offset compensation. Different offset temperature was

applied to different Intel FPGA blocks because a single offset value cannot be applied on all blocks. The following figures show the results.
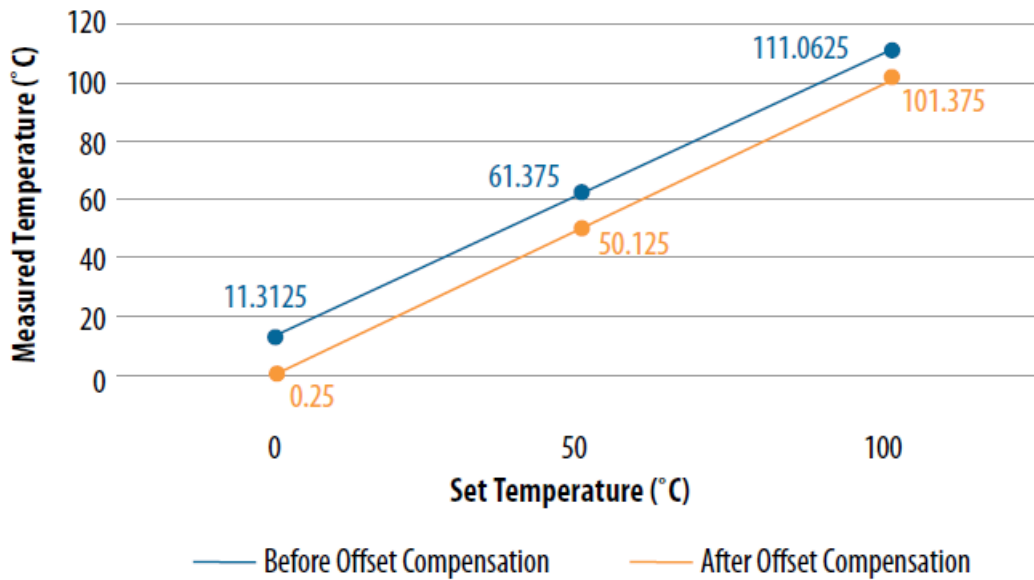
Figure 8. Data for Intel Stratix 10 Core Fabric
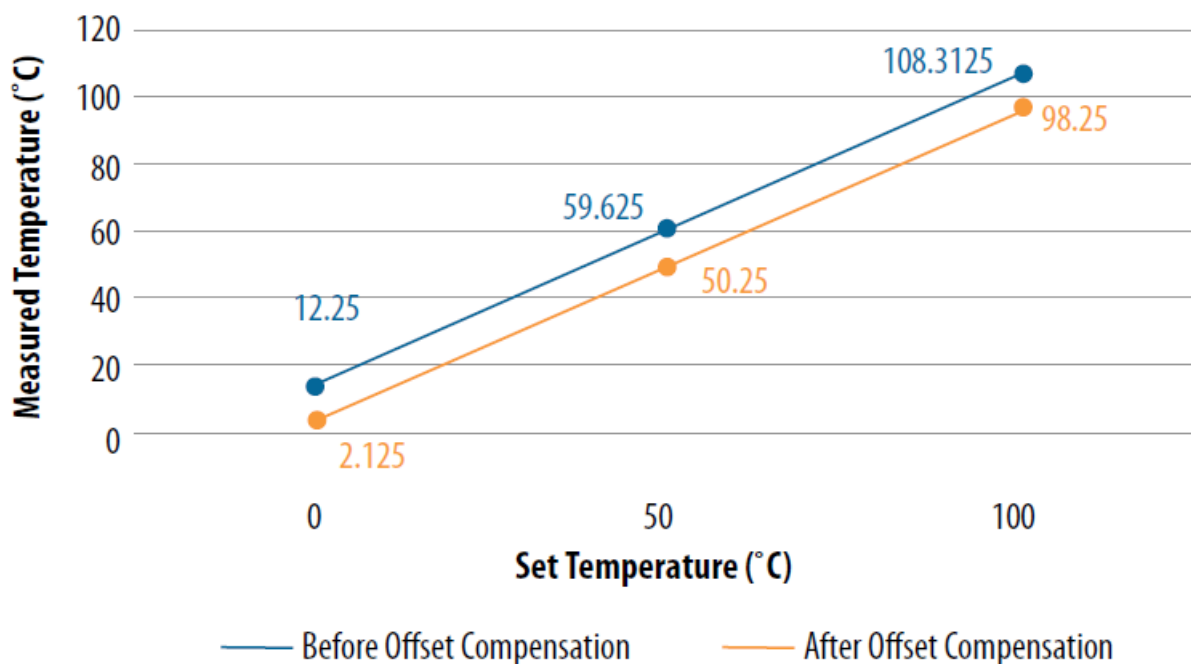
**Figure 9. Data for Intel FPGA H-Tile and L-Tile**
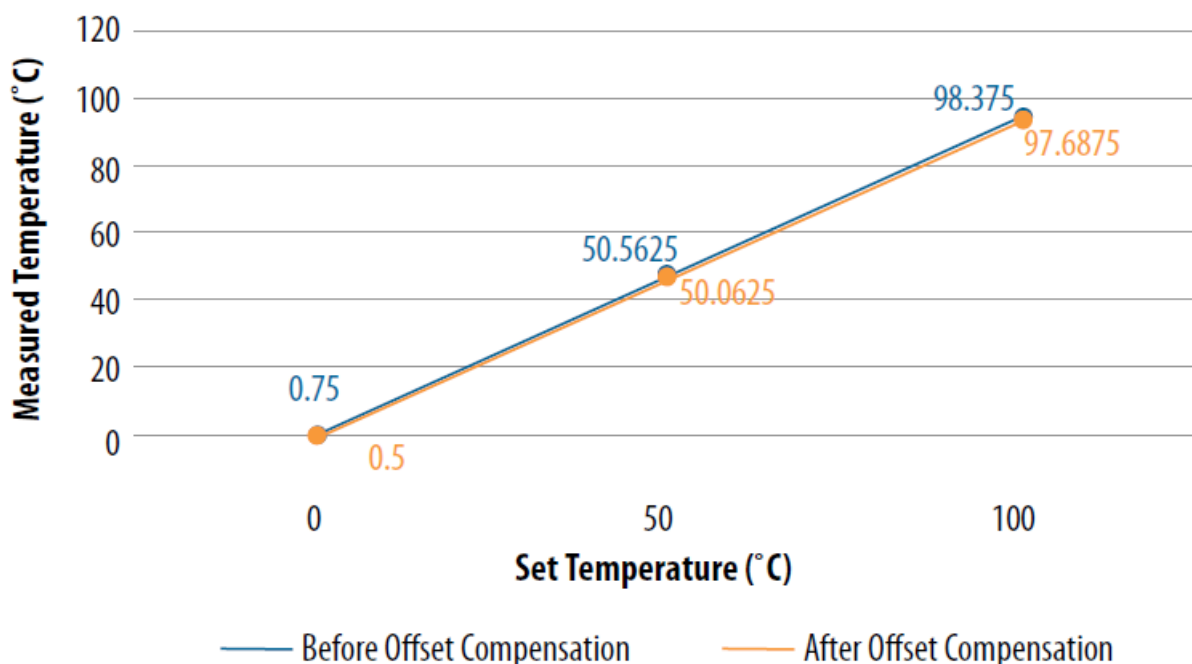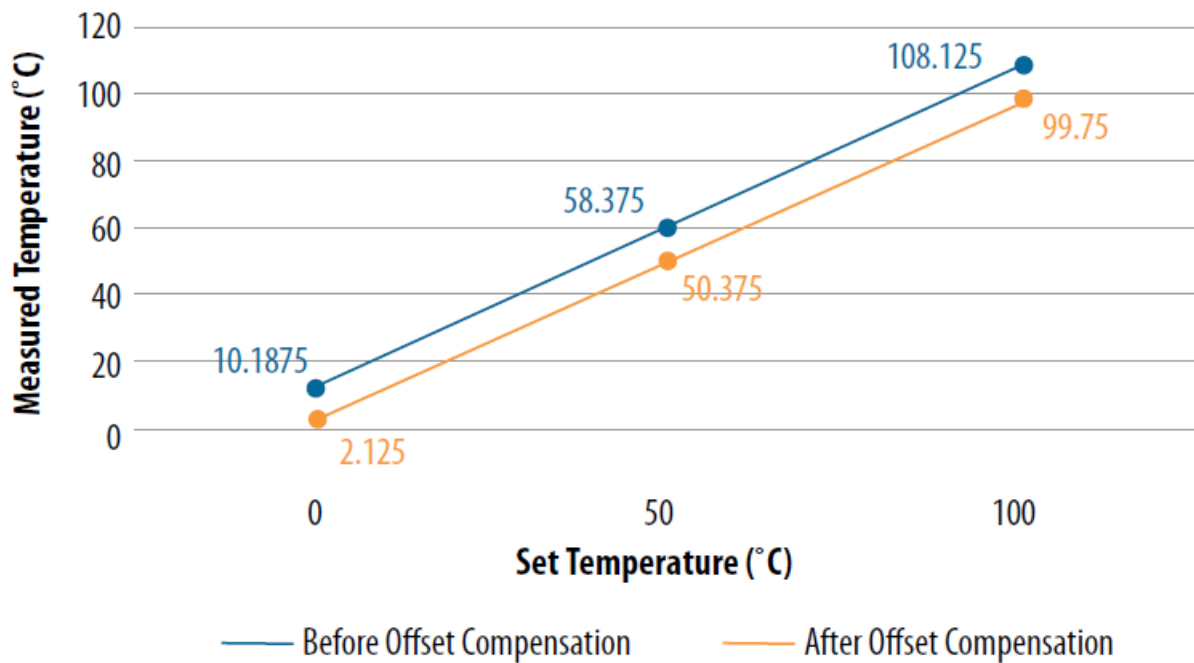

Figure 10. Data for Intel FPGA E-Tile
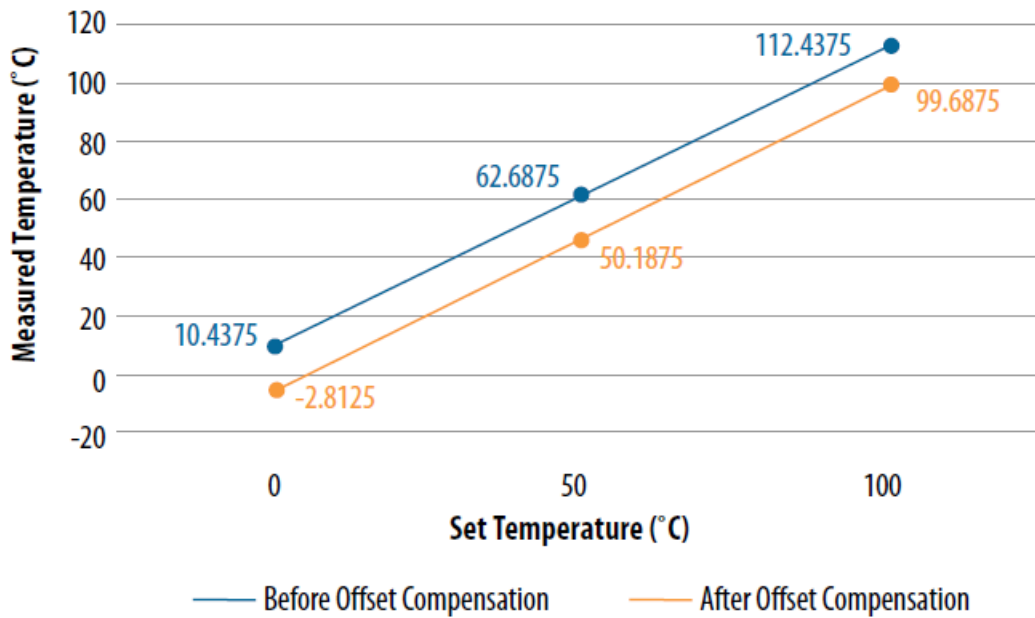
Figure 11. Data for Intel FPGA P-Tile

Evaluation with Texas Instruments's TMP468 Temperature Sensing Chip Evaluation Board

This evaluation was conducted with setup steps as described in Offset Compensation .
The data was collected before and after applying the offset compensation. Different offset temperature was applied to different Intel FPGA blocks because a single offset value cannot be applied on all blocks. The following figures show the results.

Figure 12. Data for Intel Stratix 10 Core Fabric
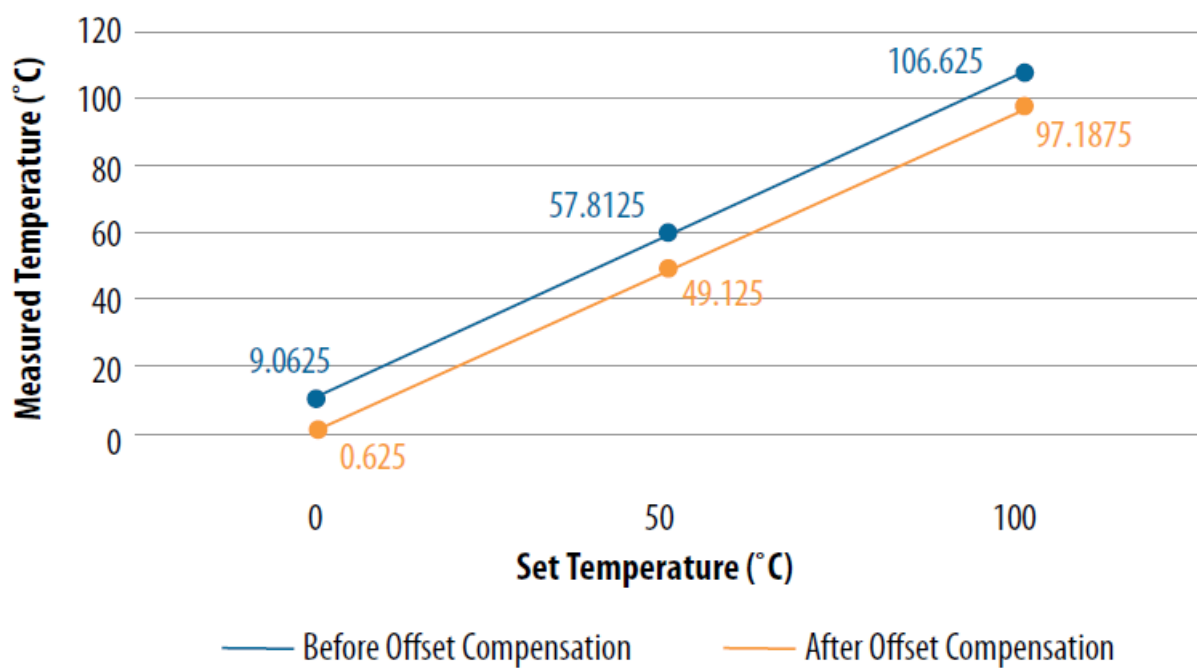
Figure 13. Data for Intel FPGA H-Tile and L-Tile
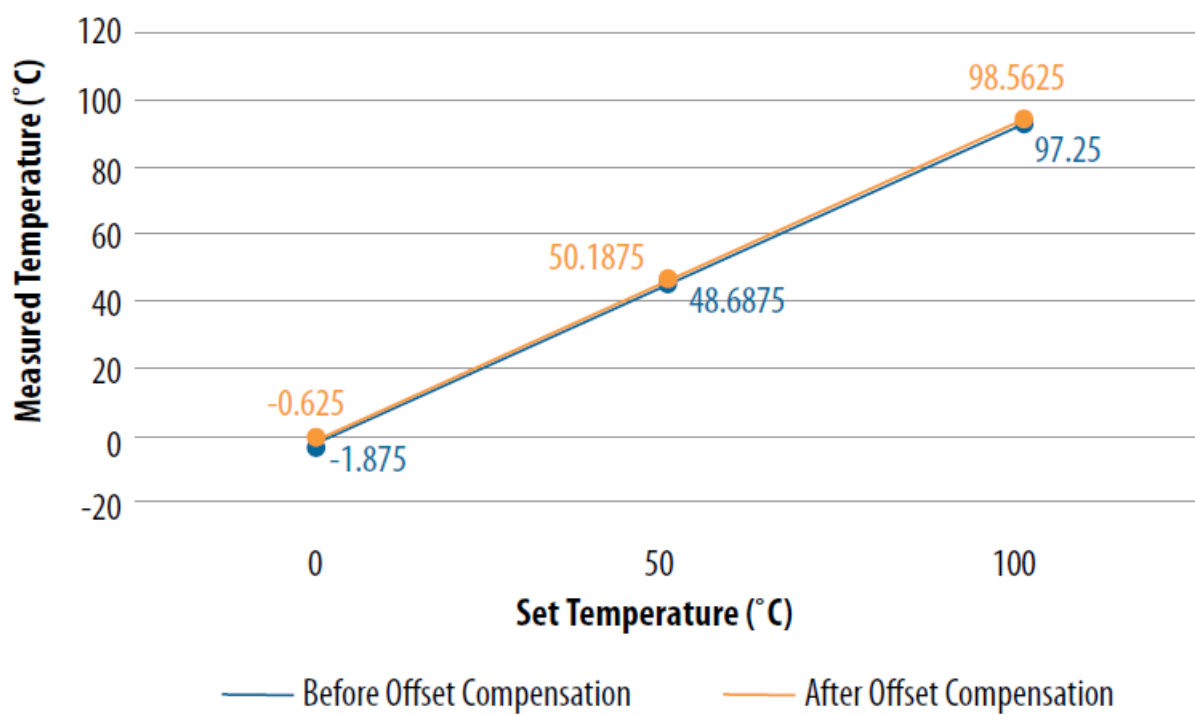
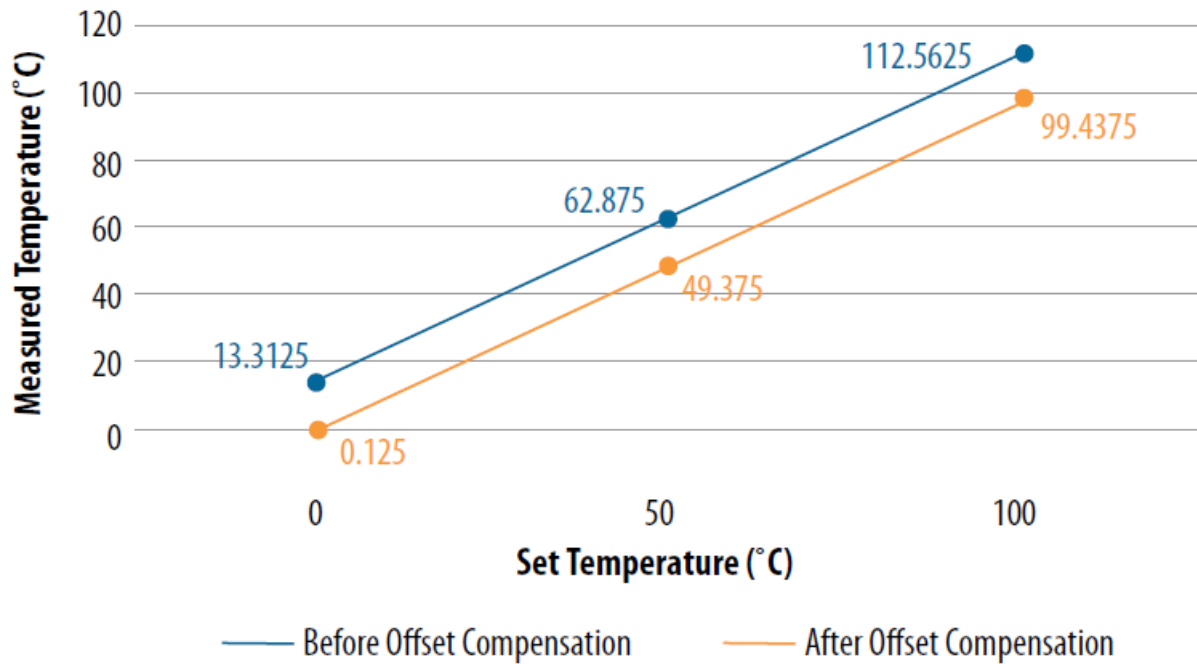**Figure 14. Data for Intel FPGA E-Tile**

Figure 15. Data for Intel FPGA P-Tile

Conclusion

There are many different temperature sensing chip manufacturers. During component selection, Intel strongly recommends that you select the temperature sensing chip with the following considerations.

1. Select a chip with configurable ideality factor feature.
2. Select a chip that has series resistance cancellation.
3. Select a chip that supports Beta compensation.
4. Select capacitors that matches the chip manufacturer's recommendations.
5. Apply any appropriate compensation after performing a temperature profile study.

Based on the implementation consideration and evaluation results, you must optimize the temperature sensing chip in your design to achieve measurement accuracy.

Document Revision History for AN 769: Intel FPGA Remote Temperature Sensing Diode Implementation Guide

Document Version	Changes
2022.04.06	- Corrected the temperature sensing chip temperature calculation in the topic about ideality factor mismatch. - Corrected the offset temperature calculation example in the topic about offset compensation.
2021.02.09	Initial release.

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