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intel Acceleration Stack for Xeon CPU with FPGAs 1.0 Errata User Manual

Contents

intel Acceleration Stack for Xeon CPU with FPGAs 1.0 Errata

Product Information

Issue	Description	Workaround	Status
Flash Fallback Does Not Meet PCIe Timeout	The host may hang or report a PCIe failure after a flash failover has occurred. This issue can be seen when the user image in flash is corrupted and the configuration subsystem loads the factory image into the FPGA.	Follow the instructions in the Updating Flash with FPGA Interface Manager (FIM) Image using Intel Quartus Prime Programmer section in the Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA. If the issue persists, contact your local field representative.	Affects: Intel Acceleration Stack 1.0 Production Status: No planned fix
Unsupported Transaction Layer Packet Types	The Acceleration Stack FPGA Interface Manager (FIM) does not support PCIe* Memory Read Lock, Configuration Read Type 1, and Configuration Write Type 1 transaction layer packets (TLPs). If the device receives a PCIe packet of this type, it does not respond with a Completion packet as expected.	No workaround available.	Affects: Intel Acceleration Stack 1.0 Production Status: No planned fix
JTAG Timing Failures May Be Reported in the FPGA Interface Manager	The Intel Quartus Prime Pro Edition Timing Analyzer may report unconstrained JTAG I/O paths in the FIM.	These unconstrained paths can be safely ignored because the JTAG I/O paths are not used in the FIM.	Affects: Intel Acceleration Stack 1.0 Production Status: Planned fix in Intel Acceleration Stack 1.1

Product Usage Instructions

To resolve the issues mentioned above, please follow the instructions provided below:

Flash Fallback Does Not Meet PCIe Timeout

If you encounter a hang or PCIe failure after a flash failover, it may be due to a corrupted user image in the flash. To resolve this issue, please do the following:

1. Refer to the Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA.
2. Follow the instructions in the "Updating Flash with FPGA Interface Manager (FIM) Image using Intel Quartus Prime Programmer" section.
3. If the issue persists, contact your local field representative for further assistance.

Unsupported Transaction Layer Packet Types

If you are experiencing issues with unsupported transaction layer packet types, such as PCIe Memory Read Lock, Configuration Read Type 1, and Configuration Write Type 1, follow these steps:

1. No workaround is available for this issue. Please note that the Acceleration Stack FPGA Interface Manager (FIM) does not support these packet types.

JTAG Timing Failures May Be Reported in the FPGA Interface Manager

If you encounter JTAG timing failures reported in the FPGA Interface Manager, follow these steps:

1. You can safely ignore the unconstrained JTAG I/O paths reported by the Intel Quartus Prime Pro Edition Timing Analyzer in the FIM.
2. These paths are not used in the FIM and should not impact its functionality.

Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs 1.0 Errata

This document provides information about errata affecting the Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs.

Issue	Affected Versions	Planned Fix
Flash Fallback Does Not Meet PCIe Timeout on page 4	Acceleration Stack 1.0 Production	No Planned Fix
Unsupported Transaction Layer Packet Types on page 5	Acceleration Stack 1.0 Production	No Planned Fix
JTAG Timing Failures May Be Reported in the FPGA Interface Manager on page 6	Acceleration Stack 1.0 Production	Acceleration Stack 1.1
fpgabist Tool Does Not Pass Hexadecimal Bus Numbers Properly on page 7	Acceleration Stack 1.0 Production	Acceleration Stack 1.1
Possible Low dma_afu Bandwidth Due to memcpy Function on page 8	Acceleration Stack 1.0 Beta and Production	Acceleration Stack 1.1
regress.sh -r Option Does Not Work With dma_afu on page 9	Acceleration Stack 1.0 Production	No planned fix

The table below can be used as a reference to identify the FPGA Interface Manager (FIM), Open Programmable Acceleration Engine (OPAE) and Intel Quartus® Prime Pro Edition version that corresponds to your software stack release.

Table 1.   Intel Acceleration Stack 1.0 Reference Table

Intel Acceleration Stack Version	Boards	FIM Version (PR Interface ID)	OPAE Version	Intel Quartus Prime Pro Edition
1.0 Production (1)	Intel PAC with Intel Arria® 10 GX FPGA	ce489693-98f0-5f33-946d-560708 be108a	0.13.1	17.0.0

Related Information

Intel Acceleration Stack for Intel Xeon CPU with FPGAs Release Notes Refer to the release notes for more information about known issues and enhancements for Intel Acceleration Stack 1.0

(1) The factory partition of the configuration flash contains the Acceleration Stack 1.0 Alpha version. When the image in the user partition cannot be loaded, a flash failover occurs and the factory image is loaded instead. After a flash failover occurs, the PR ID reads as d4a76277-07da-528d-b623-8b9301feaffe.

Flash Fallback Does Not Meet PCIe Timeout

Description

The host may hang or report a PCIe failure after a flash failover has occurred. This issue can be seen when the user image in flash is corrupted and the configuration subsystem loads the factory image into the FPGA.

Workaround
Follow the instructions in the "Updating Flash with FPGA Interface Manager (FIM) Image using Intel Quartus Prime Programmer" section in the Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA. If the issue persists, contact your local field representative.

Status

- Affects: Intel Acceleration Stack 1.0 Production
- Status: No planned fix

Related Information
Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA

Unsupported Transaction Layer Packet Types

Description
The Acceleration Stack FPGA Interface Manager (FIM) does not support PCIe* Memory Read Lock, Configuration Read Type 1, and Configuration Write Type 1 transaction layer packets (TLPs). If the device receives a PCIe packet of this type, it does not respond with a Completion packet as expected.

Workaround
No workaround available.

Status

- Affects: Intel Acceleration Stack 1.0 Production
- Status: No planned fix

JTAG Timing Failures May Be Reported in the FPGA Interface Manager

Description
The Intel Quartus Prime Pro Edition Timing Analyzer may report unconstrained JTAG I/O paths in the FIM.

Workaround
These unconstrained paths can be safely ignored because the JTAG I/O paths are not used in the FIM.

Status

- Affects: Intel Acceleration Stack 1.0 Production
- Status: Planned fix in Intel Acceleration Stack 1.1

fpgabist Tool Does Not Pass Hexadecimal Bus Numbers Properly

Description
The Open Programmable Acceleration Engine (OPAE) fpgabist tool does not pass valid bus numbers if the PCIe bus number is any character above F. If any of these characters are included, you may encounter the following error message:

```
Running mode: nlb_3

Attempting Partial Reconfiguration:

invalid bus: d4

Failed to load gbs file: /home/lab/workspace/DCP/PRC/hw/samples/nlb_mode_3/bin/
nlb_mode_3.gbs

Please try a different gbs
```

Workaround
Change /usr/bin/bist_common.py line 83 from

```
cmd = "{} -b {} -v {}".format('fpgaconf', bus_num, gbs_file)
```

to

```
cmd = "{} -b 0x{} -v {}".format('fpgaconf', bus_num, gbs_file)
```

Status
Affects: Intel Acceleration Stack 1.0 Production Status: Planned fix in Intel Acceleration Stack 1.1

Possible Low dma_afu Bandwidth Due to memcpy Function

Description
fpgabist may report lower bandwidth for the dma_afu but not the native loopback 3 (NLB3) due to the use of the memcpy function in the dma_afu driver.

Workaround
You can workaround this erratum by removing memcpy from the dma_afu driver code and adding code to accept buffers from the user that have been pre-pinned. For use with OpenCL*, there is no current workaround.

Status

- Affects: Intel Acceleration Stack 1.0 Beta and Production
- Status: Planned fix in Intel Acceleration Stack 1.1

regress.sh -r Option Does Not Work With dma_afu

Description
When using the -r option with regress.sh, the script does not work with the dma_afu example. Using the -r option results in a fatal gcc error.

Workaround
Do not use the -r option when running the regress.sh script. Running the script without the -r option places the output simulation in $OPAE_LOC/ase/rtl_sim instead of a user-specified directory.

Status

- Affects: Intel Acceleration Stack 1.0 Production
- Status: No planned fix

Intel Acceleration Stack for Intel Xeon CPU with FPGAs 1.0 Errata Revision History

Date	Intel Acceleration Stack Version	Changes
2018.06.22	1.0 Production (compatible with Intel Quartus Prime Pro Edition 17.0.0)	Updated the path of the bist_common.py file in the fpgabist Tool Does Not Pass Hexadecimal Bus Numbers Properly erratum.
2018.04.11	1.0 Production (compatible with Intel Quartus Prime Pro Edition 17.0.0)	Initial release.

Documents / Resources

	intel Acceleration Stack for Xeon CPU with FPGAs 1.0 Errata [pdf] User Manual Acceleration Stack for Xeon CPU with FPGAs 1.0 Errata, Xeon CPU with FPGAs 1.0 Errata, Acceleration Stack, Stack

References

- intel **1. About This Document**
- intel **Notice**
- intel **Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs 1.0 Errata**
- intel **Intel ISO 9001:2015 Registrations**

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