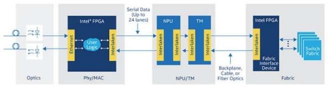

intel 50G Interlaken Design Example User Guide

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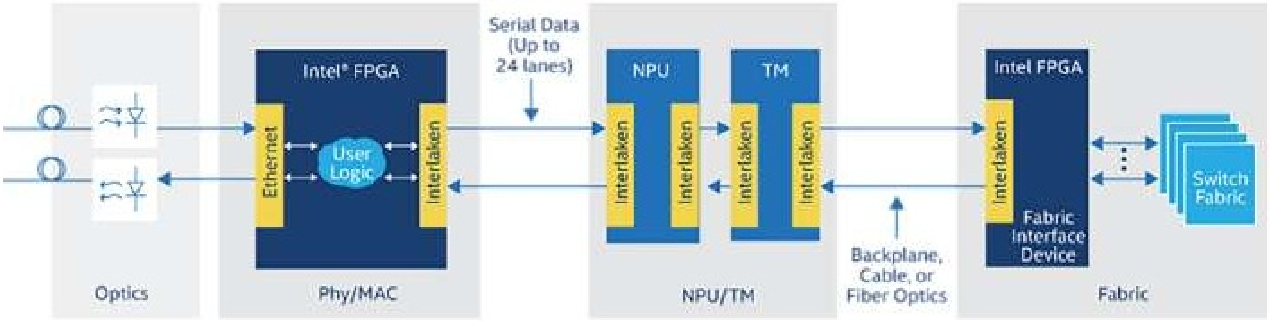
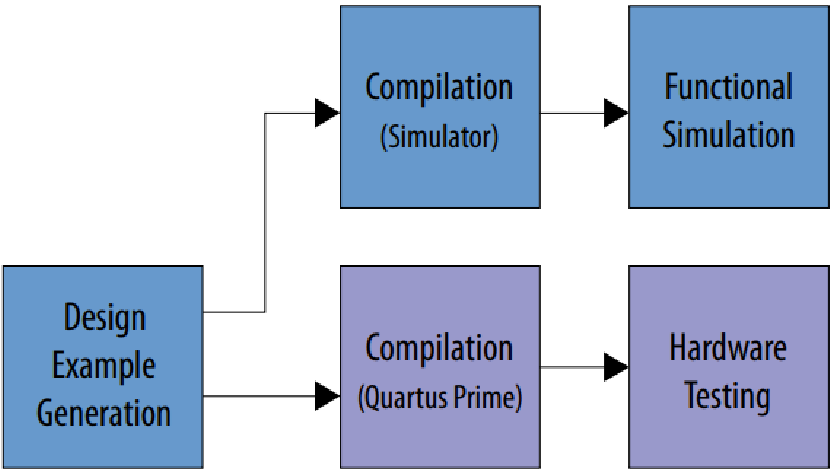


The Intel® Arria® 10 variations of the 50G Interlaken IP core feature a simulating testbench and a hardware example design that supports compilation and hardware testing, to help you understand usage.

When you generate the example design, the parameter editor automatically creates the files necessary to simulate, compile, and test the design in hardware. You can download the compiled hardware design to the Intel Arria 10 GX Transceiver Signal Integrity Development Kit. The testbench and demonstration example design are available for a wide range of parameters. However, they do not cover all possible parameterizations of the 50G Interlaken IP Core.

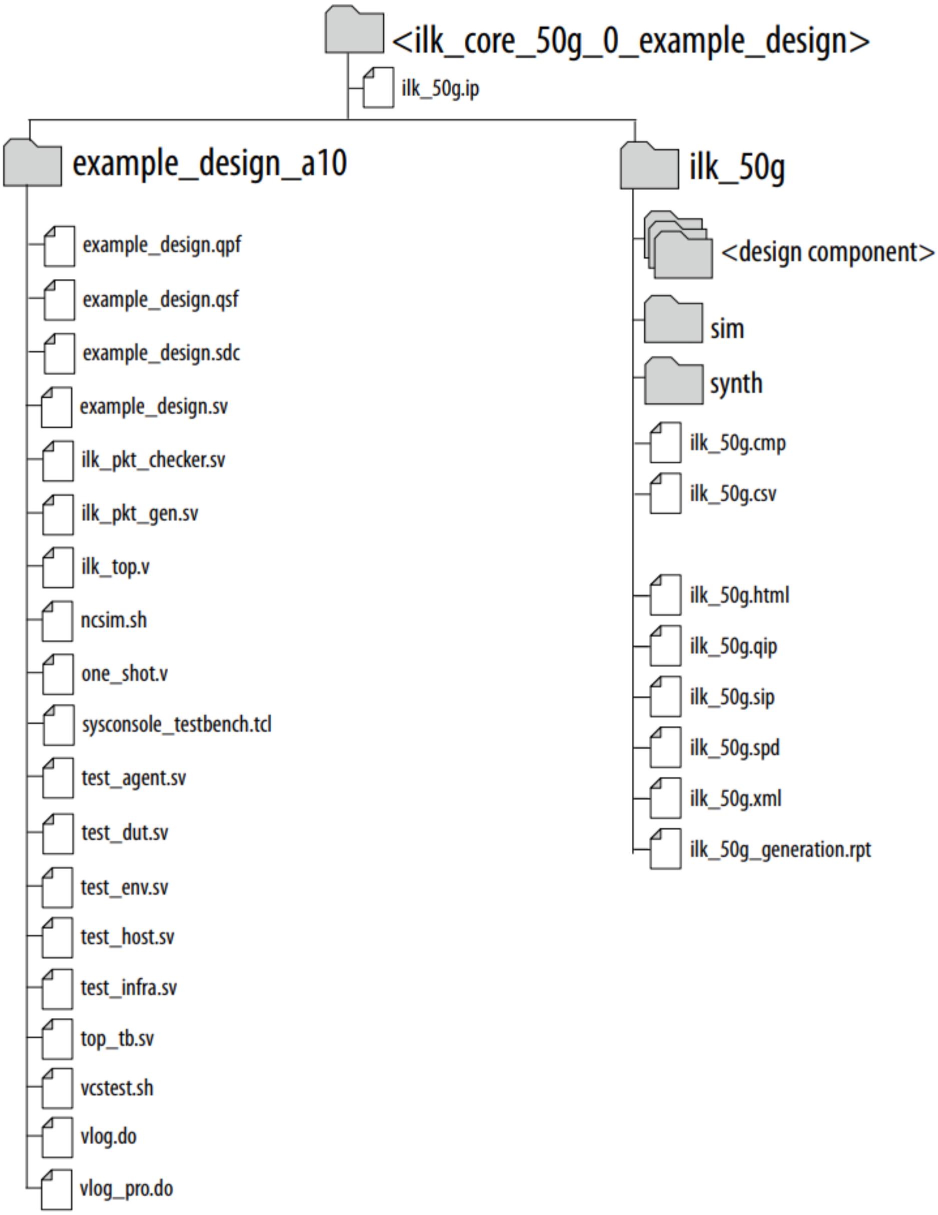
In addition, for most IP core variations, Intel provides a compilation-only example project that you can use to quickly estimate IP core area and timing.

Development Steps



Directory Structure

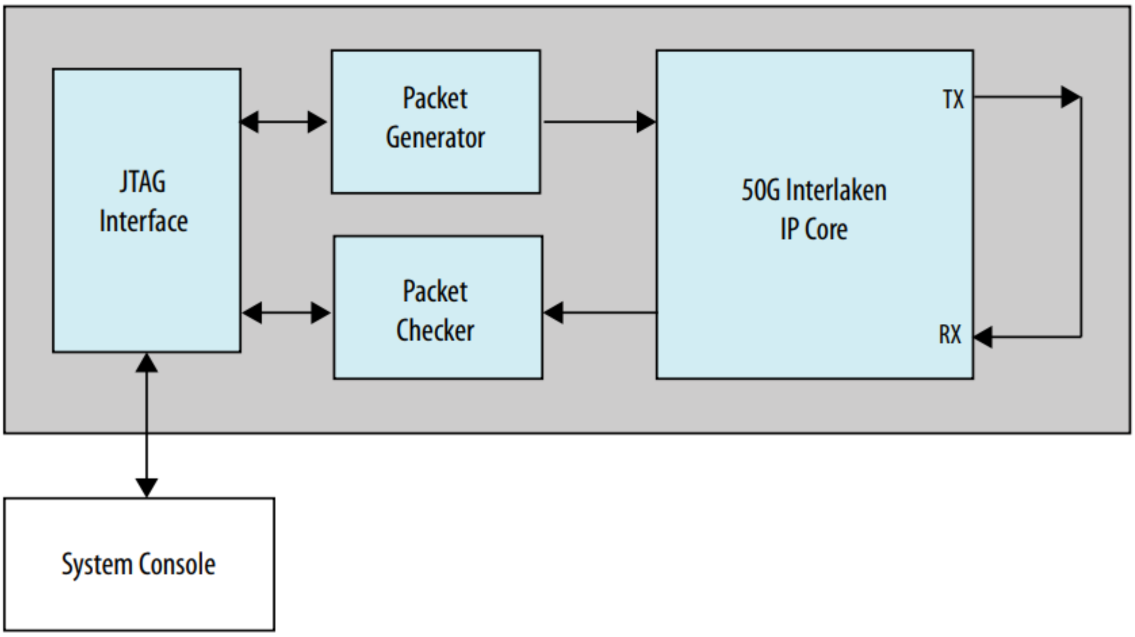
Directory Structure for the Generated Example Design



The hardware configuration, simulation, and test files are located in <example_design_install_dir>/example_design_a10.

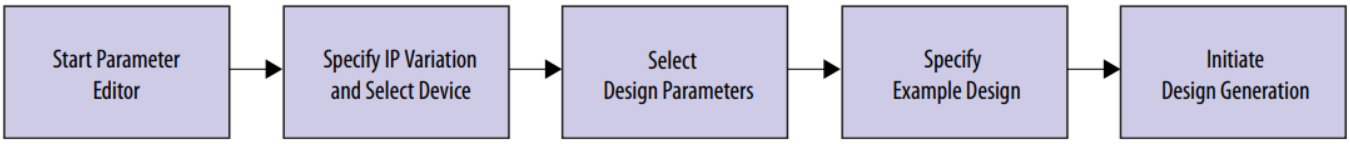
Design Components

Example Design Block Diagram



Generating the Design

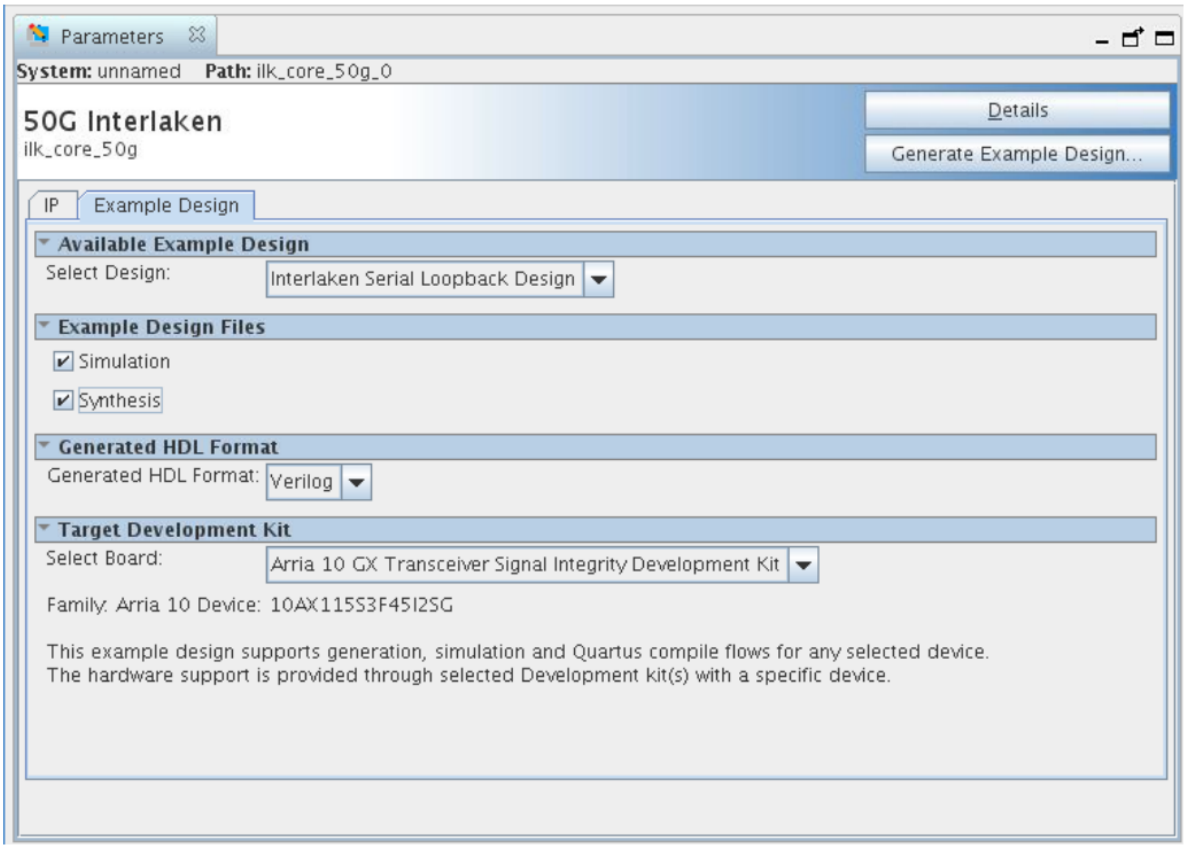
Procedure



Follow these steps to generate the Intel Arria 10 hardware example design and testbench:

1. In the IP Catalog (Tools > IP Catalog), select the Intel Arria 10 target device family.
   Note: The Quick Start hardware example design is only supported in Intel Arria 10 devices. The testbench is available for variations that target Intel Arria 10 devices or Stratix® V devices.
2. In the IP Catalog, locate and double-click 50G Interlaken. The New IP Variation window appears.
3. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file named <your_ip>.qsys.
4. You must select a specific Intel Arria 10 device in the Device field, or keep the default Intel Quartus® Prime software device selection.
5. Click OK. The parameter editor appears.

50G Interlaken Parameter Editor



System: unnamed Path: ilk_core_50g_0

50G Interlaken
ilk_core_50g

Available Example Design

Select Design: Interlaken Serial Loopback Design

Example Design Files

☑ Simulation

☑ Synthesis

Generated HDL Format

Generated HDL Format: Verilog

Target Development Kit

Select Board: Arria 10 GX Transceiver Signal Integrity Development Kit

Family: Arria 10 Device: 10AX115S3F45I2SG

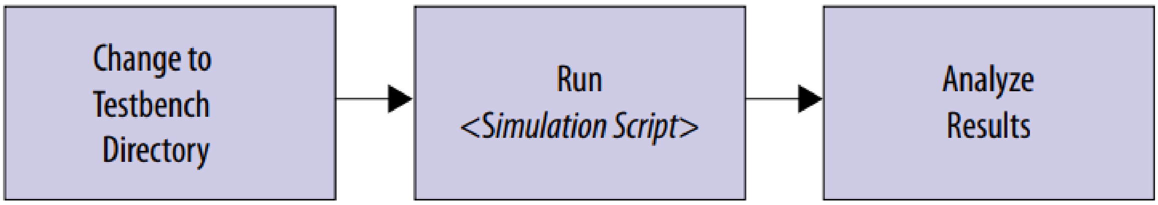
This example design supports generation, simulation and Quartus compile flows for any selected device.
The hardware support is provided through selected Development kit(s) with a specific device.

6. On the IP tab, specify the parameters for your IP core variation.
7. On the Example Design tab, select the Simulation option to generate the testbench, and select the Synthesis option to generate the hardware example design.
Note: At least one of the Simulation and Synthesis check boxes from Example Design Files must be selected to allow generation of Example Design Files.
8. For Generated HDL Format, only Verilog is available.
9. For Target Development Kit select the Intel Arria 10 GX Transceiver Signal Integrity Development Kit. If you select a development kit, then the target device (selected in step 4) for Example Design is changed to match the device on target board.
10. Click the Generate Example Design button.

Related Information
50G Interlaken IP Core Parameter Settings
Provides information about the 50G Interlaken IP core customization by specifying parameters.

Simulating the Design

Procedure



Follow these steps to simulate the testbench:

1. Change to the testbench simulation directory <example_design_install_dir>/example_ design_a10/testbench.
2. Run the simulation script for the supported simulator of your choice. The script compiles and runs the testbench in the simulator. Your script should check that the SOP and EOP counts match after simulation is complete.

Refer to the table Steps to Run Simulation.

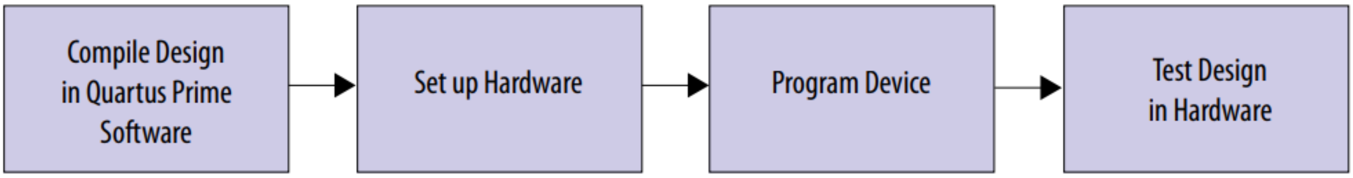
3. Analyze the results.

Steps to Run Simulation

Simulator	Instructions
ModelSim* SE or QuestaSim* or Questa* Intel FPGA Edition	In the command line, type vsim -do vlog_pro.do If you prefer to simulate without bringing up the GUI, type vsim -c -do vlog_pro.do
VCS*	In the command line, type sh vcstest.sh
Xcelium*	In the command line, type sh xcelium.sh

A successful simulation ends with the following message:

Compiling and Testing the Design



Compiling and Testing the Design
To compile and run a demonstration test on the hardware example design, follow these steps:

1. Ensure hardware example design generation is complete.
2. Open the Intel Quartus Prime project <user-specified location>/example_design_a10/quartus/example_design.qpf, where <user-specified location> is the directory location you specified when you generated the testbench and hardware example design.
3. On the Processing menu, click Start Compilation.
4. After successful compilation, a .sof file will be generated in your specified directory. Follow these steps to program the hardware example design on the Intel Arria 10:
    - **a.** On the Tools menu, click Programmer.
    - **b.** In the Programmer, click Hardware Setup.
    - **c.** Select a programming device.
    - **d.** Select and add the Intel Arria 10 GX Transceiver Signal Integrity Development Kit to which your Intel Quartus Prime session can connect.
    - **e.** Ensure that Mode is set to JTAG.
    - **f.** Select the Arria 10 device and click Add Device. The Programmer displays a block diagram of the connections between the devices on your board.
    - **g.** In the row with your .sof, check the box for the .sof.
    - **h.** Check the box in the Program/Configure column.

- **i.** Click Start.

5. After the hardware example design is configured on the Intel Arria 10 device, in the Intel Quartus Prime software, on the Tools menu, click System Debugging Tools > System Console.
6. In the Tcl Console pane, type sysconsole_testbench.tcl.
7. Type run_example_design.

The example design demonstrate the functionalities of the 50G Interlaken IP core. You can generate the design from the Example Design tab of the 50G Interlaken graphical user interface (GUI) in the IP parameter editor.

Features

- Internal TX to RX serial loopback mode.
- Automatically generates fixed size packets.
- Basic packet checking capabilities.
- You can use system console to reset the design for re-testing purpose.

Hardware and Software Requirements

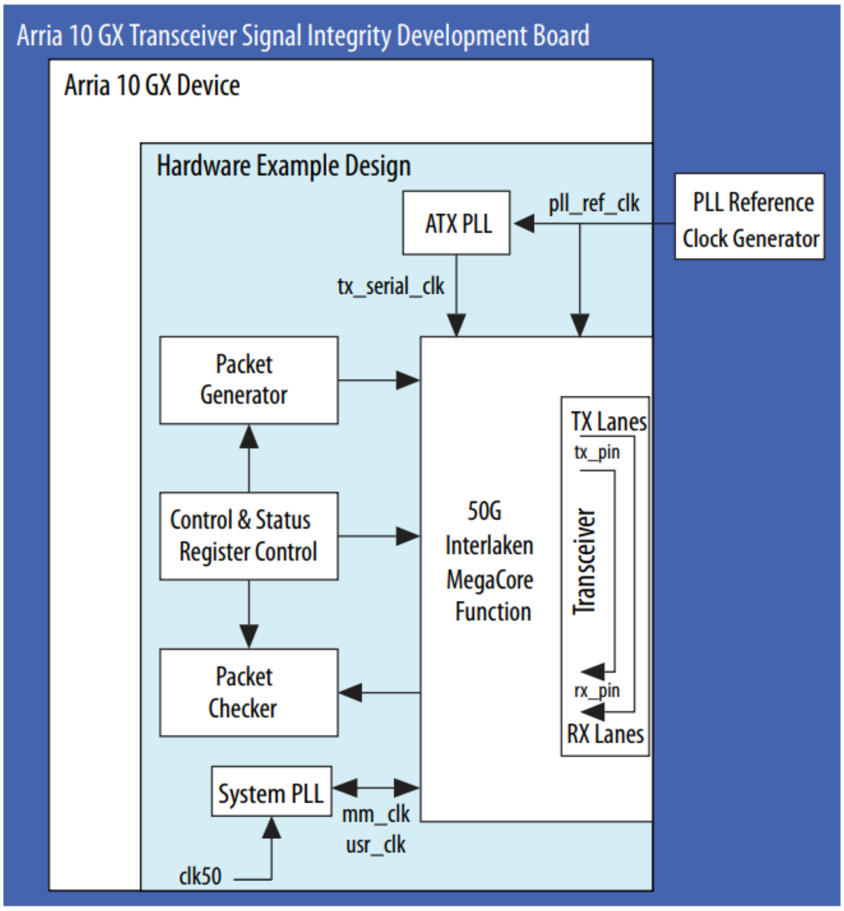
You can use the following hardware and software to test the example design:

- Intel Quartus Prime software
- System Console
- VCS, ModelSim SE, Xcelium, QuestaSim, or Questa Intel FPGA Edition simulator
- Intel Arria 10 GX Transceiver Signal Integrity Development Kit for hardware testing

Functional Description

The hardware example design connects system and PLL reference clocks and required design components. After you program the device on the Arria 10 GX transceiver signal integrity development board, the example design configures the IP core in internal loopback mode and generates packets on the IP core TX user data transfer interface. The IP core sends these packets on the internal loopback path through the transceiver. After the IP core receiver receives the packets on the loopback path, it processes the Interlaken packets and transmits them on the RX user data transfer interface. The example design checks that the packets it receives on the IP core RX user data transfer interface are consistent with the packets sent in.

Arria 10 50G Interlaken IP Core Example Design Block Diagram



The hardware example design includes external PLLs. You can examine the clear text files to view sample code that implements one possible method to connect external PLLs to the 50G Interlaken IP core.

The hardware example design packs six Interlaken lanes in a transceiver block, and connects all of the channels in the same transceiver block to a single ATX PLL. The IP core connects ATX PLL to the 50G Interlaken IP core tx_pll_locked and tx_pll_powerdown ports. This simple connection model is only one of many options available to you for configuring and connecting the external PLLs in your 50G Interlaken design.

Related Information

- Arria 10 GX Transceiver Signal Integrity Development Kit product webpage
- 50G Interlaken IP User Guide

Example Design Behavior

Immediately following configuration on the Arria 10 device, when you type run_example_design in system console, the 50G Interlaken IP core hardware example design performs the following actions:

1. Resets the 50G Interlaken IP core.
2. Configures the 50G Interlaken IP core in internal loopback mode.
3. Sends a sequence of 100 256-byte Interlaken packets with predefined data in the payload to the TX user data transfer interface of the IP core.
4. Checks the received packets and reports the status.

The packet checker included in the hardware example design provides the following basic packet checking capabilities:

- Checks that the transmitted packet sequence is not violated
- Checks that the received data matches expected values

Interface Signals

Table 2-1: Arria 10 50G Interlaken IP Core Hardware Example Design Signals

Port Name	Direction	Width (Bits)	Description
clk50	Input	1	System clock input. Clock frequency must be 50 MHz.
pll_ref_clk	Input	1	Transceiver reference clock. Drives the RX CDR PLL.
rx_pin	Input	Number of lanes	Receiver SERDES data pin.
tx_pin	Output	Number of lanes	Transmit SERDES data pin.
sys_pll_reset_n	Input	1	System reset.

Register Map

Table 2-2: Example Design Register Map

Offset	Name	Access	Description
8’h00	Reserved		
8’h01	Reserved		

Register Map

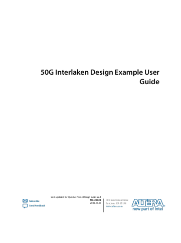
Offset	Name	Access	Description
8’h02	System PLL reset	RO	Following bits indicates system PLL reset request and enable value: • Bit [0] – sys_pll_rst_req • Bit [1] – sys_pll_rst_en
8’h03	RX lane aligned	RO	Indicates the RX lane alignment.
8’h04	WORD locked	RO	[NUM_LANES–1:0] – Word (block) boundaries id entification.
8’h05	Sync locked	RO	[NUM_LANES–1:0] – Metaframe synchroni- zatio n.
8’h06 – 8’h09	CRC32 error count	RO	Indicates the CRC32 error count.
8’h0A	CRC24 error count	RO	Indicates the CRC24 error count.
8’h0B	Overflow/Underflow signal	RO	Following bits indicate: • Bit [3] – TX underflow signal • Bit [2] – TX overflow signal • Bit [1] – RX overflow signal
8’h0C	SOP count	RO	Indicates the number of SOP.
8’h0D	EOP count	RO	Indicates the number of EOP
8’h0E	Error count	RO	Indicates the number of following errors: • Loss of lane alignment • Illegal control word • Illegal framing pattern • Missing SOP or EOP indicator
8’h0F	send_data_mm_clk	RW	Write 1 to enable the generator signal.
8’h10	Reserved		
8’h11	System PLL lock	RO	PLL lock indication.

- **Note:** Example design register address starts with 0x20** while the 50G Interlaken core register address starts with 0x10**.
- Access code: RO—Read Only, and RW—Read/Write.
- System console reads the example design registers and reports the test status on the screen.

Document Revision History for 50G Interlaken Design Example User Guide

Date	Changes
2022.10.31	Added support for the Xcelium simulator.
2021.10.04	Updated simulator information in section: *Simulating the Design* and *Hardware and Software Requirements*.
2018.03.22	Made following changes to *Simulating the Design* section: • Corrected simulation directory location. • Updated command to simulate the testbench in NCSim and VCS simulators. • Updated simulation ends display message.
2016.10.31	• Changed the title to *50G Interlaken Design Example User Guide*. • Corrected the Figure: *Arria 10 50G Interlaken IP Core Example Design Block Diagram*. • Updated the Figure: *Directory Structure for the Generated Example Design*.
2016.05.02	Initial release

Documents / Resources

 50G Interlaken Design Example User Guide Subscribe Send Feedback Last updated for Quartus Prime Design Suite: 22.1 UG-20023 2022.10.31 101 Innovation Drive San Jose, CA 95134 www.altera.com ALTERA now part of Intel	**intel 50G Interlaken Design Example** [pdf] User Guide 50G Interlaken Design Example, Interlaken Design Example, Design Example