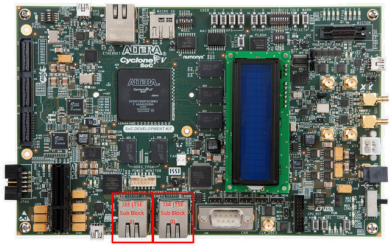

25G Ethernet Intel FPGA IP User Guide

25G Ethernet Intel® FPGA IP Release Notes
User Guide

Contents

25G Ethernet Intel FPGA IP Release Notes (Intel Agilex Devices)

Intel® FPGA IP versions match the Intel Quartus® Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.
The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

1.1. 25G Ethernet Intel FPGA IP v1.0.0

Table 1. v1.0.0 2022.09.26

Intel Quartus Prime Version	Description	Impact
22.3	Added support for Intel Agilex™ F-tile device family. • Only 25G speed rate is supported. • 1588 Precision Time Protocol is not supported.	—

25G Ethernet Intel FPGA IP Release Notes (Intel Stratix 10 Devices)

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the Intel Quartus Prime Design Suite Update Release Notes.
Intel FPGA IP versions match the Intel Quartus Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel
FPGA IP has a new versioning scheme.
The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

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Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- 25G Ethernet Intel Stratix®10 FPGA IP User Guide Archives
- 25G Ethernet Intel Stratix® 10 FPGA IP Design Example User Guide Archives
- Errata for the 25G Ethernet Intel FPGA IP in the Knowledge Base

2.1. 25G Ethernet Intel FPGA IP v19.4.1

Table 2. v19.4.1 2020.12.14

Intel Quartus Prime Version	Description	Impact
20.4	Length checking update on VLAN frames: • In previous versions of 25G Ethernet Intel FPGA IP, oversized frame error is asserted when the following conditions are met: 1. VLAN a. VLAN detection is enabled. b. The IP transmits/receives frames with length amounting to the maximum TX/RX frame length plus 1 to 4 octets. 2. SVLAN a. SVLAN detection is enabled. b. The IP transmits/receives frames with length amounting to the maximum TX/RX frame length plus 1 to 8 octets. • In this version, the IP is updated to correct this behavior.	—
	Updated the Avalon® memory-mapped interface access to the status_* interface to prevent Avalon memory-mapped timeout during reads to nonexistent addresses: • In previous versions of 25G Ethernet Intel FPGA IP, Avalon memory-mapped interface reads to non-existent addresses on the status_* interface would assert status_waitrequest until the Avalon memorymapped master's request times out. The issue has now been fixed to not hold waitrequest when a non-existent address is accessed.	—
	RS-FEC enabled variants now support 100% throughput.	—

2.2. 25G Ethernet Intel FPGA IP v19.4.0

Table 3. v19.4.0 2019.12.16

Intel Quartus Prime Version	Description	Impact
19.4	rx_am_lock behavior change: • In previous versions of the 25G Ethernet Intel FPGA IP, the rx_am_lock signal behaves the same as rx_block_lock across all variants. • In this version, for RSFEC enabled variants of the IP, rx_am_lock now asserts when alignment lock is achieved. For non-RSFEC enabled variants, rx_am_lock still behaves the same as rx_block_lock.	The interface signal, rx_am_lock, behaves differently from the previous versions for the RSFEC-enabled variants.
	Updated the RX MAC Start of Packet: • In previous versions, the RX MAC only checks for a START character to determine the start of a packet. • In this version, the RX MAC now checks for incoming packets for Start of Frame Delimiter (SFD), in addition to the START character by default. • If the preamble pass-through mode is enabled, the MAC checks only for the START character to allow for custom preamble.	—
Added a new register to enable preamble checking: • In the RX MAC registers, the register at offset 0x50A [4] can be written to 1 to enable the preamble checking. This register is a “don’t care” when the preamble pass-through is enabled.	—	

2.3. 25G Ethernet Intel FPGA IP v19.3.0

Table 4. v19.3.0 2019.09.30

Intel Quartus Prime Version	Description	Impact
19.3	For a MAC+PCS+PMA variant, the transceiver wrapper module name is now dynamically generated. This prevents unwanted module collision if multiple instances of the IP are being used in a system.	—

2.4. 25G Ethernet Intel FPGA IP v19.2.0

Table 5. v19.2.0 2019.07.01

Intel Quartus Prime Version	Description	Impact
19.2	Design Example for 25G Ethernet Intel FPGA IP: • Updated the target development kit option for Intel Stratix® 10 devices from Intel Stratix 10 L-Tile GX Transceiver Signal Integrity Development Kit to Intel Stratix 10 10 GX Signal Integrity L-Tile (Production) Development Kit.	—

2.5. 25G Ethernet Intel FPGA IP v19.1

Table 6. v19.1 April 2019

Description	Impact
Added a new feature—Adaptive mode for RX PMA Adaptation: • Added a new parameter—Enable auto adaptation triggering for RX PMA CTLE/DFE mode.	These changes are optional. If you do not upgrade your IP core, it does not have this new feature.
Renamed the Enable Altera Debug Master Endpoint (ADME) parameter to Enable Native PHY Debug Master Endpoint (NPDME) as per Intel rebranding in the Intel Quartus Prime Pro Edition software. The Intel Quartus Prime Standard Edition software still uses Enable Altera Debug Master Endpoint (ADME).	—

2.6. 25G Ethernet Intel FPGA IP v18.1

Table 7. Version 18.1 September 2018

Description	Impact
Added a new feature—Elective PMA: • Added a new parameter—Core Variants.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
• Added a new signal for 1588 Precision Time Protocol Interface—latency_sclk.	
Design Example for 25G Ethernet Intel FPGA IP: Renamed the target development kit option for Intel Stratix 10 devices from Stratix 10 GX FPGA Development Kit to Stratix 10 L-Tile GX Transceiver Signal Integrity Development Kit.	—

Related Information

- 25G Ethernet Intel Stratix 10 FPGA IP User Guide
- 25G Ethernet Intel Stratix 10 FPGA IP Design Example User Guide
- Errata for 25G Ethernet IP core in the Knowledge Base

2.7. 25G Ethernet Intel FPGA IP v18.0

Table 8. Version 18.0 May 2018

Description	Impact
Initial release for Intel Stratix 10 devices.	—

2.8. 25G Ethernet Intel Stratix 10 FPGA IP User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.
If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
20.3	19.4.0	25G Ethernet Intel Stratix 10 FPGA IP User Guide
20.1	19.4.0	25G Ethernet Intel Stratix 10 FPGA IP User Guide
19.4	19.4.0	25G Ethernet Intel Stratix 10 FPGA IP User Guide
19.3	19.3.0	25G Ethernet Intel Stratix 10 FPGA IP User Guide
19.2	19.2.0	25G Ethernet Intel Stratix 10 FPGA IP User Guide
19.1	19.1	25G Ethernet Intel Stratix 10 FPGA IP User Guide
18.1	18.1	25G Ethernet Intel Stratix 10 FPGA IP User Guide
18.0	18.0	25G Ethernet Intel Stratix 10 FPGA IP User Guide

2.9. 25G Ethernet Intel Stratix 10 FPGA IP Design Example User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.
If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
19.1	19.1	25G Ethernet Intel Stratix 10 FPGA IP Design Example User Guide
18.1	18.1	25G Ethernet Intel Stratix 10 FPGA IP Design Example User Guide
18.0	18.0	25G Ethernet Intel Stratix 10 FPGA IP Design Example User Guide

25G Ethernet Intel FPGA IP Release Notes (Intel Arria 10 Devices)

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the Intel Quartus Prime Design Suite Update Release Notes.
Intel FPGA IP versions match the Intel Quartus Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.
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Related Information

- Intel Quartus Prime Design Suite Update Release Notes

- 25G Ethernet Intel Arria® 10 FPGA IP User Guide
- 25G Ethernet Intel Arria® 10 FPGA IP Design Example User Guide
- Errata for the 25G Ethernet Intel FPGA IP in the Knowledge Base

3.1. 25G Ethernet Intel FPGA IP v19.4.1

Table 9. v19.4.1 2020.12.14

Intel Quartus Prime Version	Description	Impact
20.4	Length checking update on VLAN frames: • In previous versions of 25G Ethernet Intel FPGA IP, oversized frame error is asserted when the following conditions are met: 1. VLAN a. VLAN detection is enabled. b. The IP transmits/receives frames with length amounting to the maximum TX/RX frame length plus 1 to 4 octets. 2. SVLAN a. SVLAN detection is enabled. b. The IP transmits/receives frames with length amounting to the maximum TX/RX frame length plus 1 to 8 octets. • In this version, the IP is updated to correct this behavior.	—
	Updated the Avalon memory-mapped interface access to the status_* interface to prevent Avalon memory-mapped timeout during reads to non existent addresses: • The IP is updated to de-assert waitrequest when a non-existent address is accessed on the status_* interface.	

3.2. 25G Ethernet Intel FPGA IP v19.4.0

Table 10. v19.4.0 2019.12.16

Intel Quartus Prime Version	Description	Impact
19.4	rx_am_lock behavior change: • In previous versions of the 25G Ethernet Intel FPGA IP, the rx_am_lock signal behaves the same as rx_block_lock across all variants. • In this version, for RSFEC enabled variants of the IP, rx_am_lock now asserts when alignment lock is achieved. For non-RSFEC enabled variants, rx_am_lock still behaves the same as rx_block_lock.	The interface signal, rx_am_lock, behaves differently from the previous versions for the RSFEC-enabled variants.
	Updated the RX MAC Start of Packet: • In previous versions, the RX MAC only checks for a START character to determine the start of a packet. • In this version, the RX MAC now checks for incoming packets for Start of Frame Delimiter (SFD), in addition to the START character by default. • If the preamble pass-through mode is enabled, the MAC checks only for the START character to allow for custom preamble.	—
	Added a new register to enable preamble checking: • In the RX MAC registers, the register at offset 0x50A [4] can be written to 1 to enable the preamble checking. This register is a “don’t care” when the preamble pass-through is enabled.	—

3.3. 25G Ethernet Intel FPGA IP v19.1

Table 11. v19.1 April 2019

Description	Impact
Renamed the Enable Altera Debug Master Endpoint (ADME) parameter to Enable Native PHY Debug Master Endpoint (NPDME) as per Intel rebranding in the Intel Quartus Prime Pro Edition software. The Intel Quartus Prime Standard Edition software still uses Enable Altera Debug Master Endpoint (ADME).	—

3.4. 25G Ethernet IP Core v17.0

Table 12. Version 17.0 May 2017

Description	Impact
Added shadow feature for reading statistics registers. • In TX statistics registers, replaced the CLEAR_TX_STATS register at offset 0x845 with new CNTR_TX_CONFIG register. The new register adds a shadow request and a parity-error clear bit to the bit that clears all TX statistics registers. Added new CNTR_RX_STATUS register at offset 0x846, that includes a parity-error bit and a status bit for the shadow request. • In RX statistics registers, replaced the CLEAR_RX_STATS register at offset 0x945 with new CNTR_RX_CONFIG register.The new register adds a shadow request and a parity-error clear bit to the bit that clears all TX statistics registers. Added new CNTR_TX_STATUS register at offset 0x946, that includes a parity-error bit and a status bit for the shadow request.	The new feature supports improved reliability in statistics counter reads. To read a statistics counter, first set the shadow request bit for that set of registers (RX or TX), and then read from a snapshot of the register. The read values stop incrementing while the shadow feature is in effect, but the underlying counters continue to increment. After you reset the request, the counters resume their accumulated values. In addition, the new register fields include parityerror status and clear bits.
Modified RS-FEC alignment marker format to comply with the now-finalized Clause 108 of the IEEE 802.3by specification. Previously the RS-FEC feature complied with the 25G/50G Consortium Schedule 3, prior to IEEE specification finalization.	The RX RS-FEC now detects and locks to both the old and new alignment markers, but the TX RS-FEC generates only the new IEEE alignment marker format.

Related Information

- 25G Ethernet IP Core User Guide
- Errata for 25G Ethernet IP core in the Knowledge Base

3.5. 25G Ethernet IP Core v16.1

Table 13. Version 16.1 October 2016

Description	Impact
Initial release in the Intel FPGA IP Library.	—

Related Information

- 25G Ethernet IP Core User Guide
- Errata for 25G Ethernet IP core in the Knowledge Base

3.6. 25G Ethernet Intel Arria® 10 FPGA IP User Guide Archive

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.
If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Version	User Guide
20.3	19.4.0	25G Ethernet Intel Arria® 10 FPGA IP User Guide
19.4	19.4.0	25G Ethernet Intel Arria 10 FPGA IP User Guide
17.0	17.0	25G Ethernet Intel Arria 10 FPGA IP User Guide

3.7. 25G Ethernet Intel Arria 10 FPGA IP Design Example User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.
If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
16.1	16.1	25G Ethernet Design Example User Guide

25G Ethernet Intel® FPGA IP Release Notes

Online Version

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ID: 683067

Version: 2022.09.26

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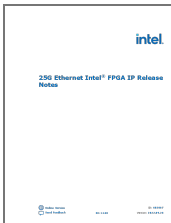	intel 25G Ethernet Intel FPGA IP [pdf] User Guide 25G Ethernet Intel FPGA IP, Ethernet Intel FPGA IP, Intel FPGA IP, FPGA IP, IP

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- 9. 25G Ethernet Intel® Stratix® 10 FPGA IP User Guide Archives
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