HOPERF CMT453x Series Bluetooth SOC User Guide

User Guide
CMT453x SDK User Guide

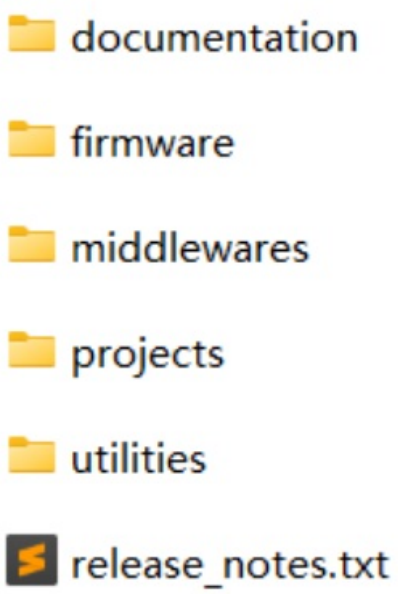
Contents

Introduction

This document is to help users to quickly familiarize with the development kit for CMT453x series Bluetooth SOC and Keil MDK-ARM settings.

Directory structure of SDK/ development firmware files

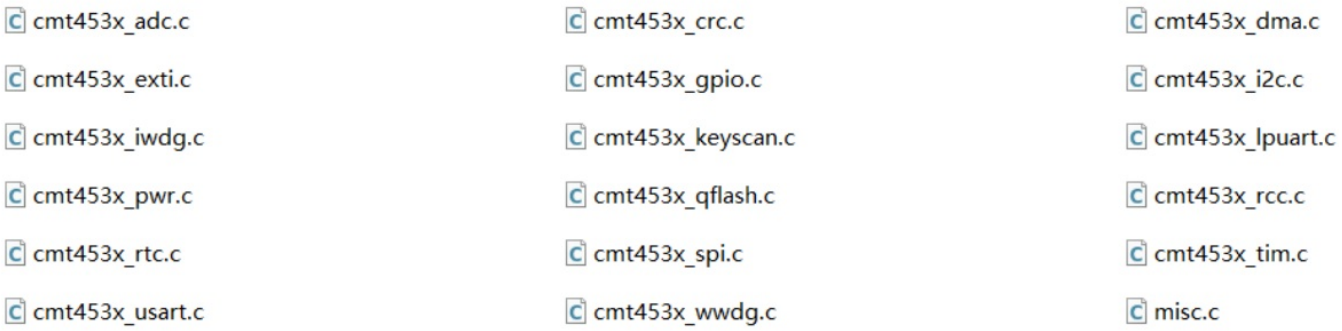
Under the SDK directory, it is a file named after the firmware library version, which contains five subfolders:



1.1 documentation
Development documentations that include the user manual and application notes.
1.2 firmware
■ CMSIS:
Cortex Microcontroller Software Interface Standard (CMSIS) is a vendor-independent hardware abstraction layer of Cortex-M processor series. CMSIS provides a general interface between core and peripherals, real-time operating system and intermediate devices.

- It contains the name definition, address definition and configuration functions of the register used to access the core. The interface includes the definition of debug channel.
- It provides the definition of all peripherals on the chip, including all peripheral register header files, startup files and system initialization template files.

■ CMT453x_std_periph_driver:
Standard driver functions of chip peripherals, including source files of .c and header files of .h. Users can transplant to the project and quickly complete the use of a peripheral module.



1.3 Middleware
The middleware mainly includes the following two directories:
■ Third_Party

- Free RTOS: Free RTOS related library

■ HopeRF

- ble_library: BLE related library
- hp_ble_stack: Ble Bluetooth protocol stack header file
- hp_ble_profile: Ble profile library source code
- hp_library: Other library source code of ble program, including log, sleep and timer, etc.

1.4 Utilities
Utility software directory, which mainly includes:
■ **dfu**
Software directory of dfu firmware upgrade related tools and bat scripts for calling these tools

- Image: bin file generated by bat script and bin file used for DFU demo.
- J Link: burning tool
- Keys: keys used to generate dfu upgrade bin
- Android Util: DFU test APK
- HP Util: serial port upgrade utility software and source code

1.5 Projects
Projects directory contains a development board directory, which includes:

■ bsp: log function with printing by debugging serial port, which is used for peripheral demo to respond to various debugging information during debugging.
■ application: application demo, a comprehensive demo that uses a variety of peripherals or functional requirements.

- peripheral_alone: Integrated peripheral demo, including serial communication, PWM output of TIM, ADC reading and voltage conversion, IO output, IO input interrupt response and RTC sleep wake-up.
- Free RTOS: Freetos related demo

■ ble_peripheral: BLE peripheral demo, to understand the basic method to develop BLE program through the BLE demo of specific profiles

- ble_basic: device service demo
- ble_blood_pressure: BLE blood pressure service demo.
- ble_heart_rate: BLE heart rate service demo
- ble_hid_mouse: BLE mouse demo
- ble_rdts_peripheral: BLE data transmission peripheral demo (128bit UUID), including DFU OTA upgrade project options.
- ble_rdts_peripheral_16bit: BLE data transmission peripheral demo (16bit UUID), including DFU OTA upgrade project options.
- ble_rdts_peripheral_3p: BLE data transmission peripheral demo which can connect 3 central devices.

■ ble_central: BLE central demo

- ble_rdts_central: BLE data transmission central demo. It can be used with the rdtss demo.
- ble_rdts_central_peripheral: BLE data transmission demo with central and peripheral mode switching . It can be used with rdtss or central_rdtsc demo.

- ble_ rdts_central_3c: BLE data transmission central demo which can connect 3 peripheral devices.
- ble_relay_1central_1peripheral: BLE data transmission relay demo, that is, one central and one peripheral work at the same time. It can be used with the rdtss demo.

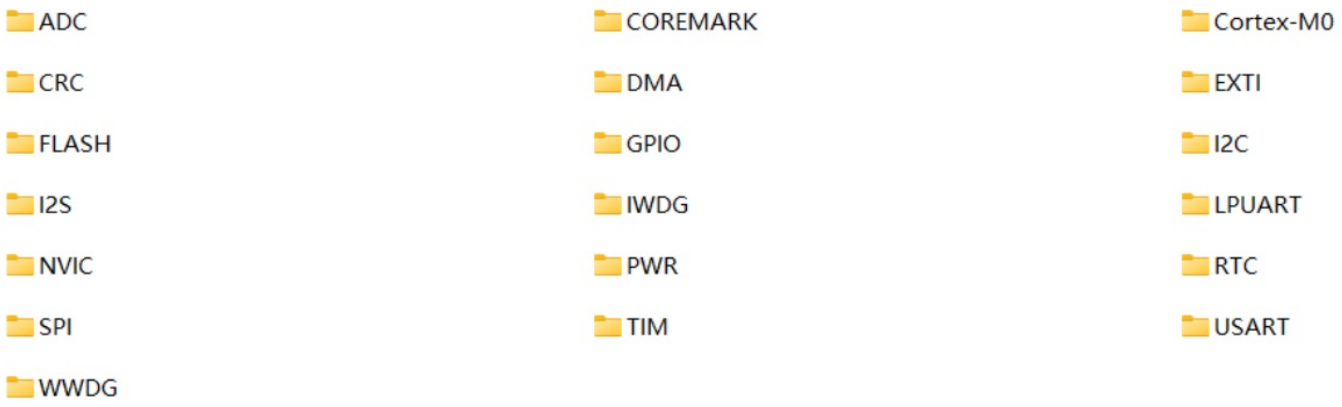
■ ble_dfu: Device firmware upgrade demo

- common: Dfu common library directory
- app_ota: BLE over-the-air upgrade demo
- image_update: in single bank mode, the source code of image_update demo
- app_usart: serial port upgrade demo (jump to masterboot)
- masterboot: firmware upgrade boot, including serial port upgrade, firmware checksum jump.

■ ble_prod_test: product test demo

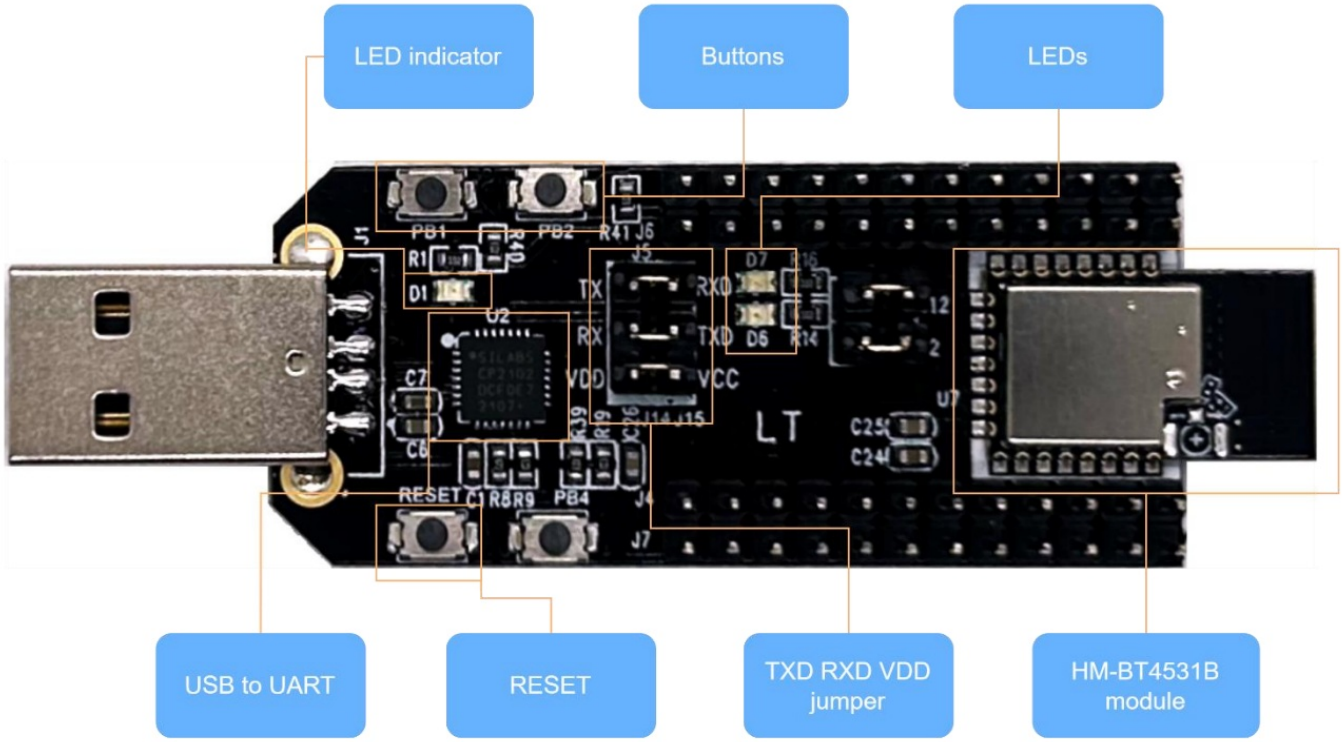
- DTM_Test: support standard HCI DTM command via USART1(PB6, PB7), it need connect with Bluetooth tester running the test.
- RF_Test: support BLE TX, RX, and constant carrier TX mode via UART commands, the UART command can send by pc software.

■ peripheral: It contains demo items of each peripheral function module, and realizes the basic function application development of each peripheral module. Users can quickly understand the use of chip peripherals through these demo items.



CMT4531 dongle board

To develop and/or evaluate the CMT4531, the dongle board below can be used which comes with a HM-BT4531B module, USB to UART interface, LEDs, buttons and additional components.
The CMT4531 EVB incorporates a HM-BT4531B module featuring 32-bit Cortex®-M0 core, 256 kB of flash memory, 48 kB of RAM and a 2.4 GHz band transceiver with output power up to 6 dBm. For additional information on the CMT4531, refer to the data sheet.



Index	Function	Description
1	USB Type-A	USB connector as the main power source of the dongle board and debug port
2	CP2102	USB-to-UART interface
3	RESET button	Reset the CMT4531
4	UART RXD jumper	UART RXD jumper, connect to the PB7
5	UART TXD jumper	UART TXD jumper, connect to the PB6
6	VDD jumper	3.3V power rail
7	HM-BT4531B	HM-BT4531B BLE module
8	LED indicator	LED indicats the dongle board is powered or not.
9	Buttons	GPIO button (PB1, PB2, PB4)
10	LEDs	LED (PB0, PA6)

Dongle Board Connector Pin Associations
The figure below shows the mapping of the pin connector on the CMT4531 dongle board.

VDD	VDD
SWDIO	GND
SWCLK	GND
PB3	PB6
PB2	PB7
PB1	PB4
PA6	PB5
PB0	PB10
PA0	PB12
PA2	PB11
PA1	PB13
PA0	RESET

Project Configuration and Burning

3.1 Compilation environment installation

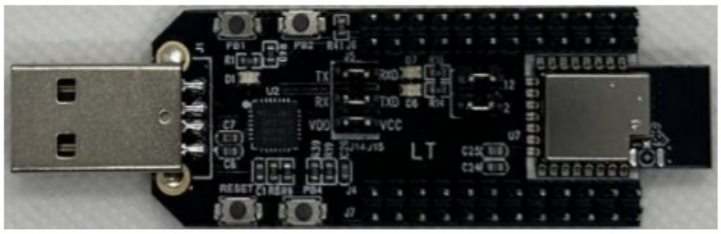
Please install KEIL MDK-ARM development environment, which requires a version V5.00 or above, and V5.24.2.0 is recommended.

3.2 Support package installation

Double-click CMT453X_DFP.1.1.0.pack to install the Keil Chip support package.

3.3 Connect to the Programmer

The CMT4531 integrates JTAG and serial single-wire debugging interface. Connect the SEGGER J-Link debugger to the SWD interface of CMT4531 (SWCLK/SWDIO/RESET), and keep the CMT4531 power on.



3.4 Build environment configuration

Note: All demo have been configured as follows, so there is no need to reconfigure the build environment to run demo.

■ The FLASH and RAM configuration of Target page

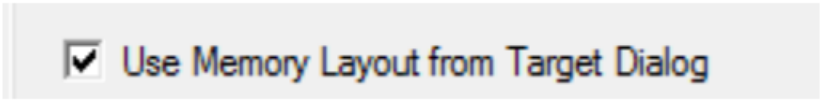
- It does not contain ble function items.

- Target page containing ble function items

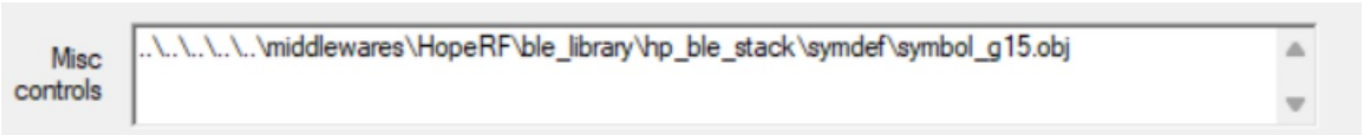
- For items with DFU function, please refer to the “irmware upgrade user guide.pdf”.

■ **Linker page**

- Check the memory configuration of the Target page.

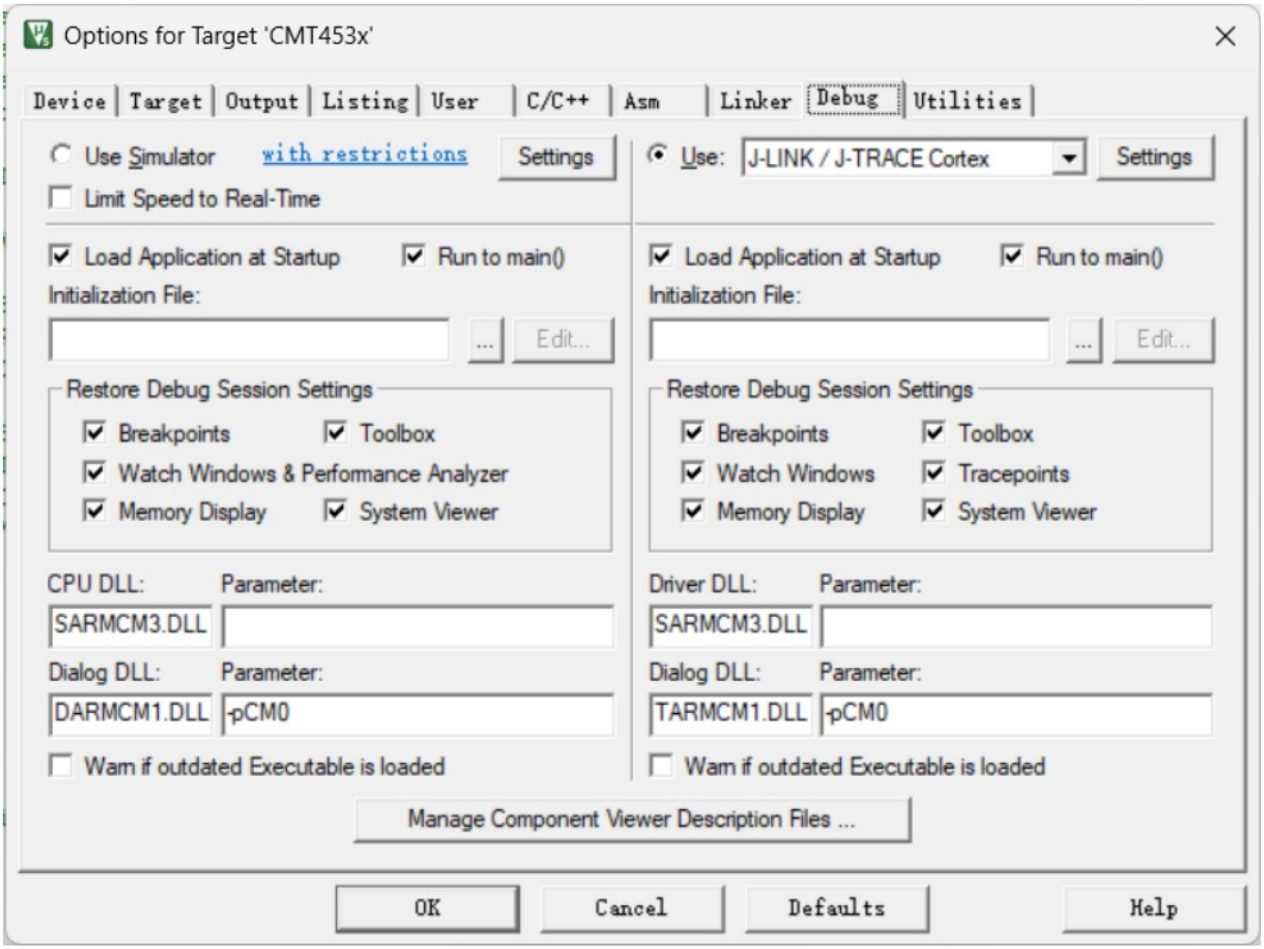


- For items with ble, add middlewares\HopeRF\ble_library\hp_ble_stack\symdef\symbol_g15.obj to Misc control. Note that the obj file used by the program with Bluetooth central function is symbol _ g15 _ central.obj.



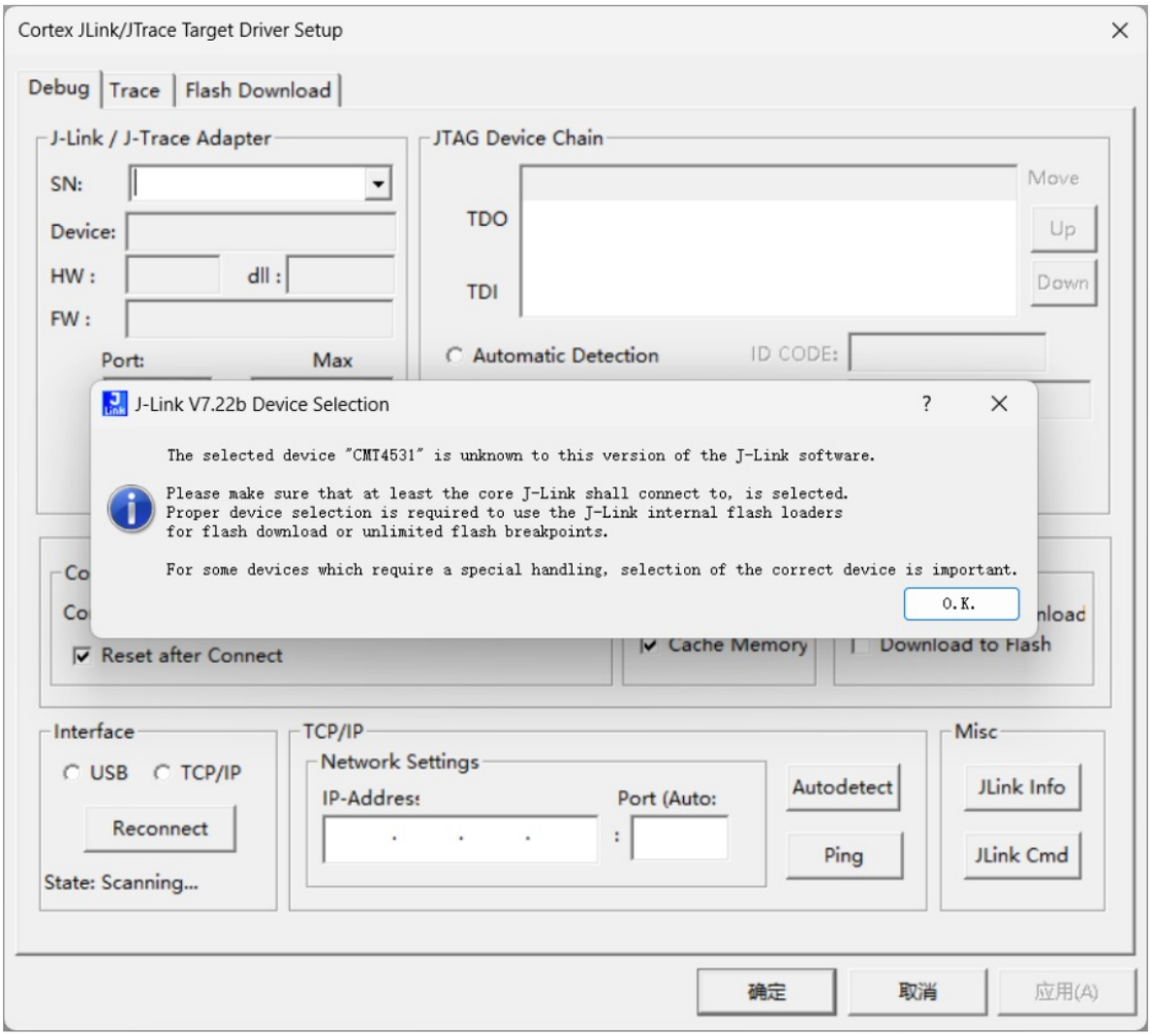
■ Debug Page

- Select the debugger J-Link/J-TRACE Cortex.

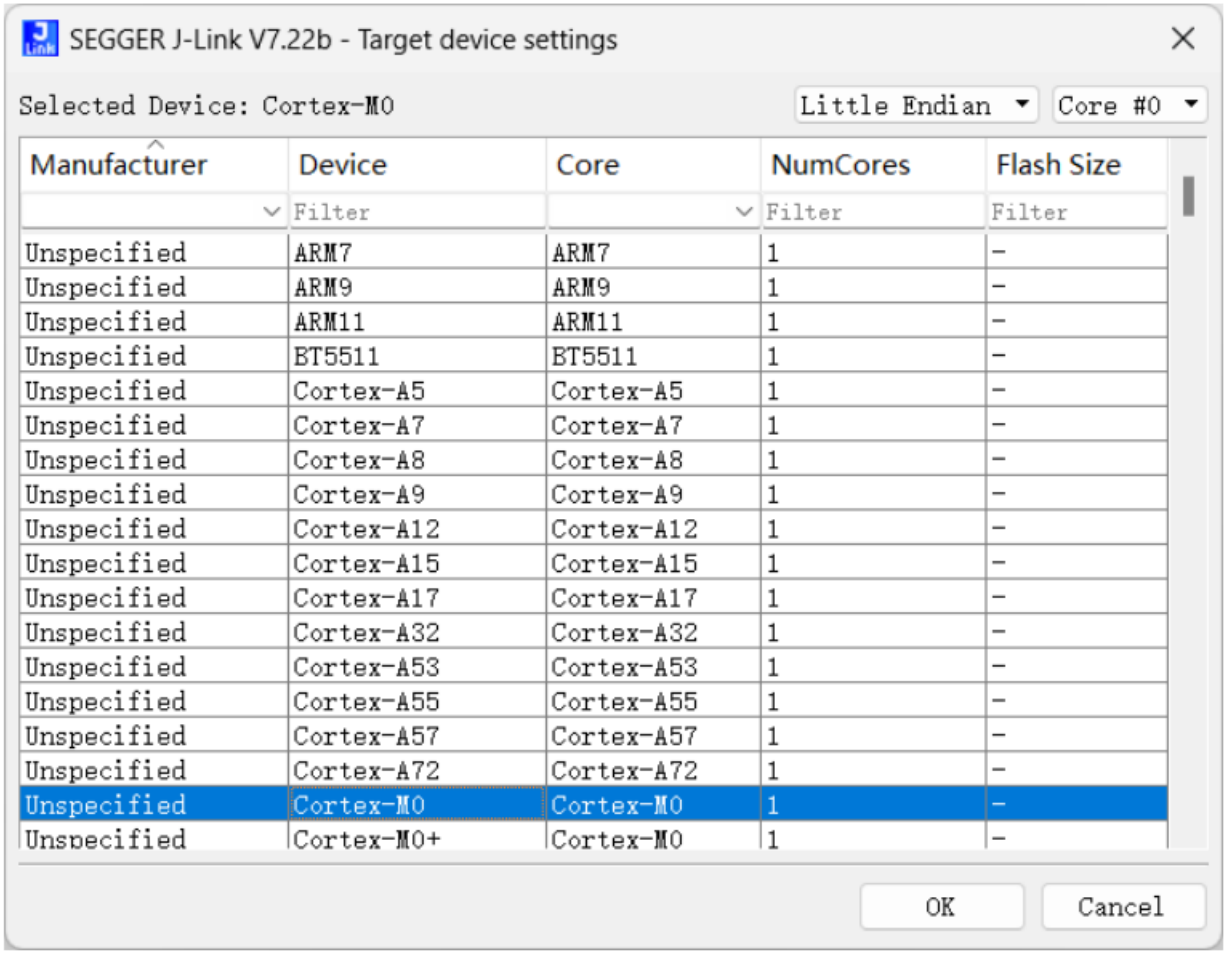


- The setting page is as follows

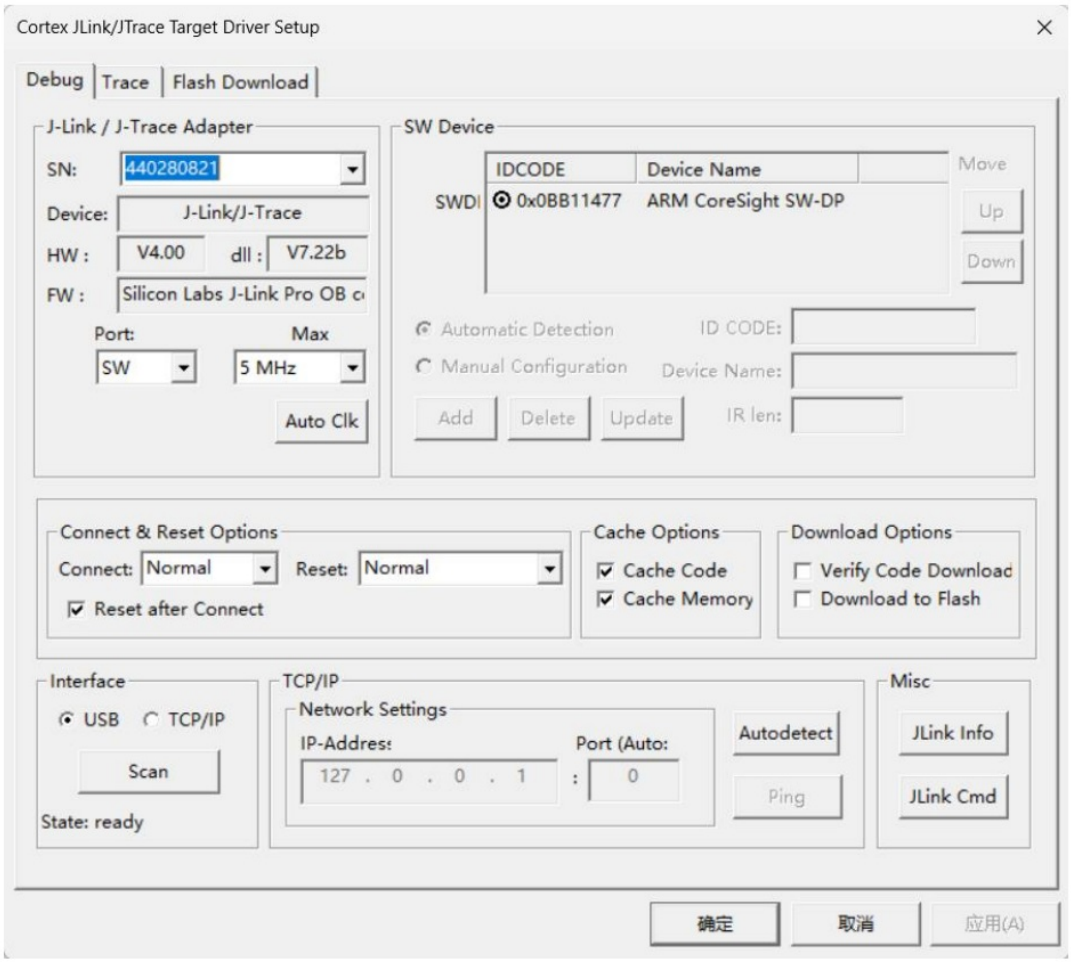
  Click Settings and you are presented with the dialog below for selecting the correct device.



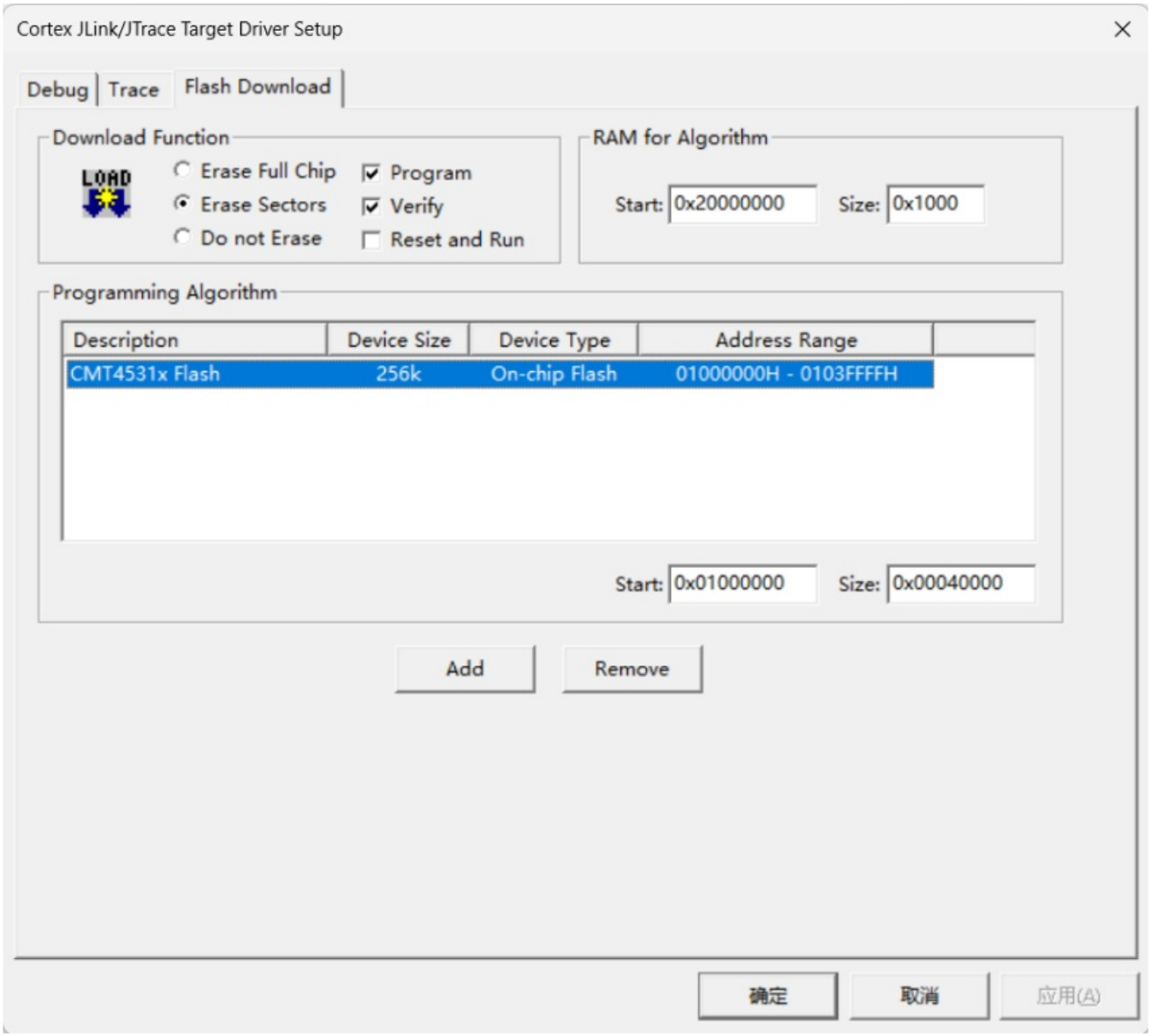
Select the device as Cortex-M0 and click OK.



Keil will detect the J-Link debugger connected to the PC. Select the right serial number and select the port as “SW”.



Check the Flash Download setting and make sure the Programming Algorithm is CMT453x.FLM, otherwise, you need to add it manually.



3.5 Build and Download

■ Build: click the build button on the menu.

■ Download: Click the Download button on the menu..

■ Debug: Click the start/stop debug session button on the menu..

Note: After downloading the program, you can't continue to download it.

■ Possibility 1: SWDIO/SWDCLK in the code is used for other purposes, resulting in the failure of the simulation interface. Generally, it is not recommended to use simulation pins for other functional design.

■ Possibility 2: When the chip enters the low-power sleep mode, the simulation interface fails, it needs to be downloaded in the wake-up state.

3.6 Structure of BLE project directory

Take ble_rdts_peripheral project as an example

■ Project Target

- CMT453x: BLE project, without DFU configuration. Generally, a ble project only has this target.
- OTA_IMG_1: OTA project with bluetooth, configured as Bank1 address.
- OTA_IMG_2: OTA project with bluetooth, configured as Bank2 address.

Note Must rebuild all the files after switch project target. The OTA_IMG_1 and OTA_IMG_2 target will copy the bin to \utilities\dfu\Image folder, user can run the bat script to download or create OTA package(zip format).

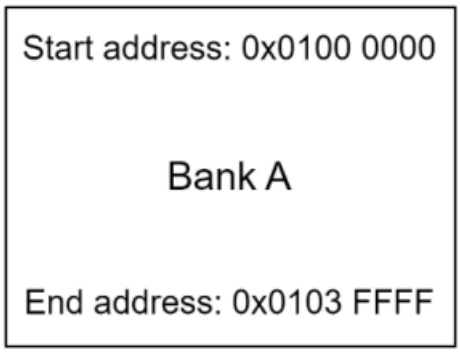
■ The directory structure is as follows

- STARTUP: chip startup file
- CMSIS: chip core configuration
- FWLB: Chip peripheral driver library
- BLE_STACK: BLE protocol stack
- BLE_PROFILE: BLE profile
- HP_DUF (optional): BLE OTA firmware upgrade related library
- Crypto (optional): Encryption-related library for BLE OTA firmware upgrade
- HP_LIB: BLE application related library
- BLE_APP: BLE application code
- USER: User application code
- CONFIG: configuration file
- DOC: Descriptive document

Memory Allocation

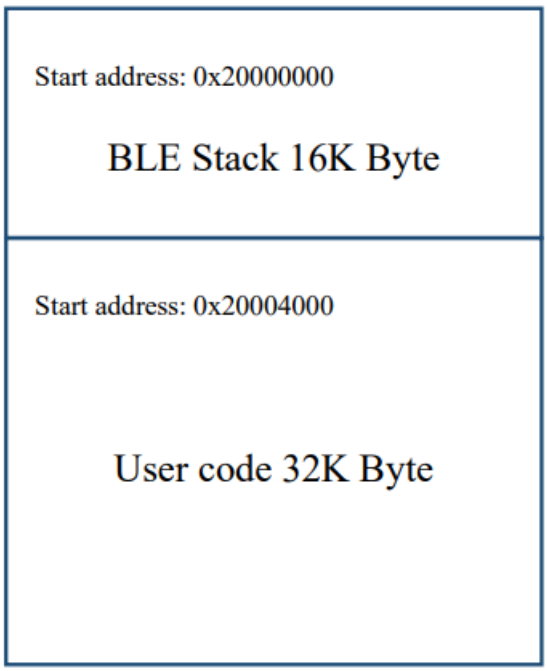
4.1 Flash allocation

The FLASH address range of chip CMT4531 is 0x01000000 – 0x0103FFFF, with a total space of 256K bytes. It's BankA and the user code can run in the bank by default.
To use the firmware upgrade function, please refer to the "FLASH memory distribution" chapter of the "firmware upgrade user guide.pdf".



4.2 RAM

The RAM address range of chip CMT4531 is 0x20000000 – 0x2000BFFF, with an available space of 48K bytes.
■ If the BLE function is enabled, the BLE protocol stack will occupy 0x20000000 – 0x20003FFF, with a total of 16K bytes of RAM, and the user code can use 0x20004000 – 0x2000BFFF, with a total of 32K bytes of RAM.
■ If the BLE function is disabled, the user code can use all 48K bytes of RAM.



BLE protocol stack is used

Not use the BLE protocol

System clock

5.1 Without BLE protocol stack application

The system clock source can be HSE or HSI, and all peripheral demo use HSI 64M as the system clock source by default. The low-speed clock source can be selected from the external crystal LSE 32.768K or the internal LSI 32K clock source.

5.2 BLE application

All BLE demo use HSI 64M as the system clock source by default, LSI as the low-speed clock source, and an external 32M crystal must be used as the dedicated clock source for BLE RF. It is not recommended to change the system clock source. The low-speed clock source can be external crystal LSE 32.768K or internal LSI 32K, but LSI or LSE can be configured only in the initialization function of BLE protocol stack and the low-speed clock source can be initialized. User code cannot switch to the low-speed clock source later, otherwise the function of BLE protocol stack will be affected.

History of Versions

Date	Version	Modification
5/23/2023	V1.3	Initial version
7/25/2023	V1.4	Add Firmware support package installation description.

Notice

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Documents / Resources

	HOPERF CMT453x Series Bluetooth SOC [pdf] User Guide CMT4531, CMT453x Series Bluetooth SOC, Bluetooth SOC, SOC

References

- Professional RF IC&modules and Digital Sensor designer and manufacturer Shenzhen Hope Microelectronics Co., Ltd
- Professional RF IC&modules and Digital Sensor designer and manufacturer Shenzhen Hope Microelectronics Co., Ltd