GOWIN IPUG902E CSC IP Programming For The Future





GOWIN IPUG902E CSC IP Programming For The Future User Guide

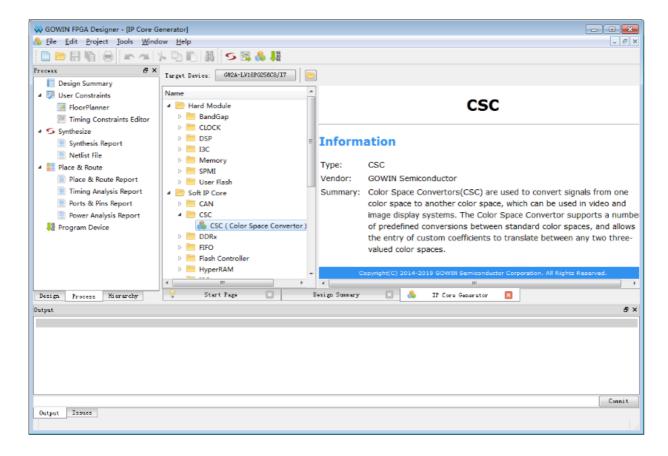
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GOWIN IPUG902E CSC IP Programming For The Future



Product Information

Specifications

Product Name: Gowin CSC IP
Model Number: IPUG902-2.0E

Trademark: Guangdong Gowin Semiconductor Corporation

• Registered Locations: China, U.S. Patent and Trademark Office, other countries

Product Usage Instructions

Overview

The Gowin CSC IP User Guide is designed to help users understand the features and functionality of the Gowin CSC IP. It provides detailed descriptions of functions, ports, timing, configuration, and reference design.

Functional Description

The functional description section provides in-depth information about the various functions and capabilities of the Gowin CSC IP.

Interface Configuration

This section guides users on how to configure interfaces for optimal performance and connectivity.

Reference Design

The reference design section offers insights into the recommended design layout for the Gowin CSC IP.

File Delivery

Details on document delivery, design source code encryption, and reference design are provided in this section.

What is the purpose of the Gowin CSC IP User Guide?

The purpose of the user guide is to assist users in understanding the features and usage of the Gowin CSC IP by providing detailed descriptions of functions, ports, timing, configuration, and reference design.

Are the software screenshots in the manual always up-to-date?

The software screenshots are based on version 1.9.9 Beta-6. As software is subject to change without notice, some information may not remain relevant and may need adjustments based on the software version in use.

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About This Guide

Purpose

The purpose of Gowin CSC IP User Guide is to help users quickly learn the features and usage of Gowin CSC IP by providing descriptions of the functions, ports, timing, configuration and call, reference design. The software screenshots in this manual are based on 1.9.9 Beta-6. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

Related Documents

The user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS100, GW1N series of FPGA Products Data Sheet
- DS117, GW1NR series of FPGA Products Data Sheet
- DS821, GW1NS series of FPGA Products Data Sheet
- DS861, GW1NSR series of FPGA Products Data Sheet
- DS891, GW1NSE series FPGA Products Data Sheet
- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- DS971, GW2AN-18X &9X Data Sheet
- DS976, GW2AN-55 Data Sheet
- DS961 GW2ANR series of FPGA Products Data Sheet
- DS981, GW5AT series of FPGA Products Data Sheet
- DS1104, GW5AST series of FPGA Products Data Sheet
- SUG100, Gowin Software User Guide

Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual. Table 1-1 Abbreviations and Terminology

Terminology and Abbreviations	Meaning
ВТ	Broadcasting Service (Television)
CSC	Color Space Convertor
DE	Data Enable
FPGA	Field Programmable Gate Array
HS	Horizontal Sync
IP	Intellectual Property
ITU	International Telecommunication Union
ITU-R	ITU-Radiocommunicationssector
RGB	R(Red) G(Green) B(Blue)
VESA	Video Electronics Standards Association
VS	Vertical Sync
YCbCr	Y(Luminance) CbCr(Chrominance)
YIQ	Y(Luminance) I(In-phase) Q(Quadrature-phase)
YUV	Y(Luminance) UV(Chrominance)

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: <u>www.gowinsemi.com</u>E-mail: <u>support@gowinsemi.com</u>

Overview

Color Space is the mathematical representation of a set of colors. The most common color models are RGB in computer graphics, YIQ, YUV, or YCbCr in video systems. Gowin CSC (Color Space Convertor) IP is used to realize different three-axis coordinates color space conversion, such as the common conversion between YCbCr and RGB.

Table 2-1 Gowin CSC IP

Gowin CSC IP	Gowin CSC IP			
Logic Resource	See <u>Table 2-2</u>			
Delivered Doc.				
Design File	Verilog (encrypted)			
Reference Design	Verilog			
TestBench Verilog				
Test and Design Flow				
Synthesis Software	GowinSynthesis			
Application Software	Gowin Software (V1.9.6.02Beta and above)			

Note!

For the devices supported, you can click here to get the information.

Features

- Supports YCbCr, RGB, YUV, YIQ three-axis coordinate color space conversion.
- Supports predefined BT601, BT709 standard color space conversion formula.
- · Support customized coefficient conversion formula
- · Support signed and unsigned data
- Supports 8, 10, 12 data bit widths.

Resource Utilization

Gowin CSC IP employs the Verilog language, which is used in the GW1N and GW2A FPGA devices. Table 2-2 presents an overview of the resource utilization. For the applications on the other GOWINSEMI FPGA devices, please see the later information.

Table 2-2 Resource Utilization

Device	GW1N-4	GW1N-4
Color Space	SDTV Studio RGB to YCbCr	SDTV Studio RGB to YCbCr
Data Width	8	12
Coefficient width	11	18
LUTs	97	106
Registers	126	129

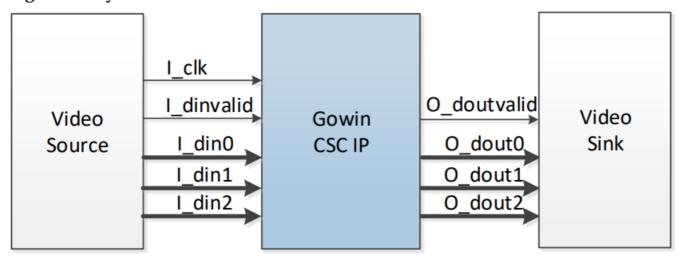
Functional Description

System Diagram

As shown in Figure 3-1, Gowin CSC IP receives three-component video data from video source and outputs in real time according to the selected conversion formula.

Figure 3-1 System Architecture

Figure 3-1 System Architecture



Working Principle

- Color space conversion is matrix operation. All color space can be derived from RGB information.
- Take the formula of color space conversion between RGB and YCbCr (HDTV, BT709) as an example:
 - RGB to YCbCr color space conversion
 - \circ Y709 = 0.213R + 0.715G + 0.072B
 - \circ Cb = -0.117R 0.394G + 0.511B + 128
 - \circ Cr = 0.511R 0.464G 0.047B + 128
 - YCbCr to RGB color space conversion
 - \circ R = Y709 + 1.540*(Cr 128)
 - \circ G = Y709 0.459*(Cr 128) 0.183*(Cb 128)
 - \bullet B = Y709 + 1.816*(Cb 128)
 - Because there is similar structure for the color space conversion formulas, the color space conversion can adopt a unified formula.
 - dout0 = A0*din0 + B0*din1 + C0*din2 + S0
 - dout1 = A1*din0 + B1*din1 + C1*din2 + S1
 - dout2 = A2*din0 + B2*din1 + C2*din2 + S2
- Among them, A0, B0, C0, A1, B1, C1, A2, B2, C2 are multiplication coefficient; S0 and S1, S2 are constant augend; din0, din1, din2 are channels input; dout0, dout1, dout2 are the outputs of the channels.
 - Table 3-1 is a table of predefined standard color space conversion formula coefficients.

Table 3-1 Standard Conversion Formula Coefficients

Color Model	_	A	В	С	S
	0	0.299	0.587	0.114	0.000
SDTV Studio RGB to YCbCr	1	-0.172	-0.339	0.511	128.000
	2	0.511	-0.428	-0.083	128.000
	0	0.257	0.504	0.098	16.000
SDTV Computer RGB to YCbCr	1	-0.148	-0.291	0.439	128.000
OBT. Compater Hab to Tobol					

I				1	
	2	0.439	-0.368	-0.071	128.000
	0	1.000	0.000	1.371	-175.488
SDTV YCbCr to Studio RGB	1	1.000	-0.336	-0.698	132.352
	2	1.000	1.732	0.000	-221.696
	0	1.164	0.000	1.596	-222.912
SDTV YCbCr to Computer RGB	1	1.164	-0.391	-0.813	135.488
·	2	1.164	2.018	0.000	-276.928
	0	0.213	0.715	0.072	0.000
HDTV Studio RGB to YCbCr	1	-0.117	-0.394	0.511	128.000
	2	0.511	-0.464	-0.047	128.000
	0	0.183	0.614	0.062	16.000
HDTV Computer RGB to YCbCr	1	-0.101	-0.338	0.439	128.000
·	2	0.439	-0.399	-0.040	128.000
	0	1.000	0.000	1.540	-197.120
HDTV YCbCr to Studio RGB	1	1.000	-0.183	-0.459	82.176
	2	1.000	1.816	0.000	-232.448
	0	1.164	0.000	1.793	-248.128
HDTV YCbCr to Computer RGB	1	1.164	-0.213	-0.534	76.992
·	2	1.164	2.115	0.000	-289.344
	0	0.299	0.587	0.114	0.000
Computer RGB to YUV	1	-0.147	-0.289	0.436	0.000
	2	0.615	-0.515	-0.100	0.000
YUV to Computer RGB	0	1.000	0.000	1.140	0.000
10 v to computer ricin	1	1.000	-0.395	-0.581	0.000

	2	1.000	-2.032	0.000	0.000
	0	0.299	0.587	0.114	0.000
Computer RGB to YIQ	1	0.596	-0.275	-0.321	0.000
	2	0.212	-0.523	0.311	0.000
	0	1.000	0.956	0.621	0.000
YIQ to Computer RGB	1	1.000	-0.272	-0.647	0.000
	2	1.000	-1.107	1.704	0.000

The specific process is as follows:

- 1. The input data is selected according to the input parameters. Since signed data operation is used, if it is unsigned data input, it needs to be converted into signed data format.
- 2. The multiplier is used to multiply the coefficients and the data. When the multiplier uses pipeline output, it is necessary to pay attention to the delay of data output.
- 3. Add the results of the multiplication operations.
- 4. Limit the data overflow and underflow.
- 5. Select the signed or unsigned output according to the parameters of the output data, and limit the output according to the range of the output data.

Port List

The I/O port of Gowin CSC IP is shown in Figure 3-2.

 I_rst_n
 O_doutvalid

 I_clk
 O_dout0[7:0]

 I_dinvalid
 O_dout1[7:0]

 I_din0[7:0]
 O_dout1[7:0]

 I_din1[7:0]
 O_dout2[7:0]

Figure 3-2 Schematic Diagram of CSC IP Port

The I/O ports of Gowin CSC IP are shown in Table 3-2.

No.	Signal Name	I/O	Description	Note
1	I_rst_n	I	Reset signal, active low	
2	I_clk	I	Working clock	
3	I_din0	I	Data input of channel 0	
			Take RGB format as an example: I_din0 = R	
			Take YCbCr format as an example: I_din0	
			= Y	
			Take YUV format as an example: I_din0 = Y	
			Take YIQ format as an example: I_din0 = Y	The I/O of all
4	I_din1	I	Data input of channel 1	the signals ta
			Take RGB format as an example: I_din1 = G	kes CSC IP
			Take YCbCr format as an example: I_din1	as reference
			= Cb	
			Take YUV format as an example: I_din1 = U	
			Take YIQ format as an example: I_din1 = I	
5	I_din2	I	Data input of channel 2	
			Take RGB format as an example: I_din2 = B	
			Take YCbCr format as an example: I_din2	
			= Cr	

			Take YUV format as an example: I_din2 = V	
			Take YIQ format as an example: I_din2 = Q	
6	I_dinvalid	1	Input data valid signal	
7	O_dout0	0	Data output of channel 0	
			Take RGB format as an example: O_dout0	
			= R	
			Take YCbCr format as an example:	
			O_dout0 = Y	

			Take YUV format as an example: O_dout0
			= Y
			Take YIQ format as an example: O_dout0 =
			Υ
8	O_dout1	0	Data output of channel 1
			Take RGB format as an example: O_dout1
			= G
			Take YCbCr format as an example:
			O_dout1 = Cb
			Take YUV format as an example: O_dout1
			= U
			Take YIQ format as an example:O_dout1 =
			V
9	O_dout2	0	Data output of channel 2
			Take RGB format as an example: O_dout2
			= B
			Take YCbCr format as an example:
			O_dout2 = Cr
			Take YUV format as an example: O_dout2
			= U
			Take YIQ format as an example:O_dout2 =
			V
10	O_doutvalid	0	Output data valid signal

Table 3-3 Global Parameter

No.	Name	Value Range	Default Value	Description
		SDTV Studio RGB to YCbC r, SDTV Computer RGB to YCbCr, SDTV		
1	Color_Model	YCbCr to Studio RGB, SDT V YCbCr to Computer RGB , HDTV Studio RGB to YCb Cr, HDTV Computer RGB t o YCbCr, HDTV YCbCr to S tudio RGB, HDTV YCbCr to Computer RGB, Computer RGB to YUV, YUV to Comp uter RGB, Computer RGB t o YIQ, YIQ to Computer	SDTV Studio RGB t o YCbCr	Color space conversion model; S pecify several predefined sets of coefficients and constant conversion formulas according to the BT601 and BT709 standard s; Custom: Customize the coefficien ts and constants of the conversion formula.

		RGB, Custom		
2	Coefficient Wi	11~18	11	Coefficient bit width; 1 bit for sign, 2 bits for integer, and the rest for f raction
3	DIN0 Data Ty pe	Signed, Unsigned	Unsigned	Input data type of Channel 0
4	DIN1 Data Ty pe	Signed, Unsigned	Unsigned	Input data type of Channel 1
5	DIN2 Data Ty pe	Signed, Unsigned	Unsigned	Input data type of Channel 2
6	Input Data Wi dth	8/10/12	8	Input data width
7	Dout0 Data Ty	Signed, Unsigned	Unsigned	Output data type of Channel 0
8	Dout1 Data Ty pe	Signed, Unsigned	Unsigned	Output data type of Channel 1
9	Dout2 Data Ty	Signed, Unsigned	Unsigned	Output data type of Channel 2
10	Output Data Width	8/10/12	8	Output data width
11	A0	-3.0~3.0	0.299	1st coefficient of Channel 0
12	В0	-3.0~3.0	0.587	2nd coefficient of Channel 0
13	C0	-3.0~3.0	0.114	3rd coefficient of Channel 0
14	A1	-3.0~3.0	-0.172	1st coefficient of Channel 1

15	B1	-3.0~3.0	-0.339	2nd coefficient of Channel 1
16	C1	-3.0~3.0	0.511	3rd coefficient of Channel 1
17	A2	-3.0~3.0	0.511	1st coefficient of Channel 2
18	B2	-3.0~3.0	-0.428	2nd coefficient of Channel 2
19	C2	-3.0~3.0	-0.083	3rd coefficient of Channel 2
20	S0	-255.0~255.0	0.0	Constant of Channel 0
21	S1	-255.0~255.0	128.0	Constant of Channel 1
22	S2	-255.0~255.0	128.0	Constant of Channel 2
23	Dout0 Max Va lue	-255~255	255	The maximum of output data rang e of channel 0
24	Dout0 Min Val ue	-255~255	0	The minimum of output data rang e of Channel 0
25	Dout1 Max Va lue	-255~255	255	The maximum of output data rang e of channel 1
26	Dout1 Min Val ue	-255~255	0	The minimum of output data rang e of Channel 1
27	Dout2 Max Va lue	-255~255	255	The maximum of output data rang e of channel 2
28	Dout2 Min Val ue	-255~255	0	The minimum of output data rang e of Channel 2

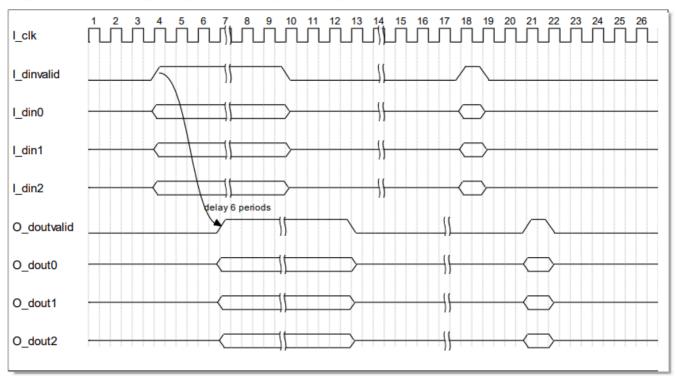
Timing Description

This section describes the timing of Gowin CSC IP.

The data is output after a delay of 6 clock cycles after the CSC operation. The duration of the output data depends on the input data and is the same as the duration of the input data.

Figure 3-3 Timing Diagram of Input/Output Data Interface

Figure 3-3 Timing Diagram of Input/Output Data Interface



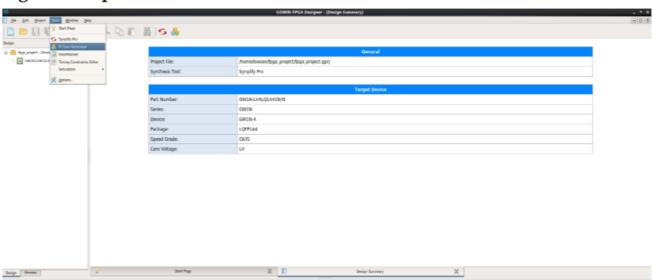
Interface Configuration

You can use IP core generator tools in the IDE to call and configure Gowin CSC IP.

1. Open IP Core Generator

After creating the project, you can click the "Tools" tab in the upper left, select and open the IP Core Generater from the drop-down list, as shown in Figure 4-1.

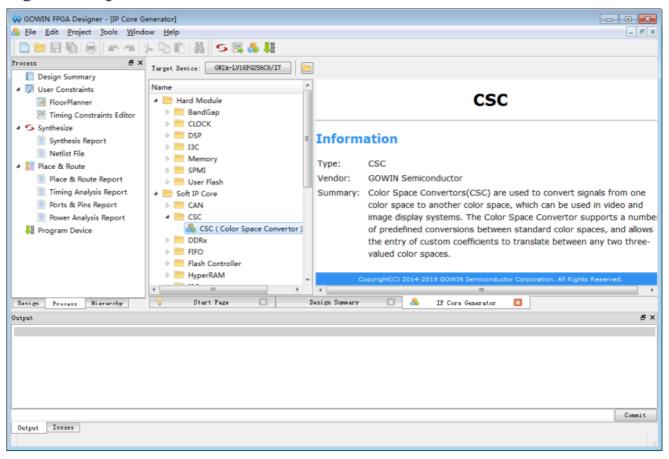
Figure 4-1 Open IP Core Generater



2. Open CSC IP core

Click "Multimedia" and double-click "Color Space Convertor" to open the configuration interface of CSC IP core, as shown in Figure 4-2.

Figure 4-2 Open CSC IP Core



3. CSC IP core ports

On the left of the configuration interface is the ports diagram of CSC IP core, as shown in Figure 4-3.

W IP Customization X Color Space Convertor General GW2A-18 Device Version: C Device: Part Number: GW2A-LV18PG484C8/I7 Language: Verilog File Name: color_space_convertor | Module Name: pr_Space_Convertor_Top proj\Gowin CSC RefDesign\project\src\color space convertor Create In: Data Options Color Model O dout0[7:0] Color Model Conversion: SDTV Studio RGB to YCbCr Din and dout refer to the input and output channels respectively: dout0 = A0*din0 + B0*din1 + C0*din2 + S0 O_dout1[7:0] dout1 = A1*din0 + B1*din1 + C1*din2 + S1 dout2 = A2*din0 + B2*din1 + C2*din2 + S2 O dout2[7:0] Coefficient Setting Coefficient Width: 11 A0: 0.299 \$\display \text{B0:} 0.587 \$\display \text{C0:} 0.114 \$\display \text{S0:} 0.000 A1: -0.172 \$\dip \text{B1:} -0.339 \$\dip \text{C1:} 0.511 \$\dip \text{S1:} 128.000 \$\dip\$ A2: 0.511 \$\displays B2: -0.428 \$\displays C2: -0.083 \$\displays S2: 128.000 \$\displays **Q**

Figure 4-3 CSC IP Core Interface Diagram

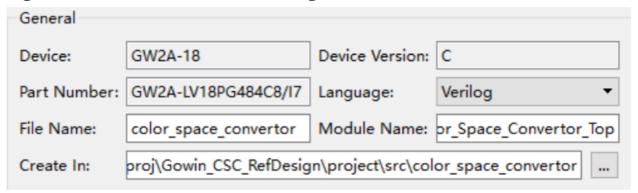
4. Configure the general information

• See the general information in the upper part of configuration interface, as shown in Figure 4-4. Take GW2A-18 chip as an example, and select PBGA256 package. The top-level file name of the generated

project is shown in the "Module Name", and the default is "

• Color_Space_Convertor_Top", which can be modified by users. The file generated by the IP core is shown in "File Name", which contains the files required by CSC IP core, and the default is "color_space_convertor", which can be modified by users. The "Creat IN" shows the path of IP core files, and the default is "\project path\src\ color_space_convertor", which can be modified by users.

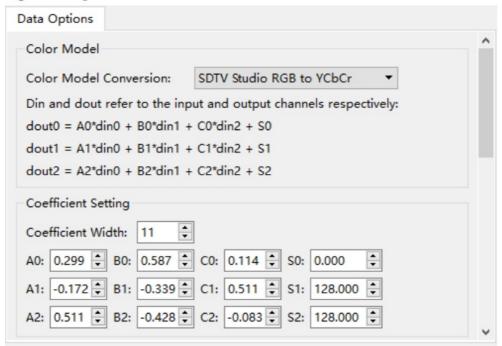
Figure 4-4 General Information Configuration Interface



5. Data Options

In the "Data Options" tab, you need to configure the formula, data type, data bit width and other parameter information for the CSC operations, as shown in Figure 4-5.

Figure 4-5 Options Tab



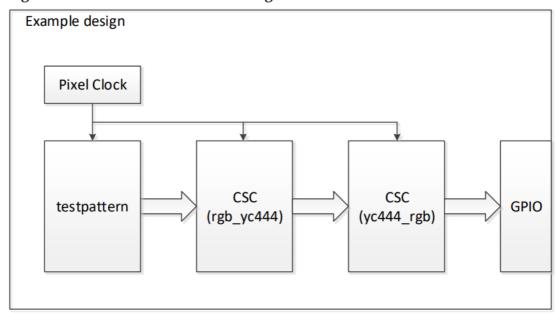
Reference Design

This chapter focuses on the usage and constructure of the reference design instance of CSC IP. Please see the CSC Reference Design for details at Gowinsemi website.

Design Instance Application

• Take DK-VIDEO-GW2A18-PG484 as an example, the structure is as shown in Figure 5-1. For the DK-VIDEO-GW2A18-PG484 development board information, you can click here.

Figure 5-1 Structure of Reference Design



- In the reference design, video_top is the top-level module, whose workflow is shown below.
 - 1. The test pattern module is used to generate the test pattern with a resolution of 1280×720 and data format of RGB888.
 - 2. Call CSC IP core generator to generatergb_yc_top module to achieve RGB888 to YC444.
 - 3. Call CSC IP core generator to generate yc_rgb_top module to achieve YC444 to RGB88.
 - 4. After the two conversions, the RGB data can be compared to see whether they are correct.
 When the reference design is applied to the board-level test, you can convert the output data through the video encoding chip and then output to the display.

In the simulation project provided by the reference design, BMP is used as the test excitation source, and tb_top is the top-level module of the simulation project. Comparison can be made by the output image after simulation.

File Delivery

The delivery file for Gowin CSC IP includes document, design source code and reference design.

Document

The document mainly contains PDF file of the user guide.

Table 6-1 Documents List

Name	Description
IPUG902, Gowin CSC IP User Guide	Gowin CSC IP user guide, namely this one.

Design Source Code (Encryption)

The encrypted code file contains the Gowin CSC IP RTL encrypted code which is used for GUI in order to cooperate with Gowin YunYuan software to generate the IP core required by users.

Table 6-2 Design Source Code List

Name	Description
color_space_convertor.v	The top-level file of the IP core, which provides users with interface informati on, encrypted.

Reference Design

The Ref. Design file contains the netlist file for Gowin CSC IP, user reference design, constraints file, top-level file and the project file, etc.

Table 6-3 Ref.Design File List

Name	Description
video_top.v	The top module of reference design
testpattern.v	Test pattern generation module
csc_ref_design.cst	Project physical constraints file
csc_ref_design.sdc	Project timing constraints file
color_space_convertor	CSC IP project folder
rgb_yc_top.v	Generate the first CSC IP top-level file, encrypted
rgb_yc_top.vo	Generate the first CSC IP netlist file
yc_rgb_top.v	Generate the second CSC IP top-level file, encrypted

—yc_rgb_top.vo	Generate the second CSC IP netlist file
gowin_rpll	PLL IP project folder
key_debounceN.v	Key debouncing module
i2c_master	I2C Master IP project folder
adv7513_iic_init.v	ADV7513 chip initialization module

Documents / Resources

GO₩IN	
Gover CSC IP User Guide **CONTRACTORS** **CONTRACTORS**	GOWIN IPUG902E CSC IP Programming For The Future [pdf] User Guide IPUG902E CSC IP Programming For The Future, IPUG902E, CSC IP Programming For The Future, Programming For The Future, The Future

References

• Ocdn.gowinsemi.com.cn/CSC_RefDesign.rar

- * Home GOWIN Semiconductor
- **One moment, please...**
- **One moment, please...**
- * IP and Reference Design | Gowin
- User Manual

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