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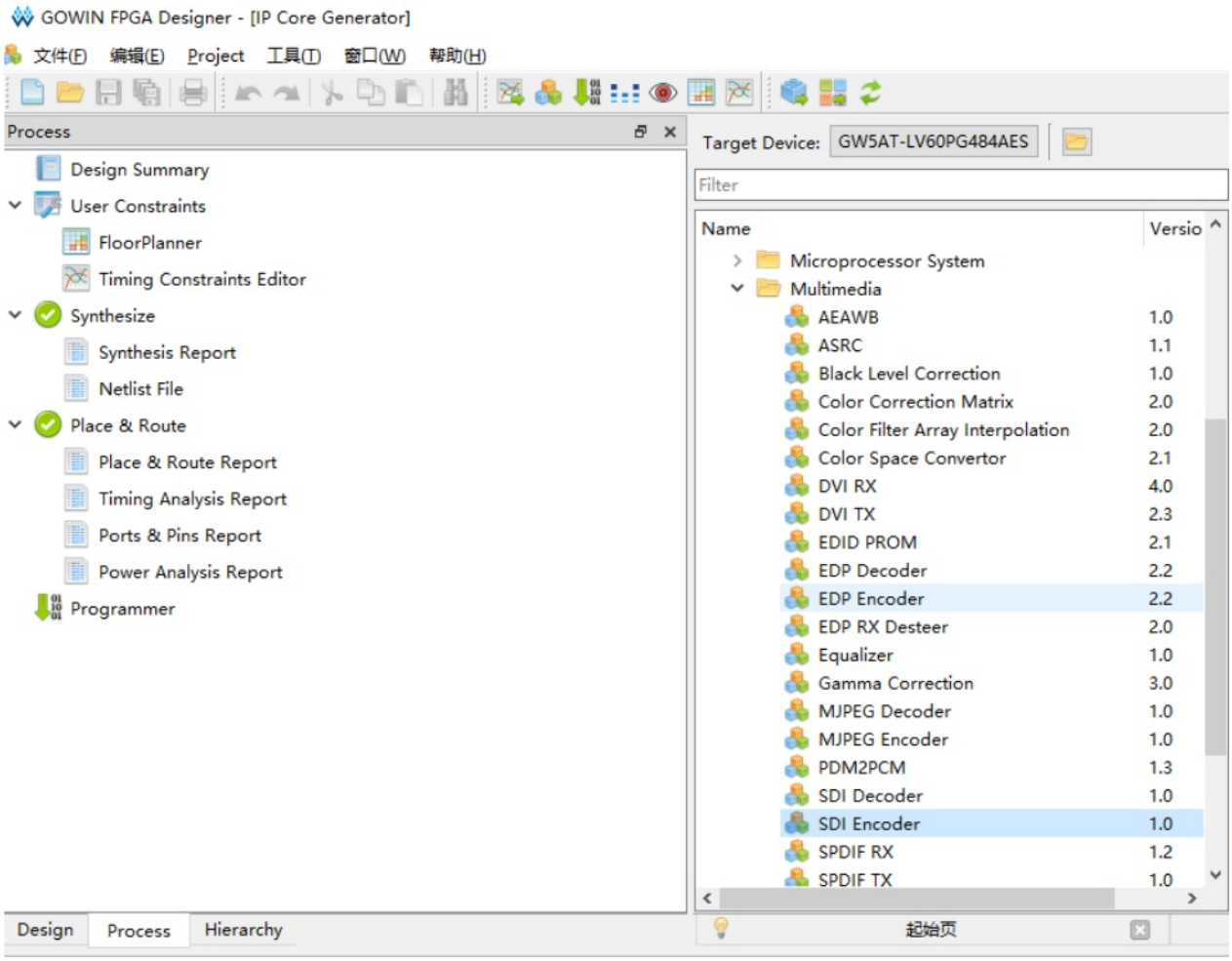
GOWIN IPUG1205 SDI Encoder IP



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Revision History

Date	Version	Description
04/11/2025	1.0E	Initial version published.

About This Guide

Purpose

The purpose of Gowin SDI Encoder IP is to help you learn the features and usage of Gowin SDI Encoder IP by providing the descriptions of features, functions, ports, timing, GUI and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.11 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- DS981, GW5AT series of FPGA Products Data Sheet
- DS1239, GW5AST series of FPGA Products Data Sheet
- SUG100, Gowin Software User Guide

Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning

DE	Data Enable
FPGA	Field Programmable Gate Array
HS	Horizontal Sync
IP	Intellectual Property
SDI	Serial Digital Interface
SerDes	Serializer/Deserializer
SMPTE	Society of Motion Picture and Television Engineers
VESA	Video Electronics Standards Association
VS	Vertical Sync

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com E-mail: support@gowinsemi.com

Overview

The Serial Digital Interface (SDI) is a member of the digital video interface family and is used for transmitting digital video signals. Gowin SDI Encoder IP can be operated under HD or 3G rate standards defined by the Society of Motion Picture and Television Engineers (SMPTE), converting video signals into SDI signals.

Table 2-1 Gowin SDI Encoder IP

Gowin SDI Encoder IP

Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.11 and above)

Note!

For the devices supported, you can click here to get the information.

Features

- Operates with 1 lane
- Supports link rates of 1.485/2.97 Gbps per lane
- Supports HD-SDI and 3G-SDI

Resource Utilization

Gowin SDI Encoder IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AST series of FPGA as an instance, the resource utilization of Gowin SDI Encoder IP is as shown in Table 2-2.

Table 2-2 Gowin SDI Encoder IP Resource Utilization

Device	GW5AST-60
Register	629

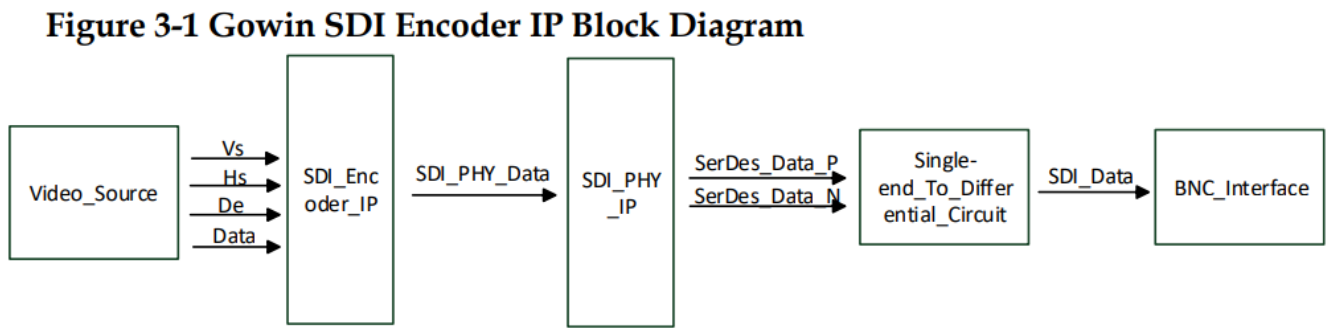
LUT	1015

Functional Description

System Block Diagram

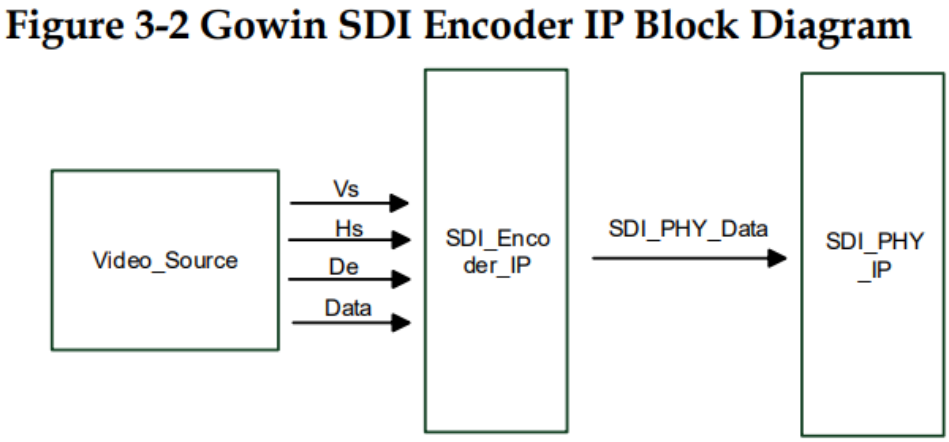
Gowin SDI Encoder IP can convert video signals into SDI signals. The SDI signal is then connected into the SDI PHY IP. The block diagram of Gowin SDI Encoder IP is as shown in Figure 3-1.

Figure 3-1 Gowin SDI Encoder IP Block Diagram



Function Modules

Figure 3-2 Gowin SDI Encoder IP Block Diagram



As shown in the diagram above, Gowin SDI Encoder IP can convert video data into SDI data.

Supported Format

Table 3-1 shows the formats supported by Gowin SDI Encoder IP.

Table 3-1 Formats Supported by Gowin SDI Encoder IP

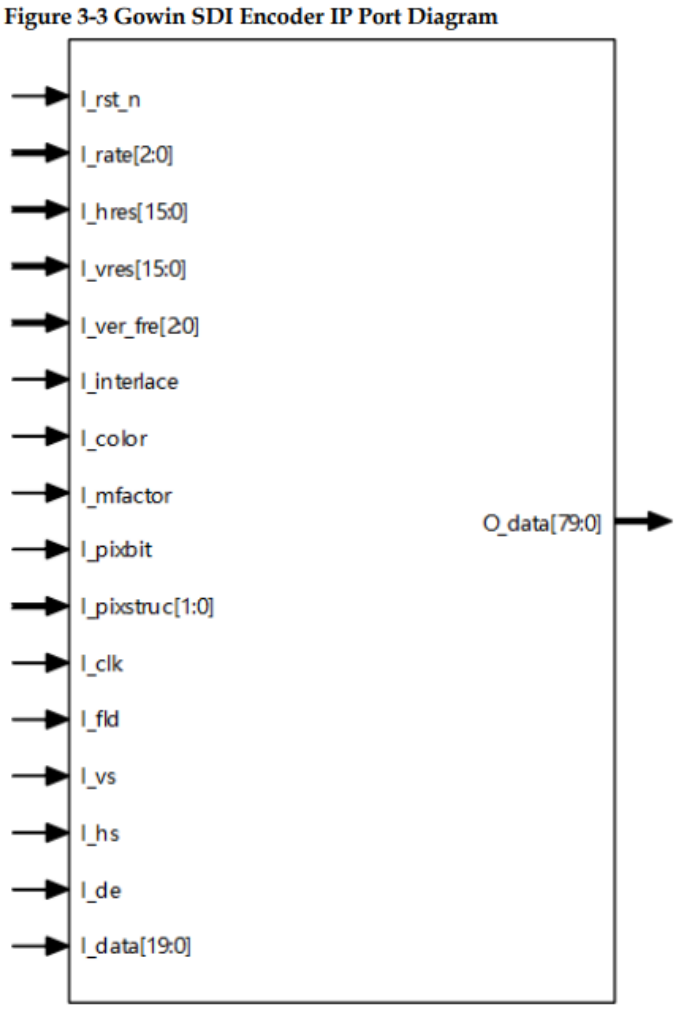
Standard	HD-SDI					3G-SDI	
Hor Addr Pixel	1280	1280	1920	1920	1920	1920	1920
Ver Addr Line	720	720	1080	1080	1080	1080	1080
Hor Total Pixel	1650	1980	2200	2640	2750	2200	2640

Standard	HD-SDI					3G-SDI	
Ver Total Line	750	750	1125	1125	1125	1125	1125
Scan Mode	Progressive	Progressive	Progressive	Progressive	Progressive	Progressive	Progressive
Frame Rate	60	50	30	25	24	60	50
Bit Per Word	20	20	20	20	20	20	20
Word Rate (Mhz)	74.25	74.25	74.25	74.25	74.25	148.5	148.5
Pixel Sample Rate (Mhz)	74.25	74.25	74.25	74.25	74.25	148.5	148.5
Structure	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2
Pixel Depth	10	10	10	10	10	10	10

Port List

The IO port of Gowin SDI Encoder IP is shown in Figure 3-3.

Figure 3-3 Gowin SDI Encoder IP Port Diagram



The IO ports vary slightly depending on the parameters.

The details of IO port of Gowin SDI Encoder IP are shown in Table 3-2.

Table 3-2 I/O List of Gowin SDI Encoder IP

Signal Name	I/O	Data Width	Description
I_rst_n	I	1	Reset signal, active-low

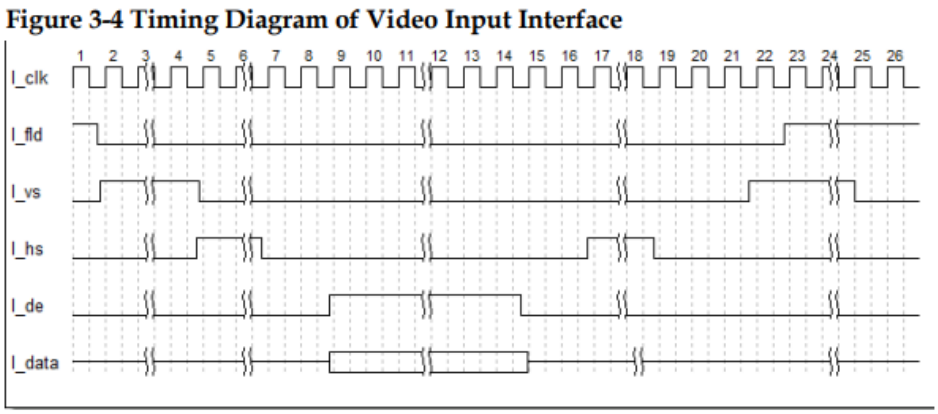
I_rate	I	3	Rate input: 0: Reserved 1: HD-SDI 2: 3G-SDI
I_hres	I	16	Horizontal resolution input
I_vres	I	16	Vertical resolution input
I_ver_fre	I	3	Vertical frequency input: 0: 60Hz 1: 50Hz 2: 30Hz 3: 25Hz 4: 24Hz
I_interlace	I	1	Interlace input: 0: Reserved 1: Progressive scan P
I_color	I	1	Color input: 0: YC 1: Reserved
I_mfactor	I	1	N factor input: 0: M = 1 1: Reserved
I_pixbit	I	1	Pixel bit input: 0: 10bit 1: Reserved

I_pixstruc	I	2	Pixel structure input: 2'b00: 4:2:2 2'b01: Reserved 2'b10: Reserved 2'b11: Reserved
I_clk	I	1	Input clock
I_fld	I	1	Field input (odd/even)
I_vs	I	1	vs input (positive polarity)
I_hs	I	1	hs input (positive polarity)
I_de	I	1	de input
I_data	I	20	Data input
O_data	O	80	The encoded data, connected to the SDI PHY IP.

Timing Description

The input interface timing diagram of Gowin SDI Encoder IP is as shown in Figure 3-4. For standard video, simply input the signals, and Gowin SDI Encoder IP will encode them. The encoded data is then output to the SDI PHY IP.

Figure 3-4 Timing Diagram of Video Input Interface



Interface Configuration

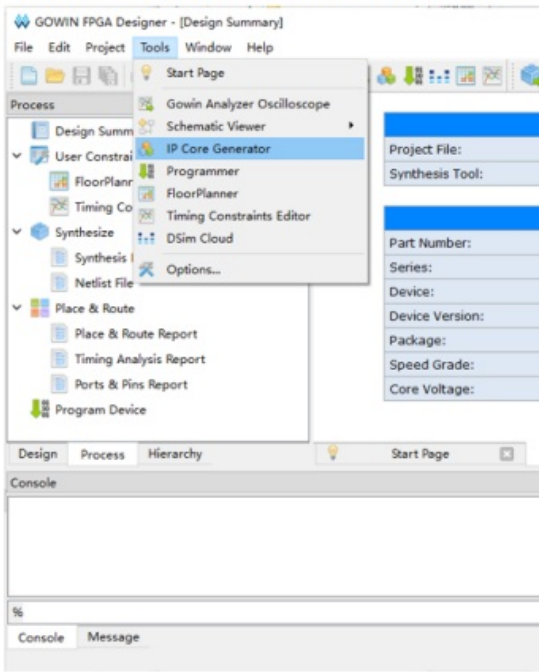
You can use IP core generator tool in Gowin Software to call and configure Gowin SDI Encoder IP.

Open IP Core Generator

After creating the project, click the “Tools” tab in the upper left, click “IP Core Generator” from the drop-down list to open Gowin IP Core Generator, as shown in Figure 4-1.

Figure 4-1 Open IP Core Generator

Figure 4-1 Open IP Core Generator

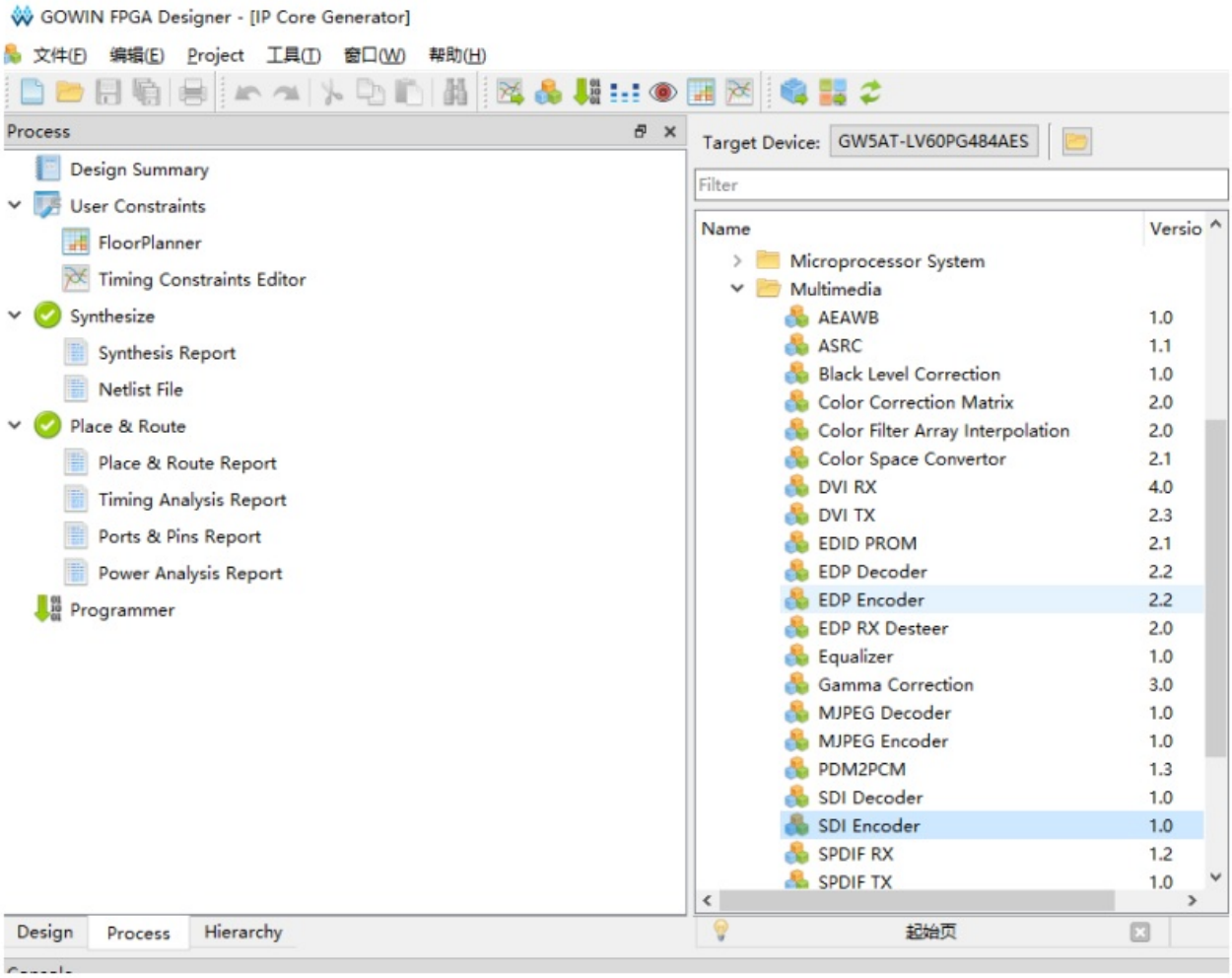


Select SDI Encoder IP.

Double Click “Multimedia” and select SDI Encoder to open SDI Encoder IP configuration interface, as shown in Figure 4-2.

Figure 4-2 Select SDI Encoder IP

Figure 4-2 Select SDI Encoder IP



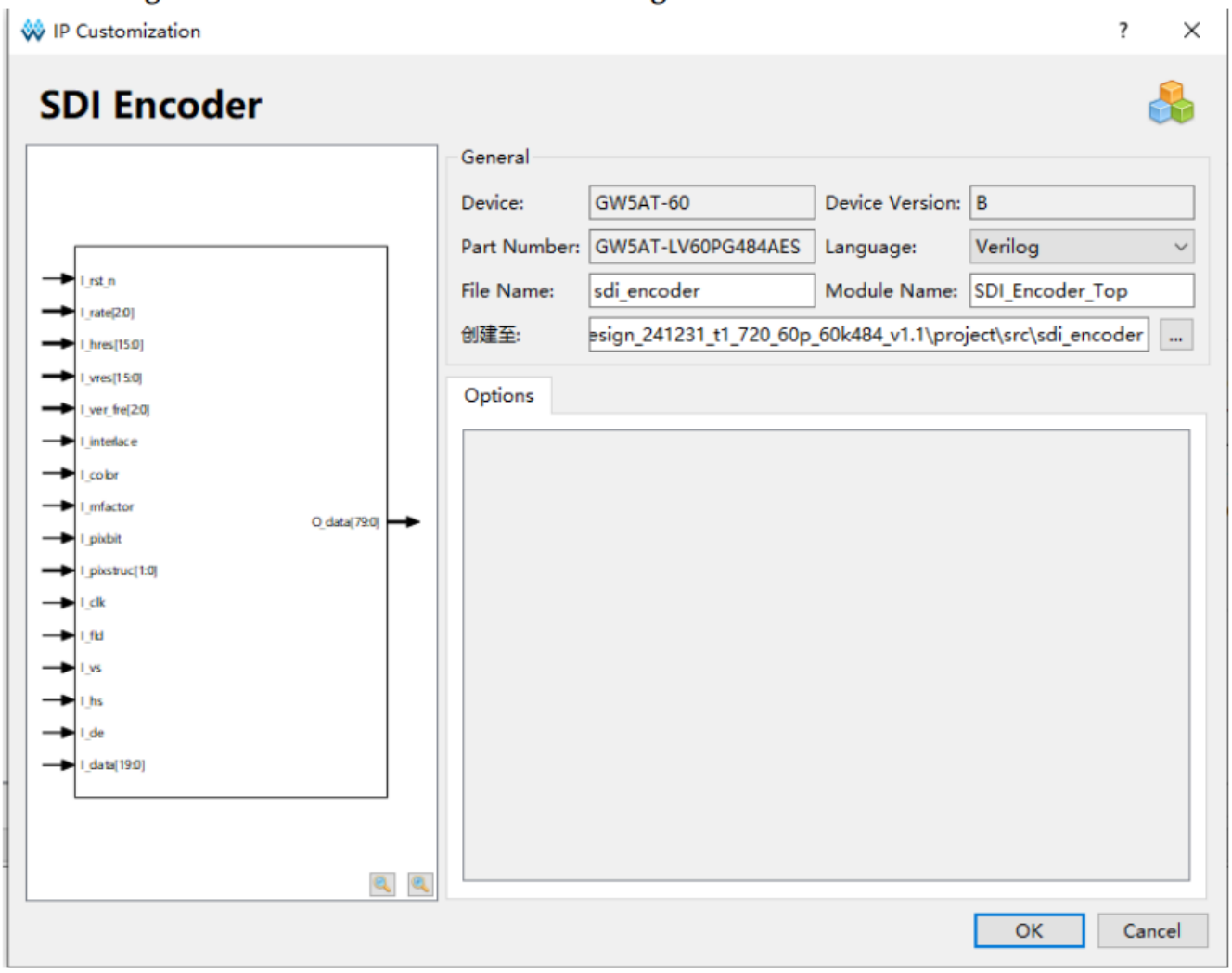
Gowin SDI Encoder IP Configuration Interface

First configure “General” tab in the SDI Encoder IP interface as shown in Figure 4-3.

- Device, Device Version, Part Number: Part number settings, determined by the current project, and the user can not set it.
- Language: Supports Verilog and VHDL; choose the language as requirements, and the default is Verilog.
- File Name, Module Name, Create In: Displays SDI file name, module name and the generated file path.

Figure 4-3 Gowin SDI Encoder IP Configuration Interface

Figure 4-3 Gowin SDI Encoder IP Configuration Interface



Click “OK” directly to generate the IP.

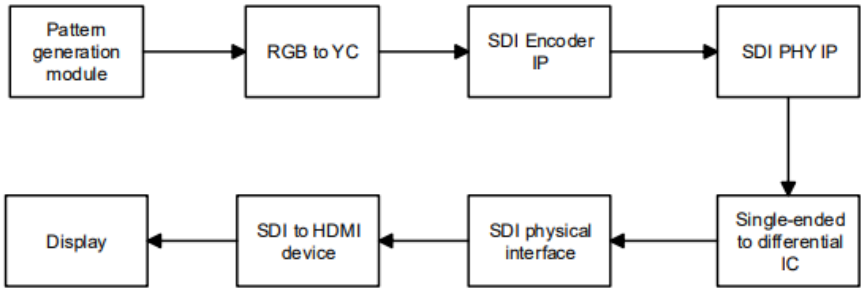
Reference Design

This chapter is intended to introduce the usage and structure of the reference design of Gowin SDI Encoder IP. Please see the SDI PHY IP Reference Design for details at Gowinsemi website.

This reference design takes DK_START_GW5AT-LV60PG484A_V1.1 development board as an example. For more information about DK_START_GW5AT-LV60PG484A_V1.1 development board, please refer to Gowinsemi website. The block diagram of reference design is shown in Figure 5-1.

Figure 5-1 Block Diagram of Reference Design

Figure 5-1 Block Diagram of Reference Design



File Delivery

The file delivery for Gowin SDI Encoder IP includes the documentation, the design source code, and the reference design.

Documentation

Table 6-1 Document List

Name	Description
IPUG1025 Gowin SDI Encoder IP User Guide	Gowin SDI Encoder IP User Guide, i.e., this manual.

Design Source Code (Encryption)

The encrypted code folder contains encrypted RTL code for Gowin SDI Encoder IP. This code is intended for use with GUI to generate the IP core as needed.

Table 6-2 File List of Gowin SDI Encoder IP

Name	Description
sdi_encoder.v	SDI Decoder IP File, encrypted.

Reference Design

The RefDesign folder contains the netlist files, user reference designs, constraints files, top-level files, and project files for Gowin SDI PHY IP, Gowin SDI Encoder IP, and Gowin

SDI Decoder IP.

Table 6-2 Gowin SDI Encoder IP RefDesign Folder Content List

Name	Description
video_top.v	The top module of reference design
testpattern.v	Test pattern generation module
dk_video.cst	Project physical constraints file
dk_video.sdc	Project timing constraints file
key_debounceN.v	Key debouncing
adv7513_iic_init.v	adv7513 configuration file
yc_to_rgb	yc_to_rgb folder
rgb_to_yc	rgb_to_yc folder
i2c_master	I2c_master folder, encrypted.

Documents / Resources

	GOWIN IPUG1205 SDI Encoder IP [pdf] User Guide IPUG1205-1.0E, IPUG1205 SDI Encoder IP, SDI Encoder IP, Encoder IP

References

- User Manual

Encoder IP, GOWIN, IPUG1205 SDI Encoder IP, IPUG1205-1.0E, SDI Encoder IP

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