



GOWIN IPUG1195-1.0E MII IP Host Controller User Guide

[Home](#) » [GOWIN](#) » **GOWIN IPUG1195-1.0E MII IP Host Controller User Guide**

Contents

- 1 GOWIN IPUG1195-1.0E MII IP Host Controller
- 2 Disclaimer
- 3 Revision History
- 4 1. About This Guide
 - 4.1 1.1 Purpose
 - 4.2 1.2 Related Documents
 - 4.3 1.3 Terminology and Abbreviations
 - 4.4 1.4 Support and Feedback
- 5 2. Overview
 - 5.1 2.1 Introduction
 - 5.2 2.2 Features
 - 5.3 2.3 Resource Utilization
- 6 3. Functional Description
 - 6.1 3.1 Structure
 - 6.2 3.2 Clocking
 - 6.3 3.3 Speed
 - 6.4 3.4 MII
 - 6.5 3.5 RMII
 - 6.6 3.6 Associated IP
- 7 4. Port Description
- 8 5. Call and Configure IP
- 9 6. Reference Design
 - 9.1 6.1 System Structure
 - 9.2 6.2 Operating Flow
- 10 7. File Delivery
 - 10.1 7.1 Document
 - 10.2 7.2 Design Source Code (Encryption)
 - 10.3 7.3 Reference Design
- 11 Specifications
- 12 FAQ
 - 12.1 Q: Can I modify the source code provided with the IP?
 - 12.2 Q: Is technical support available for using the Gowin MII to RMII IP?
- 13 Documents / Resources
 - 13.1 References
- 14 Related Posts

GOWIN IPUG1195-1.0E MII IP Host Controller



USER MANUAL

IPUG1195-1.0E, 2024-12-31

The Gowin MII to RMII IP is a specialized intellectual property designed by Gowin Semiconductor Corporation for data conversion purposes. It facilitates the conversion of Media Independent Interface (MII) signals to Reduced Media Independent Interface (RMII) signals.

Copyright © 2024 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

Gowin Semiconductor Corporation and are registered in China and/or other countries or regions. All other words and logos identified as trademarks or service marks are the property of their respective holders. No part of this document may be reproduced or transmitted in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
12/31/2024	1.0E	Initial version published.

1. About This Guide

1.1 Purpose

The purpose of Gowin MII to RMII IP User Guide is to help you to quickly understand the features and usage of Gowin MII to RMII IP by providing the descriptions of the functions, signal definition, parameters, and reference design. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.11. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- SUG100, Gowin Software User Guide
- DS100, GW1N series of FPGA Products Data Sheet
- DS117, GW1NR series of FPGA Products Data Sheet
- DS821, GW1NS series of FPGA Products Data Sheet
- DS861, GW1NSR series of FPGA Products Data Sheet
- DS841, GW1NZ series of FPGA Products Data Sheet
- DS961, GW2ANR series of FPGA Products Data Sheet
- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- DS971, GW2AN-18X & 9X Data Sheet
- DS976, GW2AN-55 Data Sheet
- DS981, GW5AT series of FPGA Products Data Sheet
- DS1103, GW5A series of FPGA Products Data Sheet

- DS1104, GW5AST series of FPGA Products Data Sheet
- DS1105, GW5AS series of FPGA Products Data Sheet
- DS1108, GW5AR series of FPGA Products Data Sheet
- DS1118, GW5ART series of FPGA Products Data Sheet

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
IP	Intellectual Property
LUT	Look-up Table
MII	Media Independent Interface
REG	Register
RMII	Reduced Media Independent Interface

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2. Overview

2.1 Introduction

Gowin MII to RMII IP implements the conversion between MII and RMII interfaces, providing a 16-signal MII interface and a 7-signal RMII interface. It supports both 10M and 100M data rates.

Table 2-1 Gowin MII to RMII IP Overview

Gowin MII to RMII IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encryption)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.11 and above)

Note!

For the devices supported, you can click here to get the information.

2.2 Features

- Supports MII and RMII interfaces
- Supports timing conversion between MII and RMII
- Supports both 10M and 100M data rates

2.3 Resource Utilization

Gowin MII to RMII IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices or at different densities, speeds, or grades. Taking Gowin GW5AST-138 device as an instance, the resource utilization is as shown in Table 2-2. For the resource utilization of other devices, please refer to later release information.

Table 2-2 Resource Utilization

Device	Programming Language	LUTs	REGs
GW5AST-138	Verilog	36	37

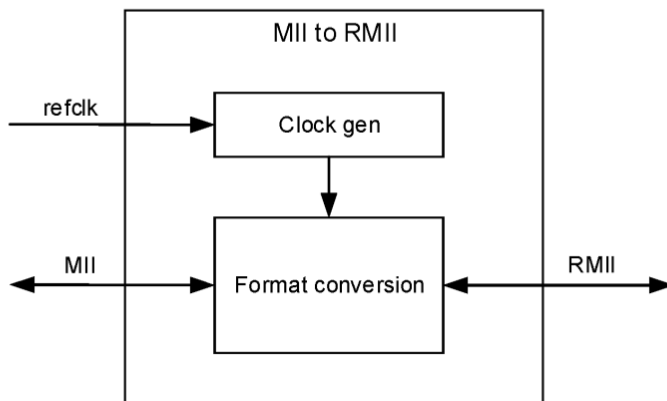
3. Functional Description

3.1 Structure

Gowin MII to RMII IP consists of Clock Gen and Format Conversion, as shown in Figure 3-1.

Figure 3-1.

Figure 3-1 Gowin MII to RMII IP Structure Diagram

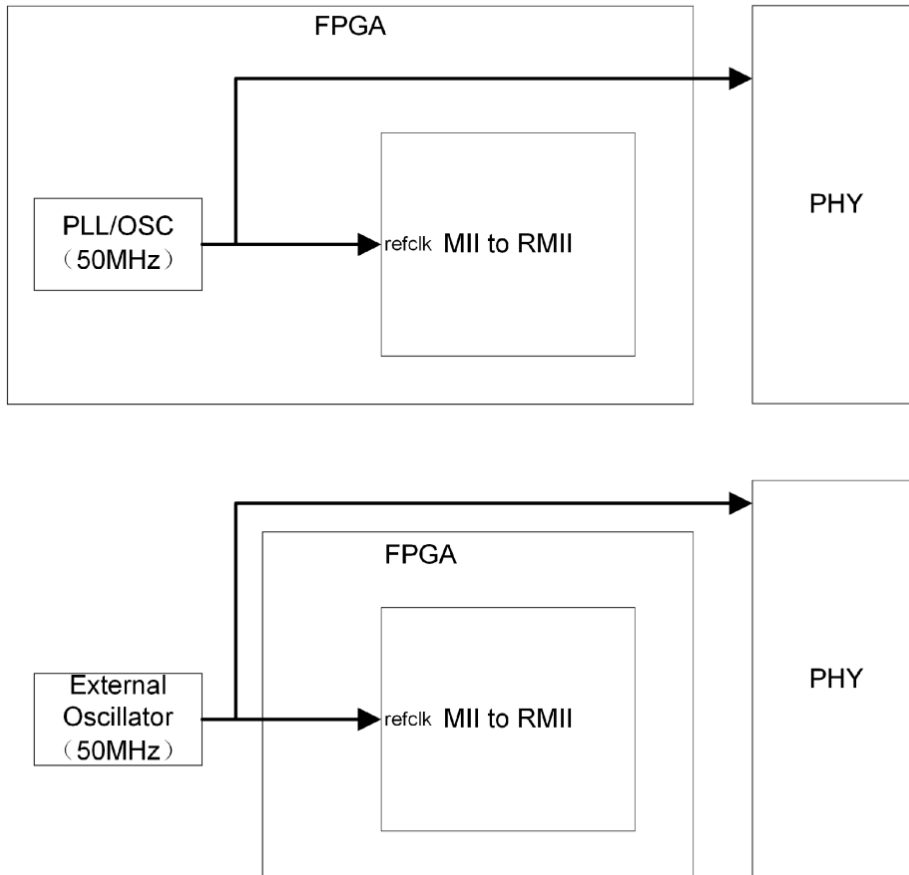


- **Clock gen:** Used to generate the clock signals required for MII.
- **Format Conversion:** Used to support timing conversion between MII and RMII.

3.2 Clocking

Gowin MII to RMII IP performs MII and RMII data conversion using a 50 MHz input clock. This 50 MHz clock can either be internally generated by the FPGA or externally provided by crystal. Note that a 50 MHz clock with the same source must be provided to both Gowin MII to RMII IP and the external PHY, as shown in Figure 3-2.

Figure 3-2 Clock Structure



3.3 Speed

Gowin MII to RMII IP supports both 10M and 100M rates, which can be selected via `speedis_100`; when `speedis_100` is set to 1, the IP is running at 100M, and when `speedis_100` is set to 0, the IP is running at 10M.

3.4 MII

The data transmission of the MII is driven by two clocks, `mii_rx_clk` and `mii_tx_clk`. All receive signals are synchronized with `mii_rx_clk`. All transmit signals are synchronized with `mii_tx_clk`.

The clocks `mii_rx_clk` and `mii_tx_clk` are derived by dividing the 50 MHz `refclk`. At 100M data rate, the frequency of `mii_rx_clk` and `mii_tx_clk` is 25 MHz; at the 10M data rate, the frequency is 2.5 MHz.

4 bits data is transmitted in one clock cycle, and when one byte of data needs to be transmitted, the data transmission sequence is as shown in Table 3-1.

Table 3-1 Byte Data Transmission Sequence in MII

Transmission Sequence	Byte Data
1st 4-bit data	[3:0]
2nd 4-bit data	[7:4]

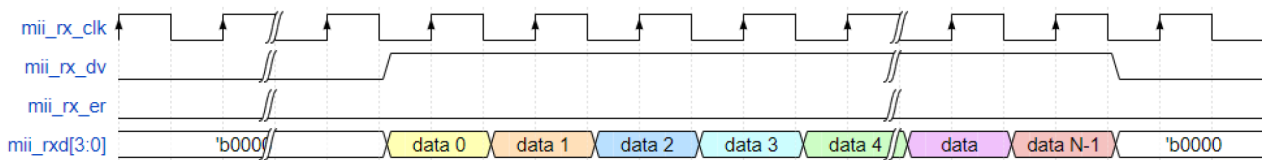
3.4.1 Data Reception

Normal Data Reception

Figure 3-3 shows the normal data reception via MII interface.

Throughout the entire data reception, `mii_rx_dv` remains 1 until the reception is complete, at which point it transitions to 0. Meanwhile, `mii_rx_er` also remains 0, and `mii_rxd` is the received data. `mii_rx_dv`, `mii_rx_er`, and `mii_rxd` perform state transitions on the falling edge of `mii_rx_clk`, providing reliable setup and hold times. It should be noted that there is no buffer in IP for the received data, so the user must always be ready to receive data continuously.

Figure 3-3 Normal Data Reception via MII Interface

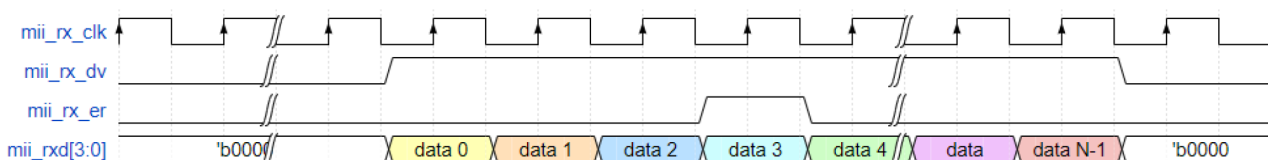


Error Data Reception

Figure 3-4 shows the error data reception via MII interface.

When `mii_rx_dv` is set to 1 and `mii_rx_er` is also 1, the data received on `mii_rxd` is error data.

Figure 3-4 Error Data Reception via MII Interface



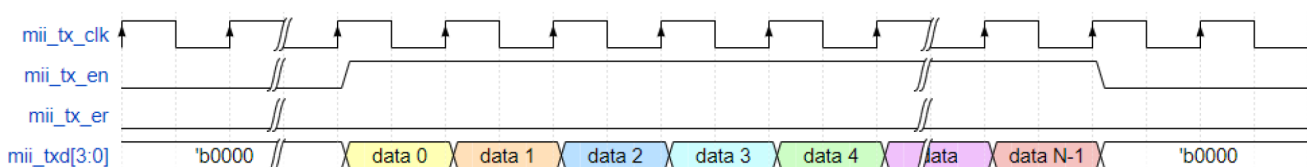
3.4.2 Data Transmitting

Normal Data Transmitting

Figure 3-5 shows the normal data transmitting via MII interface.

When there is data being transmitted, `mii_tx_en` is set to 1 and remains high until the transmission is complete, at which point it is set to 0. During the period when `mii_tx_en` is 1, `mii_tx_er` must remain 0, and valid data is output on `mii_txd`. `mii_tx_en`, `mii_tx_er` and `mii_txd` perform state transitions on the rising edge of `mii_tx_clk`.

Figure 3-5 Normal Data Transmitting via MII Interface



3.5 RMII

The data transmission of the RMII is driven by the clock `refclk`. All signals are synchronized with `refclk`, which runs at a frequency of 50 MHz.

During the data transmission, the number of clock cycles required to transmit 2-bit data varies depending on the rate. At 100M, each 2-bit data occupies 1 clock cycle for transmission; at 10M, each 2-bit data occupies 10 clock cycles for transmission.

When one byte of data needs to be transmitted, the data transmission sequence is as shown in Table 3-2.

Table 3-2 Byte Data Transmission Sequence in RMII

Transmission Sequence	Byte Data
1st 2-bit data	[1:0]
2nd 2-bit data	[3:2]
3rd 2-bit data	[5:4]
4th 2-bit data	[7:6]

3.5.1 Data Reception

Normal Data Reception

Figure 3-6 shows the normal data reception at 100M rate via RMII interface. Figure 3-7 shows the normal data reception at 10M rate via RMII interface.

Throughout the entire data reception, `rmii_rx_crs_dv` remains 1 until the reception is complete, at which point it transitions to 0. Meanwhile, `rmii_rx_er` also remains 0, and `rmii_rxd` is the received data. `rmii_rx_crs_dv`, `rmii_rx_er`, and `rmii_rxd` perform state transitions on the rising edge of `refclk`.

It should be noted that after `rmii_rx_crs_dv` is set to 1, `rmii_rxd` may contain zero or more clock cycles of idle data, represented as 2'b00.

Figure 3-6 Normal Data Reception at 100M Rate via RMII Interface

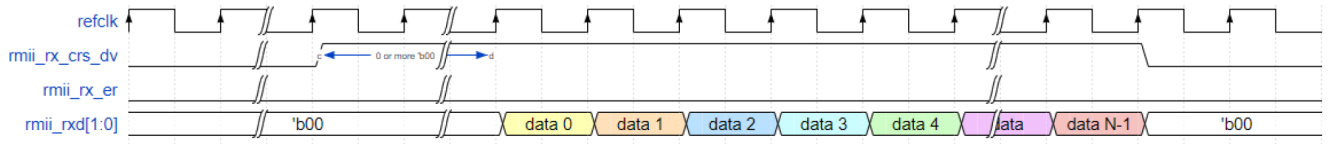
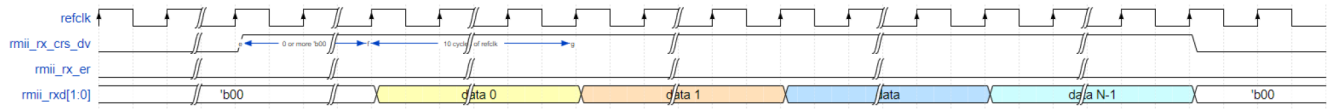


Figure 3-7 Normal Data Reception at 10M Rate via RMII Interface



Error Data Reception

Figure 3-8 shows the error data reception at 100M rate via RMII interface. Figure 3-9 shows the error data reception at 10M rate via RMII interface.

When `rmii_rx_crs_dv` is set to 1 and `rmii_rx_er` is also 1, the data received on `rmii_rxd` is error data.

Figure 3-8 Error Data Reception at 100M rate via RMII Interface

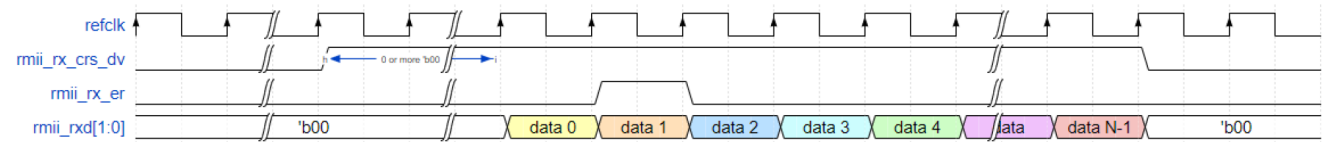
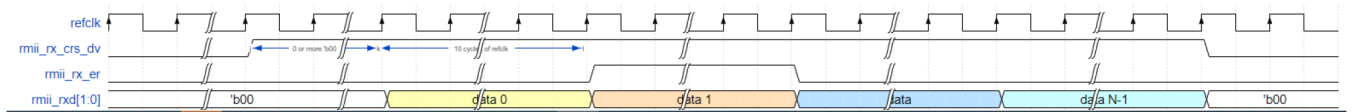


Figure 3-9 Error Data Reception at 10M rate via RMII Interface



3.5.2 Data Transmitting

Normal Transmitting

Figure 3-10 shows the normal data transmitting at 100M rate via RMII interface. Figure 3-11 shows the normal data transmitting at 10M rate via RMII interface.

When there is data being transmitted, `rmii_tx_en` is set to 1 and remains high until the transmission is complete, at which point it is set to 0. During the period when `rmii_tx_en` is 1, the data on `rmii_txd` is the valid data. `Rmii_tx_en` and `rmii_txd` perform state transitions on the rising edge of `refclk`.

Figure 3-10 Normal Data Transmitting at 100M rate via RMII Interface

Normal Transmitting

Figure 3-10 shows the normal data transmitting at 100M rate via RMII interface. Figure 3-11 shows the normal data transmitting at 10M rate via RMII interface.

When there is data being transmitted, rmii_tx_en is set to 1 and remains high until the transmission is complete, at which point it is set to 0. During the period when rmii_tx_en is 1, the data on rmii_txd is the valid data. Rmii_tx_en and rmii_txd perform state transitions on the rising edge of refclk.

Figure 3-10 Normal Data Transmitting at 100M rate via RMII Interface

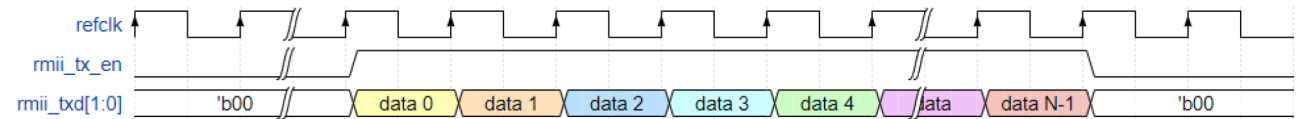
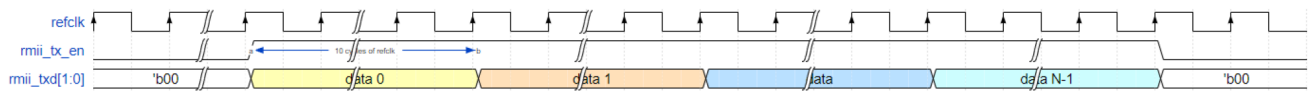


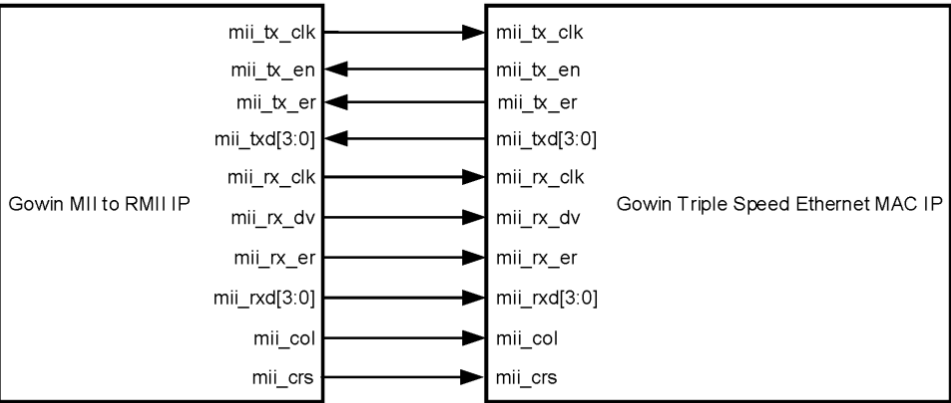
Figure 3-11 Normal Data Transmitting at 10M rate via RMII Interface



3.6 Associated IP

Gowin MII to RMII IP can be used together with Gowin Triple Speed Ethernet MAC IP to implement MAC function for RMII interface. They are connected through the MII interface, and the connection diagram is as shown in Figure 3-12.

Figure 3-12 Connected with Gowin Triple Speed Ethernet MAC IP



4. Port Description

The port diagram of Gowin MII to RMII IP is as shown in Figure 4-1.

Figure 4-1 Gowin MII to RMII IP Port Diagram

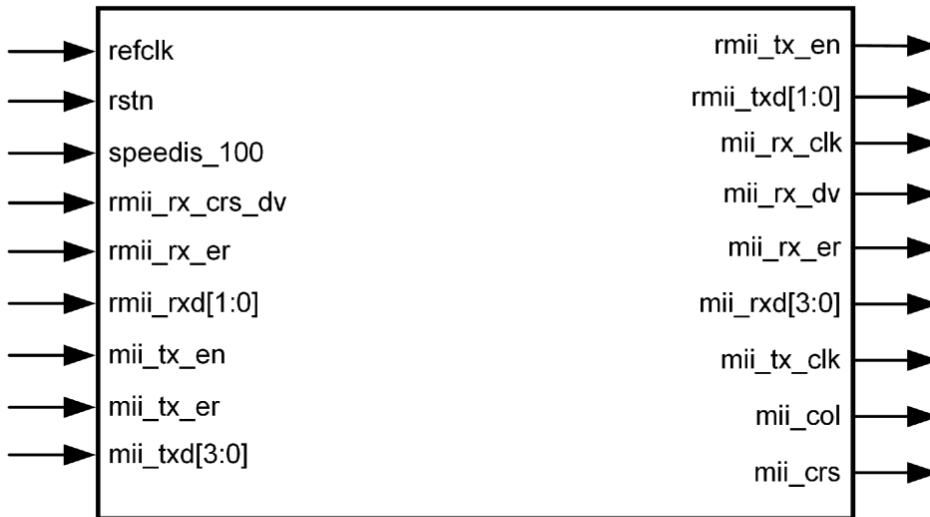


Table 4-1 Gowin MII to RMII Port List

No.	Signal Name	Type	Data Width	Description	Clock Domain
1	refclk	Input	1	IP clock input, 50 MHz	-
2	rstn	Input	1	IP reset signal, active-low	refclk
3	speedis_100	Input	1	Rate selection signal 1: 100M 0: 10M	

5. Call and Configure IP

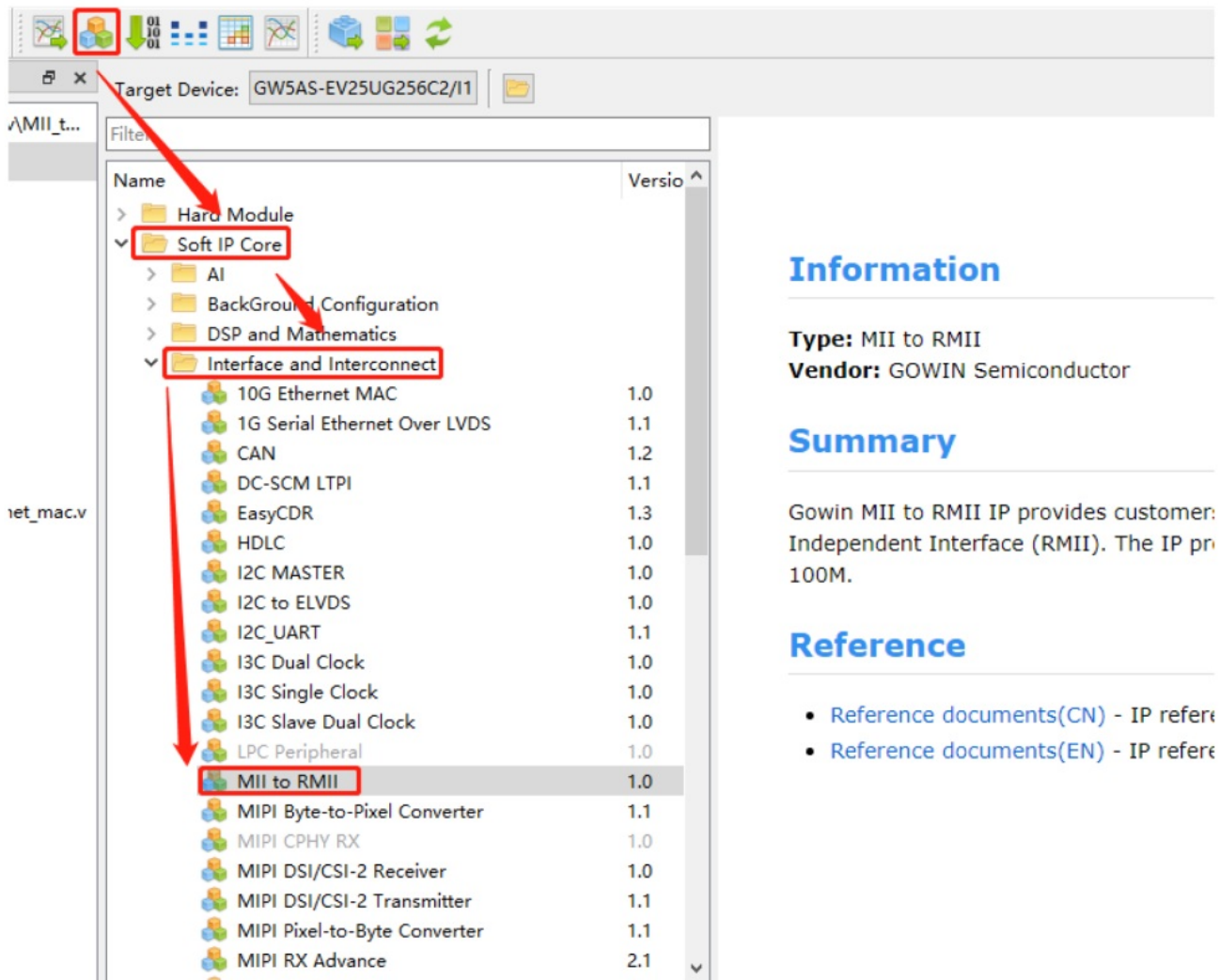


Click on the shortcut “ ” or “Tools > IP Core Generator” on the menu bar in Gowin Software to call and configure IP.

1. Open IP Core Generator.

After creating a new project, click “IP Core Generator” to open the IP Core Generator, as shown in Figure 5-1.

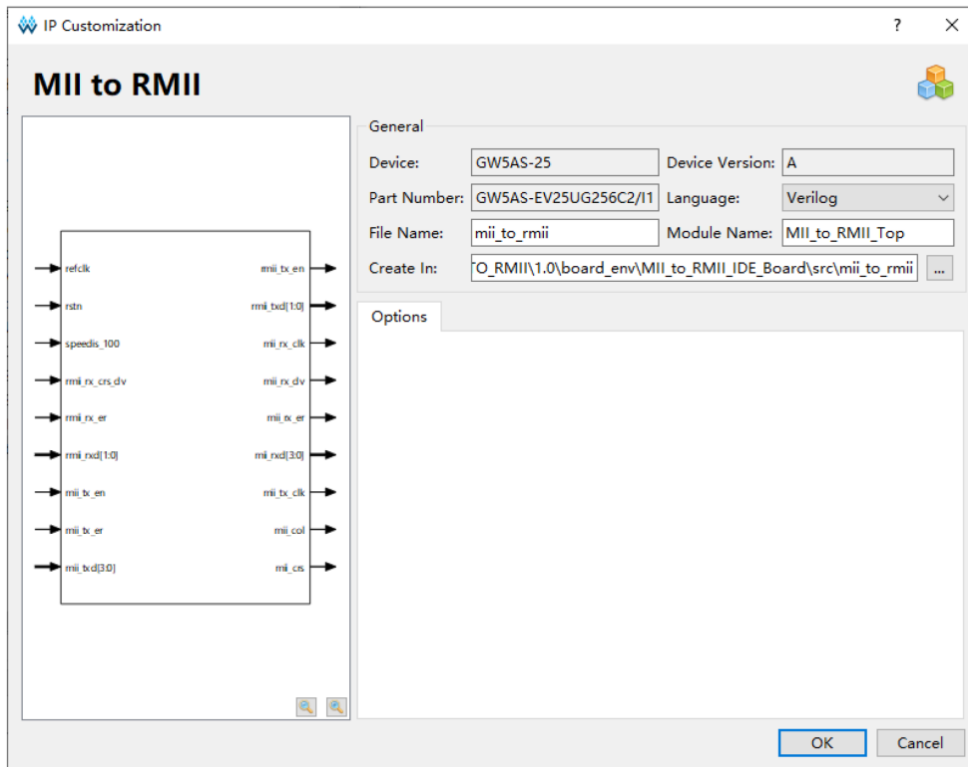
Figure 5-1 IP Core Generator Interface



2. Open the IP.

Double-click "Soft IP Core > Interface and Interconnect > MII to RMII", open Gowin MII to RMII IP Interface, as shown in Figure 5-2.

Figure 5-2 Gowin MII to RMII Configuration Interface



- You can configure the generated file name by modifying “File Name” text box.
- You can configure the top module name by modifying “Module Name” text box.
- You can configure other options by modifying “Options” tab.

6. Reference Design

For more information, please see Gowin MII to RMII IP reference designs at Gowin website.

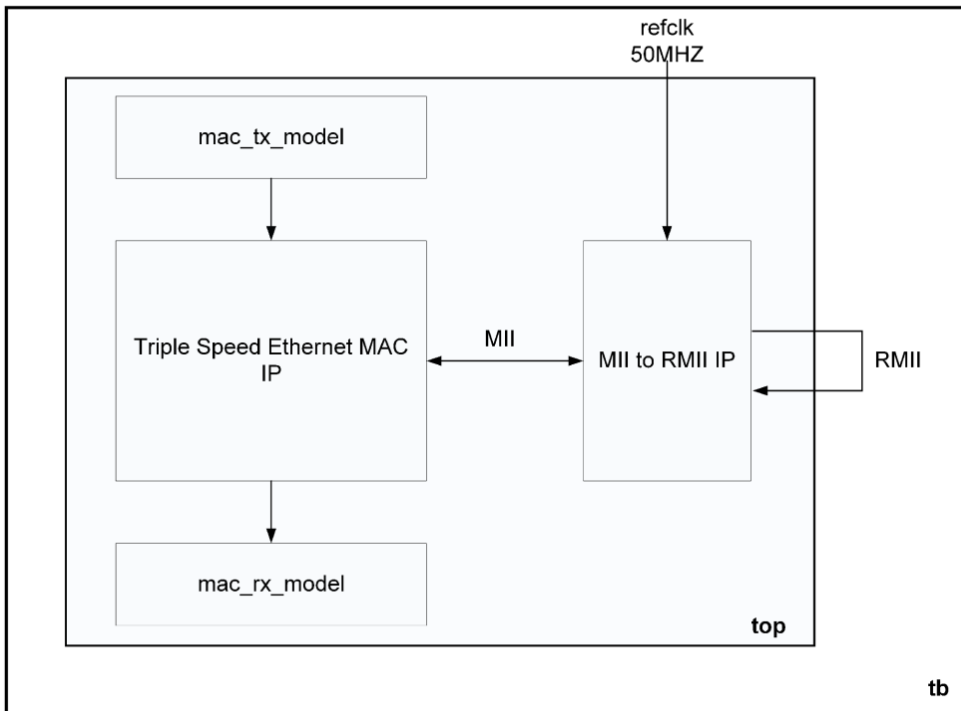
Note!

The provided reference design is solely for customers to perform functional simulation.

6.1 System Structure

The system structure of functional simulation is shown in Figure 6-1.

Figure 6-1 System Structure



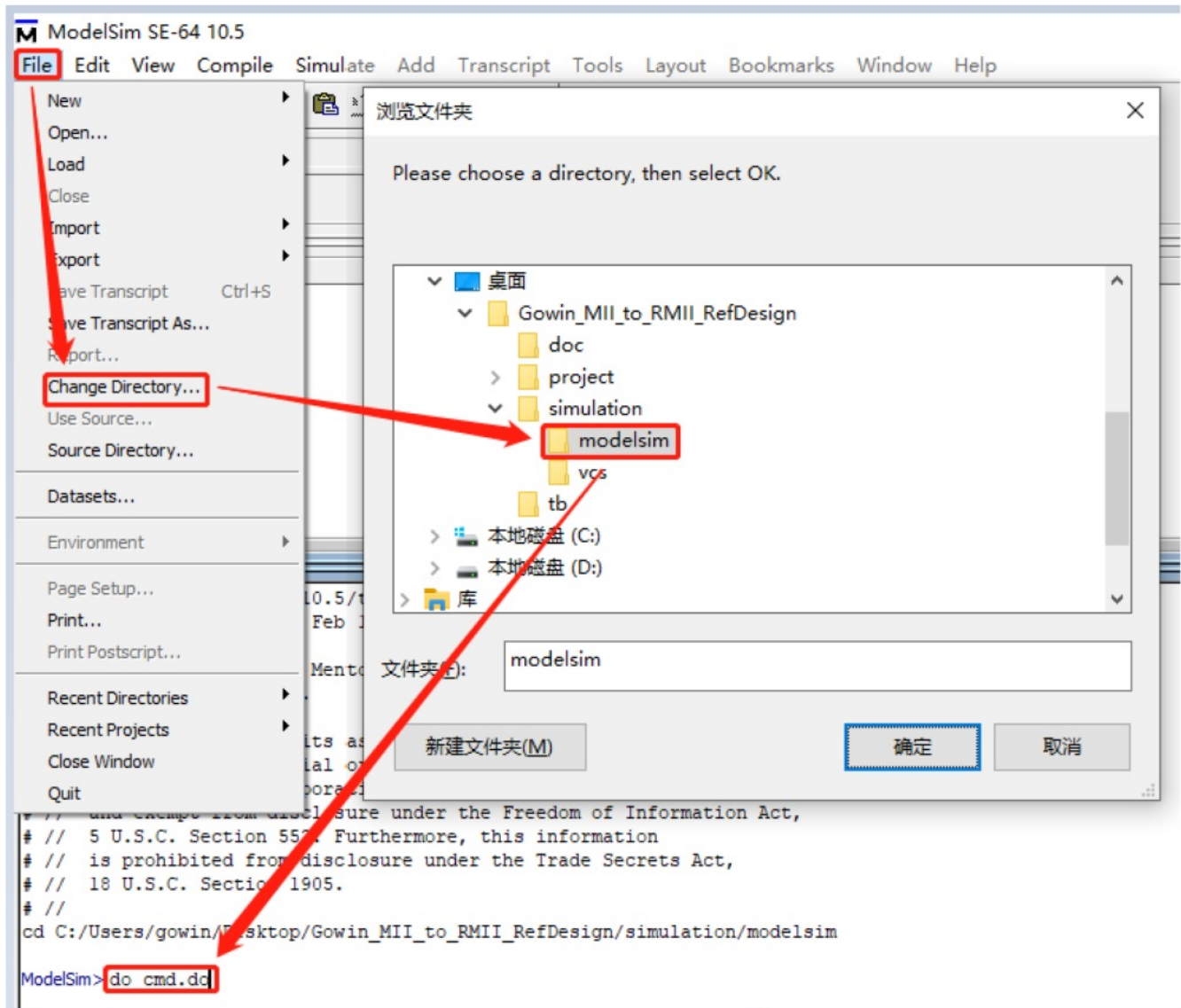
1. The top-level testbench provides a 50 MHz refclk, and the loopback for the RMII interface.
2. The top-level design includes the mac_tx_model, mac_rx_model, Triple Speed Ethernet MAC IP, and MII to RMII IP.
3. The mac_tx_model is used to send Ethernet frames, each containing 1500 bytes of data.
4. The mac_rx_model is used to receive Ethernet frames and check the accuracy of the Ethernet frames.

6.2 Operating Flow

6.2.1 Modelsim

1. Open ModelSim software, and click on "File" in the menu bar, then select "Change Directory" from the dropdown.
2. In the file explorer, navigate to the downloaded reference design folder Gowin_MII_to_RMII_RefDesign, and then select the "simulation" and "modelsim" folders.
3. In the ModelSim command window, enter the command "do cmd.do" and press Enter to start the functional simulation.

Figure 6-2 ModelSim Operating Flow Diagram



6.2.2 VCS

1. Open a terminal (command line) in the Linux environment where VCS is installed.
2. Use the cd command to navigate to the downloaded reference design folder Gowin_MII_to_RMII_RefDesign, and then sequentially enter the "simulation" and "vcs" folders.
3. Run the vcs.sh command and press Enter to start the functional simulation.

7. File Delivery

The delivery file of Gowin MII to RMII IP includes documentation and reference design.

7.1 Document

The folder contains the user guide in PDF version.

Table 7-1 Document List

Name	Description
IPUG1195, Gowin MII to RMII IP User Guide	Gowin MII to RMII IP User Guide

7.2 Design Source Code (Encryption)

The encryption code folder contains the RTL encryption code of Gowin MII to RMII IP, used for the GUI, and it is used with Gowin Software to generate the IP core as needed.

Table 7-2 Gowin MII to RMII IP Design Source Code List

Name	Description
mii_to_rmii_wrap.v	The top-level file of the IP core, which provides users with interface information, encrypted.
mii_to_rmii.v	IP core RTL design File, encrypted
static_macro_define.v	Local static parameter configuration file, not encrypted
define.vh	IP configuration file, generated from GUI

7.3 Reference Design

The Ref. Design folder contains the top file, and the project folder of Gowin MII to RMII IP

File Name	Description
top.v	The top module of reference design
mac_rx_model.v	MAC layer RX signal control module
mac_tx_model.v	MAC layer TX signal control module
triple_speed_ethernet_mac	Triple Speed Ethernet MAC IP folder
mii_to_rmii	II to RMII IP folder

Specifications

- Product Name: Gowin MII to RMII IP
- Model Number: IPUG1195-1.0E
- Trademark: Gowin Semiconductor Corporation
- Version: 1.0E
- Publication Date: 12/31/2024



FAQ

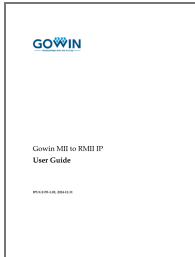
Q: Can I modify the source code provided with the IP?

A: The source code is provided for reference and integration purposes. Any modifications should be done carefully to ensure compatibility.

Q: Is technical support available for using the Gowin MII to RMII IP?

A: For technical support, please contact Gowin Semiconductor Corporation for assistance with any issues or inquiries regarding the IP usage.

Documents / Resources

	<p>GOWIN IPUG1195-1.0E MII IP Host Controller [pdf] User Guide</p> <p>IPUG1195-1.0E, IPUG1195-1.0E MII IP Host Controller, MII IP Host Controller, IP Host Controller, Host Controller, Controller</p>
---	--

References

- [User Manual](#)

[Manuals+](#), [Privacy Policy](#)

This website is an independent publication and is neither affiliated with nor endorsed by any of the trademark owners. The "Bluetooth®" word mark and logos are registered trademarks owned by Bluetooth SIG, Inc. The "Wi-Fi®" word mark and logos are registered trademarks owned by the Wi-Fi Alliance. Any use of these marks on this website does not imply any affiliation with or endorsement.