GOWIN IPUG1174-1.0E USB 2.0 Host Controller IP User Guide

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Contents

INTRODUCTION

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Revision History

Date	Version	Description
11/16/2023	1.0E	Initial version published.

List of Figures

List of Tables

About This Guide

Purpose

The purpose of Gowin USB 2.0 Host Controller IP User Guide is to help you learn the features and usage of Gowin USB 2.0 Host Controller IP by providing functional description, signal description and interface configuration. The software screenshots in this manual are based on 1.9.9 Beta-6. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

Related Documents

The latest user guides are available on the GOWINSEMI Website.
You can find the related documents at **www.gowinsemi.com/**:

- **DS100, GW1N series of FPGA Products Data Sheet**
- **DS117, GW1NR series of FPGA Products Data Sheet**
- **DS891, GW1NRF series of FPGA Products Data Sheet**
- **DS821, GW1NS series of FPGA Products Data Sheet**
- **DS871, GW1NSE series FPGA Products Data Sheet**
- **DS881, GW1NSER series FPGA Products Data Sheet**
- **DS861, GW1NSR series of FPGA Products Data Sheet**
- **DS102, GW2A series of FPGA Products Data Sheet**
- **DS226, GW2AR series of FPGA Products Data Sheet**
- **DS971, GW2AN-18X &9X Data Sheet**
- **DS976, GW2AN-55 Data Sheet**
- **DS981, GW5AT series of FPGA Products Data Sheet**
- **DS1103, GW5A series of FPGA Products Data Sheet**
- **DS981, GW5AST series of FPGA Products Data Sheet**
- **SUG100, Gowin Software User Guide**

Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DMA	Direct Memory Access
IP	Intellectual Property
PHY	Port Physical Layer
R/W	Read/Write
R/WC	Read/Write Clear
RO	Read Only
TD	Transmission Descriptor
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.
Website: www.gowinsemi.com
E-mail: support@gowinsemi.com

Introduction

Overview

Universal Serial Bus, commonly known as USB, is an external bus used to standardize the connection and communication between computers and external devices.
Gowin USB 2.0 Host Controller IP is based on the EHCI protocol, supporting SRAM interface, allowing connection to any microprocessor supporting the SRAM interface. It also supports ULPI interface, allowing connection to any USB 2.0 transceiver supporting the ULPI interface. It includes an internal 24K RAM space for storing transmission descriptors and data.

Table 2-1 Gowin USB 2.0 Host Controller IP Overview

Gowin USB 2.0 Host Controller IP	
Logic Resource	Please refer to Table 2-2
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9Beta-5 and above)

Note!
For the devices supported, you can click **here** to get the information.

Features

The features of Gowin USB 2.0 Host Controller IP are as follows:

- Supports high-speed (480 Mbps), full-speed (12Mbps), and low-speed (1.5Mbps)
- Supports device plug-and-play detection, reset, high-speed handshake, suspend, and wake-up
- Supports control transfer, bulk transfer, synchronous transfer, and interrupt transfer
- Supports split control transfer, split bulk transfer, split synchronous transfer, and split interrupt transfer
- Supports USB transceiver macrocell interface (ULPI)
- Supports SRAM interface as well as direct memory access (DMA) operations

Resource Utilization

Gowin USB 2.0 Host Controller IP can be implemented by Verilog language. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW2AN-18 series of FPGA as an instance, the resource utilization of Gowin USB 2.0 Host Controller IP is as shown in Table 2-2.

Table 2-2 Resource Utilization

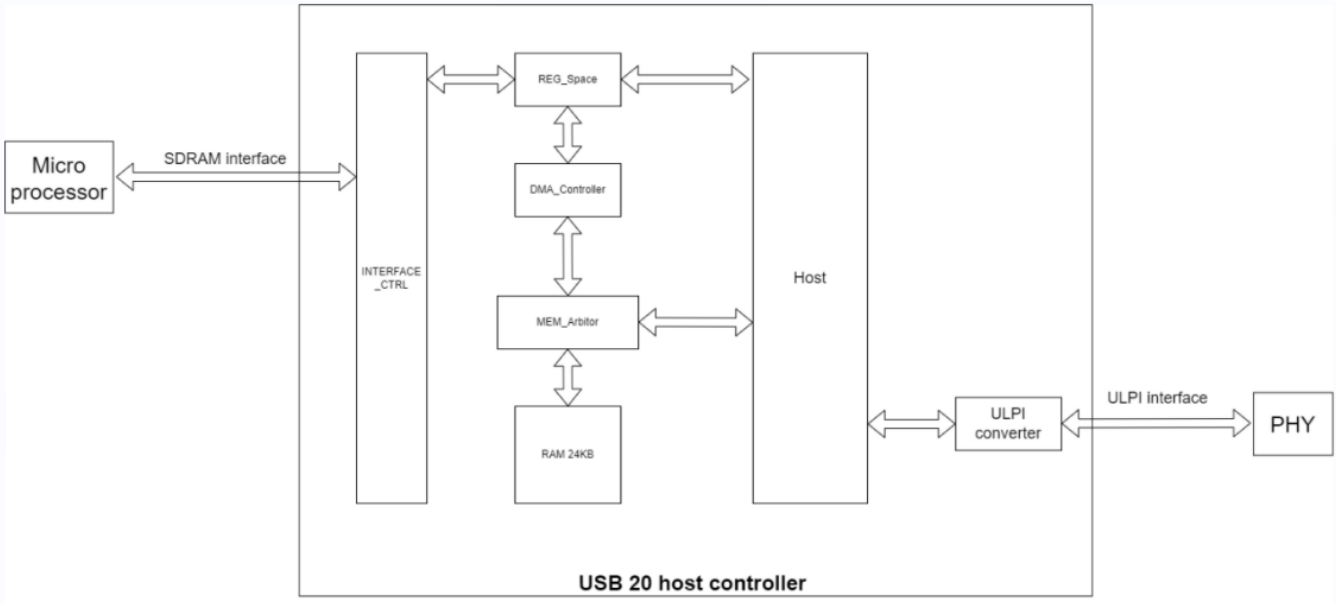
Device	**Speed Grade**	**Name**	**Resource Utilization**	**Note**
GW2AN-18	C7/I6	LUT	6981	–
		REG	3115	
		ALU	1253	
		BSRAM	277	

Functional Description

USB 2.0 Host Controller Structure

The USB 2.0 Host Controller is located between the microprocessor and downstream USB device. The USB 2.0 Host Controller links the microprocessor with downstream USB devices, receiving commands from the microprocessor, and facilitating data interaction between the microprocessor and the USB device. Figure 3-1 shows the block diagram of USB 2.0 host controller.

Figure 3-1 USB 2.0 Host Controller Block Diagram



Register Definition

This section introduces the internal register distribution of USB 2.0 Host Controller. The internal registers of the host controller include three categories: Capability registers, Operational registers, and DMA registers.

Table 3-1 Internal Register Distribution of USB 2.0 Host Controller

Address	Size(byte)	Mnemonic	Description
Capability Registers			
00h	1	CAPLENGTH	Capability Register Length
01h	1	Reserved	N/A
02h	2	HCIVERSION	Interface Version Number
04h	4	HCSPARAMS	Structural Parameters
08h	4	HCCPARAMS	Capability Parameters
Operational Registers			
0Ch	4	USBCMD	USB Command
10h	4	USBSTS	USB Status
14h	4	USBINTR	USB Interrupt Enable
18h	4	FRINDEX	USB Frame Index
1Ch	4	CTRLDSSEGMENT	4G Segment Selector
20h	4	PERIODICLISTBASE	Frame List Base Address
24h	4	ASYNCLISTADDR	Next Asynchronous List Address
1Ch – 3Fh		Reserved	N/A
4Ch	4	CONFIGFLAG	Configured Flag Register
50h	4	PORTSC	Port Status/Control
DMA Registers			
54h	4	MEMADDR	DMA initial address
58h	4	DMACONFIG	DMA configuration

Capability Register

You can see the Section 2.2 of the **Enhanced Host Controller Interface Specification for Universal Serial Bus protocol** for the definitions of each field in the Capability registers.

Operational Register

You can see the Section 2.3 of the **Enhanced Host Controller Interface Specification for Universal Serial Bus protocol** for the definitions of each field in the Operational registers.

DMA Register

MEMADDR (DMA Start Address)

Address 54h
Size: 32 bits

This register is used to store the start address for each DMA read/write.

Table 3-2 MEMADDR Register

Bit	Type	Default	Description
31:16	RO	16'b0	Reserved
15:0	R/W	16'b0	Start address for DMA read/write; the addressing rang e of the internal 24K RAM is from 0x0000 to 0x5FFF.

DMACONFIG (DMA Configuration)

Address 58h
Size:32 bits

This register is used to store each DMA read/write command.

Table 3-3 DMACONFIG Register

Bit	Type	Default	Description
31:18	RO	14'b0	Reserved
17	R/W	1'b0	DMA read/write **0:** DMA write **1:** DMA read
16	R/W	1'b0	DMA request **0:** Disable **1:** Enable
15:0	R/W	15'b0	DMA read/write data length; preset each DMA read/write dat a length, and the maximum value is 24K.

Signal Descriptions

Signal Definitions

Signal definitions of Gowin USB 2.0 Host Controller IP are as shown in Table 4-1.
Table 4-1 Signal Definition

No.	Signal Name	I/O	Data Width	Description
System Interface				
1	clk_i	I	1	Clock signal
2	rst_n_i	I	1	Reset signal, active-low
Host Controller SDRAM Interface				
3	cs_n_i	I	1	Chip selected signal, activ e-low
4	rd_n_i	I	1	Read enable signal, active -low
5	wr_n_i	I	1	Write enable signal, active -low
6	addr_i	I	8	Address bus
7	dack_i	I	1	DMA response signal; low level indicates that the us er responds to a DMA req uest
8	dreq_o	O	1	DMA request signal; high l evel indicates that the hos t controller is requesting a DMA
9	dat_io	IO	8	Data bus; When rd_n_i is high, it enters a high-impe dance state
10	hardware_int errupt_o	O	1	Host controller interrupt si gnal; high level indicates t hat the host controller gen erates an interrupt
Host Controller PHY Interface[1]				
11	phy_clk_o	O	1	ULPI PHY input clock
12	phy_rst_o	O	1	ULPI PHY reset signal
13	ulpi_dir_i	I	1	ULPI DIR signal
14	ulpi_data_io	IO	8	ULPI DATA signal
15	ulpi_nxt_i	I	1	ULPI NXT signal
16	ulpi_stp_o	O	1	ULPI STP signal

Note!
[1] This interface is used to connect external ULPI PHY.

USB 2.0 Host Controller SDRAM Interface Timing

When the user needs to read register, set cs_n_i to 0 and addr_i to register address, and control rd_n_i to generate a negative pulse. The read data will be output to dat_io waiting for Toe after the falling edge of rd_n_i.

When the user needs to write register, set cs_n_i to 0 and addr_i to register address, input the write data to dat_io, and control wr_n_i to generate a negative pulse. The write data will be written to the destination register waiting for Tadhw after the rising edge of wr_n_i.

Note!

- Each read and write operation to a register requires a unit of 4 bytes.
- For timing characteristics, see Table 4-2.

Figure 4-1 and Figure 4-2 are respectively the read and write register timing diagrams.

Figure 4-1 Timing Diagram of Host Controller Read Register

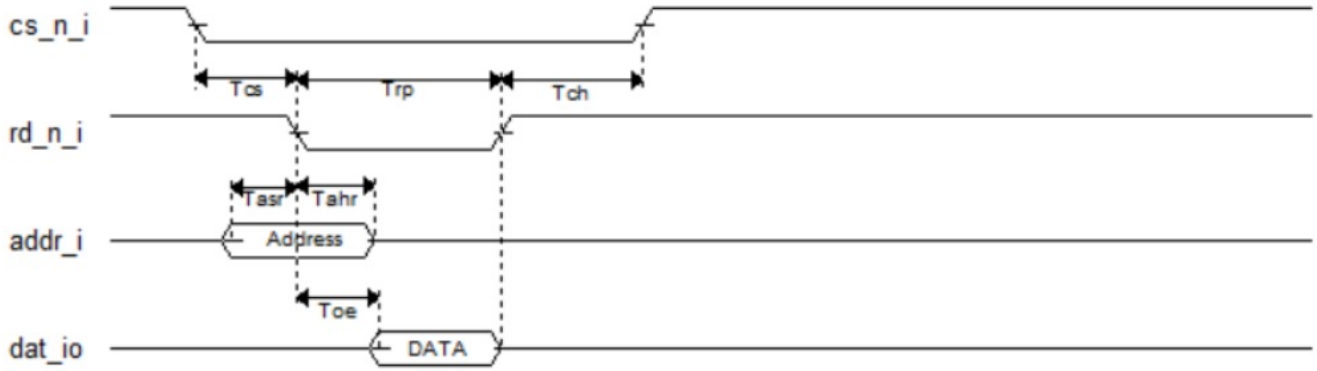
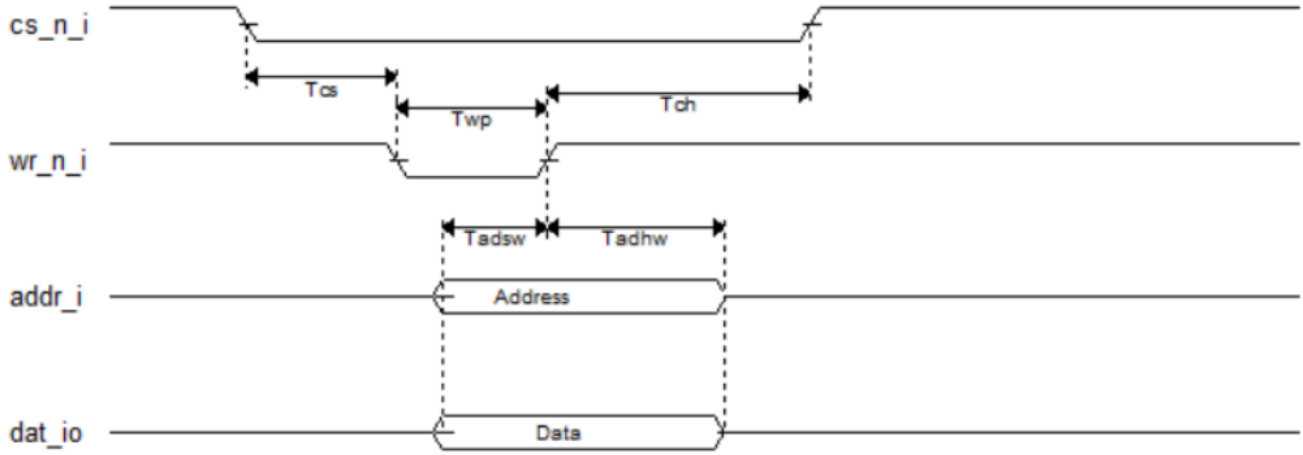


Figure 4-2 Timing Diagram of Host Controller Write Register



When the user needs to read or write internal RAM, it is necessary to initiate the process through the DMA method. If a DMA operation is required, the user first needs to write the start address to the MEMADDR register. Subsequently, the DMA write/read command along with the data length should be written to the DMACONFIG register, and the DMA enable field should be set to 1. Upon the host controller setting dreq_o to 1, the user sets dack_i to 0, entering DMA write/read mode.

During the DMA read process, the user controls rd_n_i to generate a negative pulse, and the host controller outputs the data in address order to the data bus waiting for Toe after each falling edge of rd_n_i.

During the DMA write process, the user controls wr_n_i to generate a negative pulse, and the host controller writes the data in address order to the internal RAM space on each rising edge of wr_n_i.

Throughout the DMA read/write process, the host controller calculates the number of wr_n_i/rd_n_i pulses. When the count reaches the byte length preset in DMACONFIG, the host controller sets dreq_o to 0, ending the current DMA operation.

Figure 4-3 and Figure 4-4 are respectively the DMA read and write timing diagrams.

Figure 4-3 Timing Diagram of Host Controller DMA Read

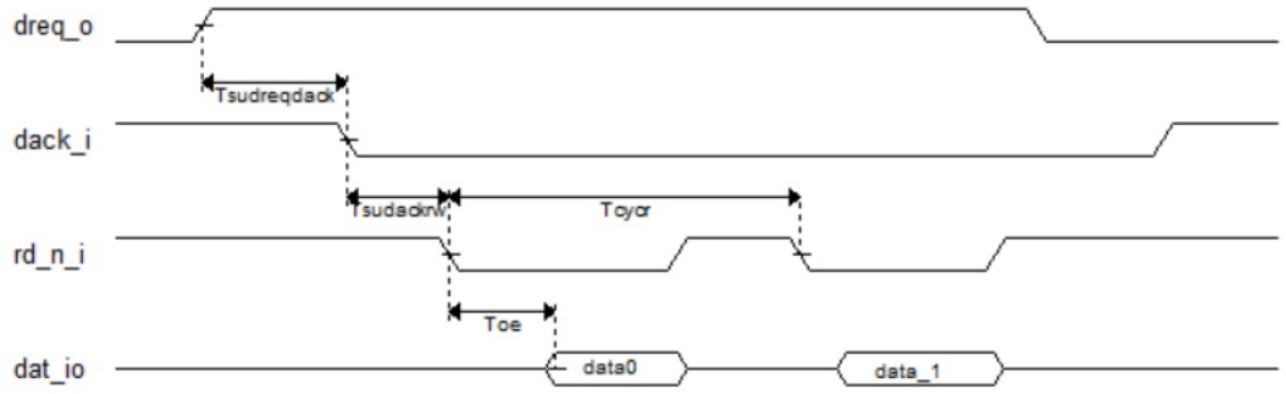


Figure 4-4 Timing Diagram of Host Controller DMA Write

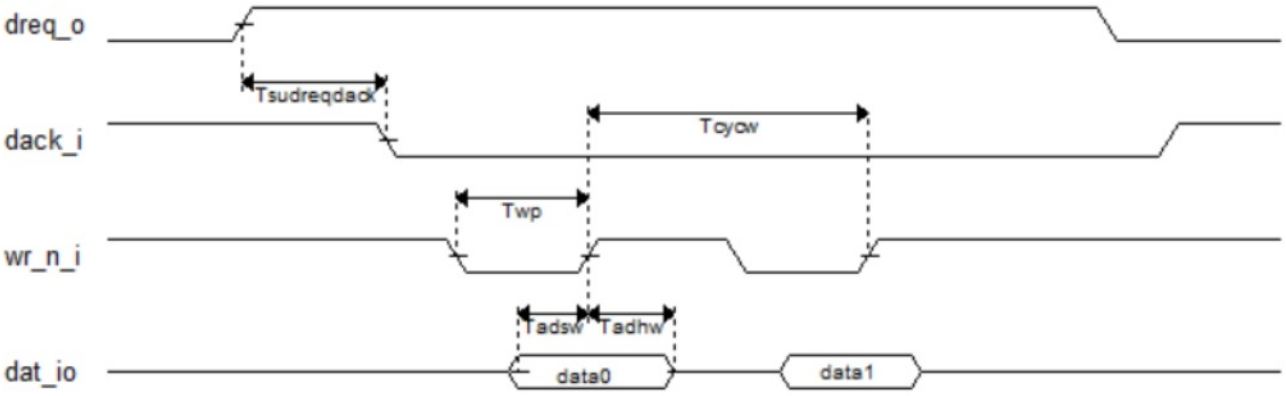


Table 4-2 Timing Characteristics

Parameter	Description	Min	Max	Unit
Tcs	The setup time of cs_n_i before wr_n_i/rd_n_i is set to 0	0	–	ns
Tch	The hold time of cs_n_i after wr_n_i/rd_n_i is set to 1	0	–	ns
Tadsw	The setup time of addr_i and dat_io before wr_n_i is set to 1	0	–	ns
Tadhw	The hold time of addr_i and dat_io after wr_n_i is set to 1	34	–	ns
Tasr	The setup time of addr_i before rd_n_i is set to 0	0	–	ns
Tahr	The hold time of addr_i after rd_n_i is set to 0	34	–	ns
Toe	Time from rd_n_i set to 0 to data valid	50	–	ns
Twp	wr_n_i pulse width	17	–	ns
Trp	rd_n_i pulse width	68	–	ns
Tsudreqdack	The setup time of dreq_o before dack_i is set to 0	0	–	ns
Tsudackrw	The hold time of dack_i before rd_n_i/wr_n_i is set to 0	0	–	ns
Tcycr	DMA read cycles	85	–	ns
Tcycw	DMA write cycles	51	–	ns

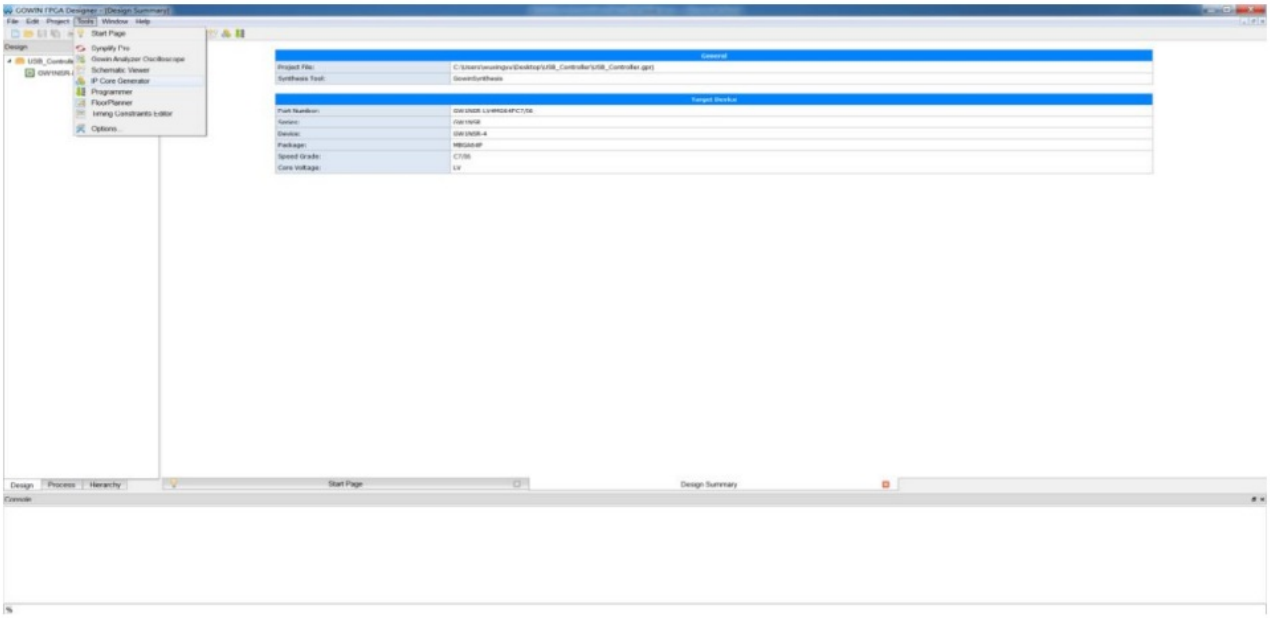
Interface Configuration

You can click “Tools > IP Core Generator” in Gowin Software to call and configure USB 2.0 Host Controller.

1. **Open IP Core Generator**

   After creating the project, you can click the “Tools” tab in the upper-left corner, then click the “IP Core Generator” via the drop-down list, as shown in Figure 5-1.

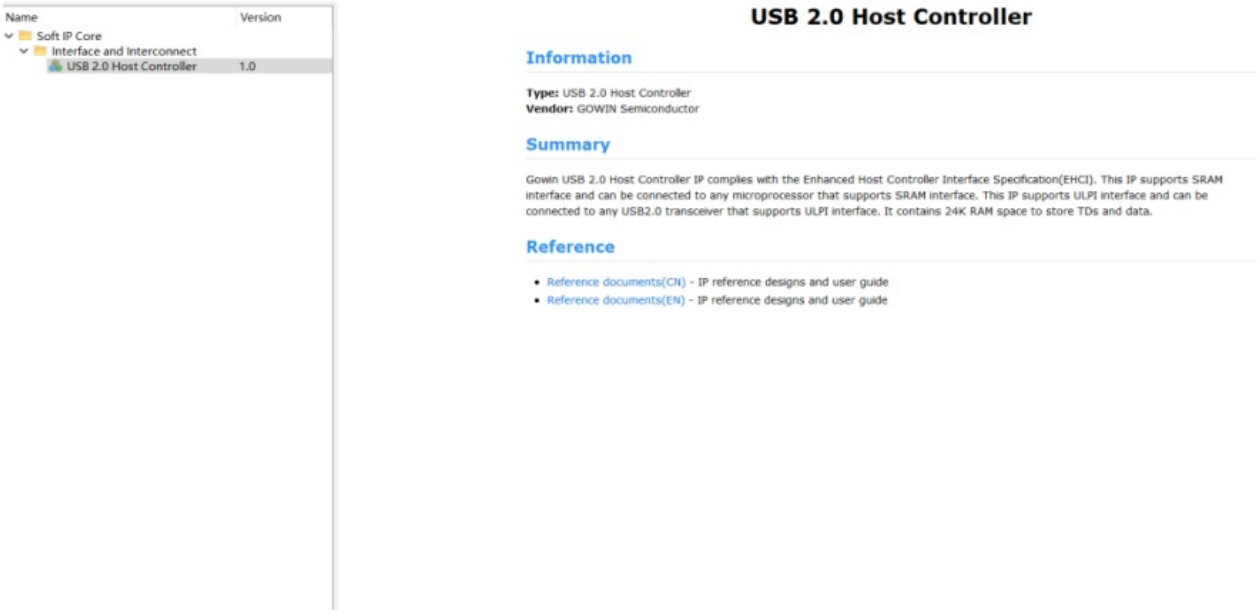
   Figure 5-1 IP Core Generator



2. **Open USB 2.0 Host Controller IP Core**

   Select “Soft IP Core > Interface and Interconnect > USB 2.0 Host Controller IP”, as shown in Figure 5-2. Double-click to open the configuration interface.

   Figure 5-2 USB 2.0 Host Controller IP Core

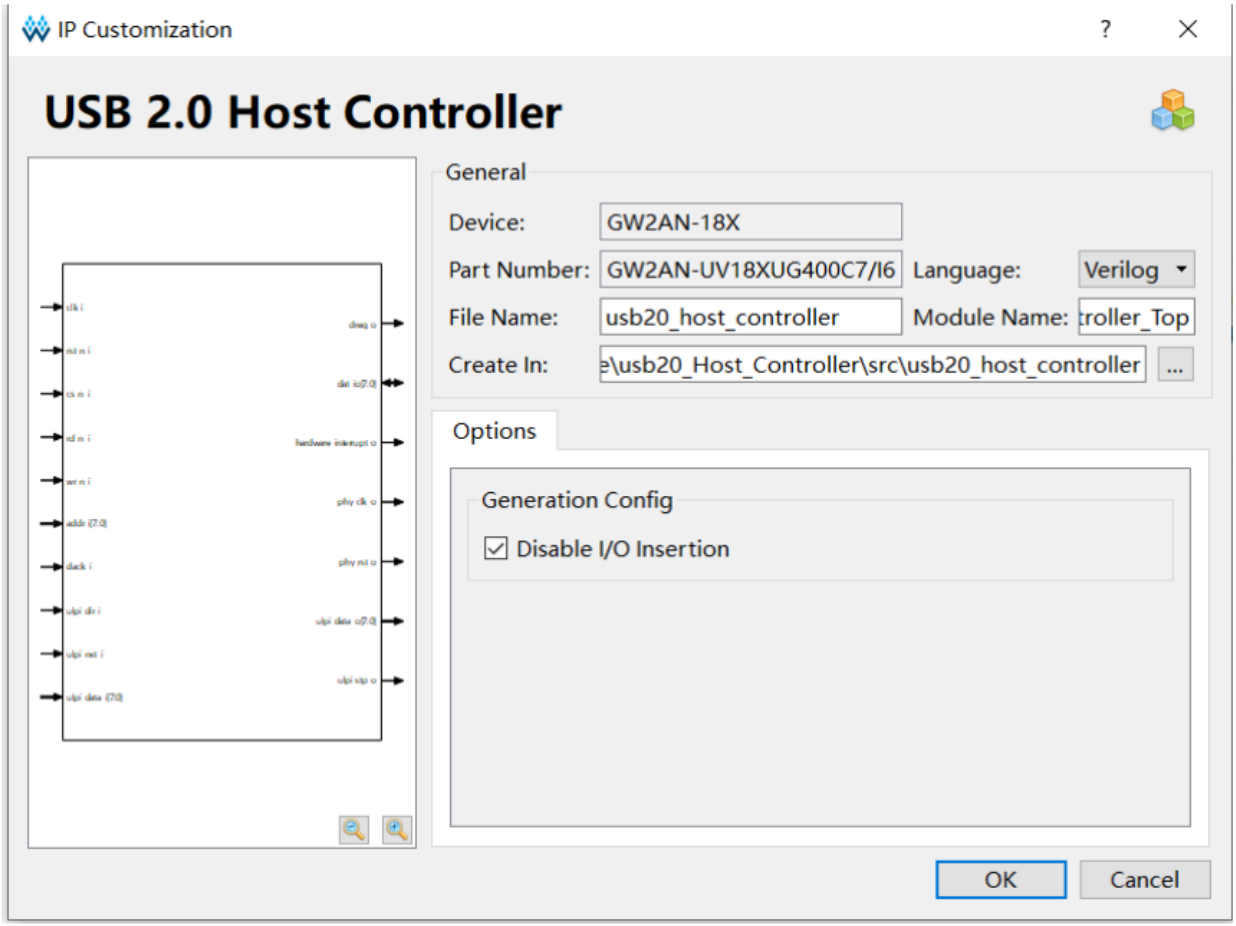


3. **USB 2.0 Host Controller IP Core Configuration Interface**

   The USB 2.0 Host Controller IP core configuration interface is shown in Figure 5-3. The port diagram is on the left, and the options are on the right.

   - You can configure the generated file name in “File Name” text box.
   - You can configure the generated top module name in “Module Name” text box.

     Figure 5-3 USB 2.0 Host Controller Configuration Interface



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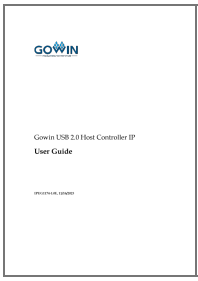	GOWIN IPUG1174-1.0E USB 2.0 Host Controller IP [pdf] User Guide IPUG1174-1.0E Gowin USB 2.0 Host Controller IP, IPUG1174-1.0E, Gowin USB 2.0 Host Controller IP, USB 2.0 Host Controller IP, 2.0 Host Controller IP, Host Controller IP, Controller IP

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