GOWIN IPUG1082 Reed Solomon Encoder IP User Guide

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About This Guide

Purpose

The purpose of Gowin Reed-Solomon Encoder IP User Guide is to help you learn the features and usage of Gowin Reed-Solomon Encoder IP by providing the descriptions of functions, ports, timing, GUI and reference design. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.9.01 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- DS100, GW1N series of FPGA Products Datawww.gowinsemi.com: Sheet
- DS117, GW1NR series of FPGA Products Data Sheet
- DS821, GW1NS series of FPGA Products Data Sheet

- DS861, GW1NSR series of FPGA Products Data Sheet
- DS841, GW1NZ series of FPGA Products Data Sheet
- S891, GW1NSE series FPGA Products Data Sheet
- DS961, GW2ANR series of FPGA Products Data Sheet
- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- DS971, GW2AN-18X & 9X Data Sheet
- DS976, GW2AN-55 Data Sheet
- DS981, GW5AT series of FPGA Products Data Sheet
- DS1103, GW5A series of FPGA Products Data Sheet
- DS1104, GW5AST series of FPGA Products Data Sheet
- DS1108, GW5AR series of FPGA Products Data Sheet
- DS1105, GW5AS series of FPGA Products Data Sheet
- SUG100, Gowin Software User Guide

Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
BSRAM	Block Static Random Access Memory
DSP	Digital Signal Processing
ECC	Error Checking and Correction
IP	Intellectual Property
SRAM	Static Random Access Memory

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.
Website: www.gowinsemi.com
E-mail: support@gowinsemi.com

Overview

Gowin Reed-Solomon Encoder IP Introduction

Gowin Reed-Solomon Encoder IP is an encoder based on the principles of Reed-Solomon, capable of encoding input information using primitive polynomials. This IP can be utilized for data error checking and correction.

Table 2-1 Gowin Reed-Solomon Encoder IP

Gowin Reed-Solomon Encoder IP	
IP Core Application	
Logic Resource	Please refer to Table 2-2
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.01 and above)

Note!
For the devices supported, you can click here to get the information.

Features

- Configurable input and output data width
- Configurable codeword length
- Configurable message length
- Configurable Galois fieldx

Max. Frequency

The maximum frequency of Gowin Reed-Solomon Encoder IP is mainly determined by the speed grade of the devices and configuration parameters. For example, when using GW2A-55 series of devices, the system clock can reach up to 250MHz

Latency

The latency of Gowin Reed-Solomon Encoder IP usually depends on the codeword length and message length

Resource Utilization

Gowin Reed-Solomon Encoder IP resource utilization mainly depends on the configuration of codeword length and message length. The resource utilization may be different with different devices.

Take GW2A-55 series of FPGA as an example, Gowin Reed-Solomon

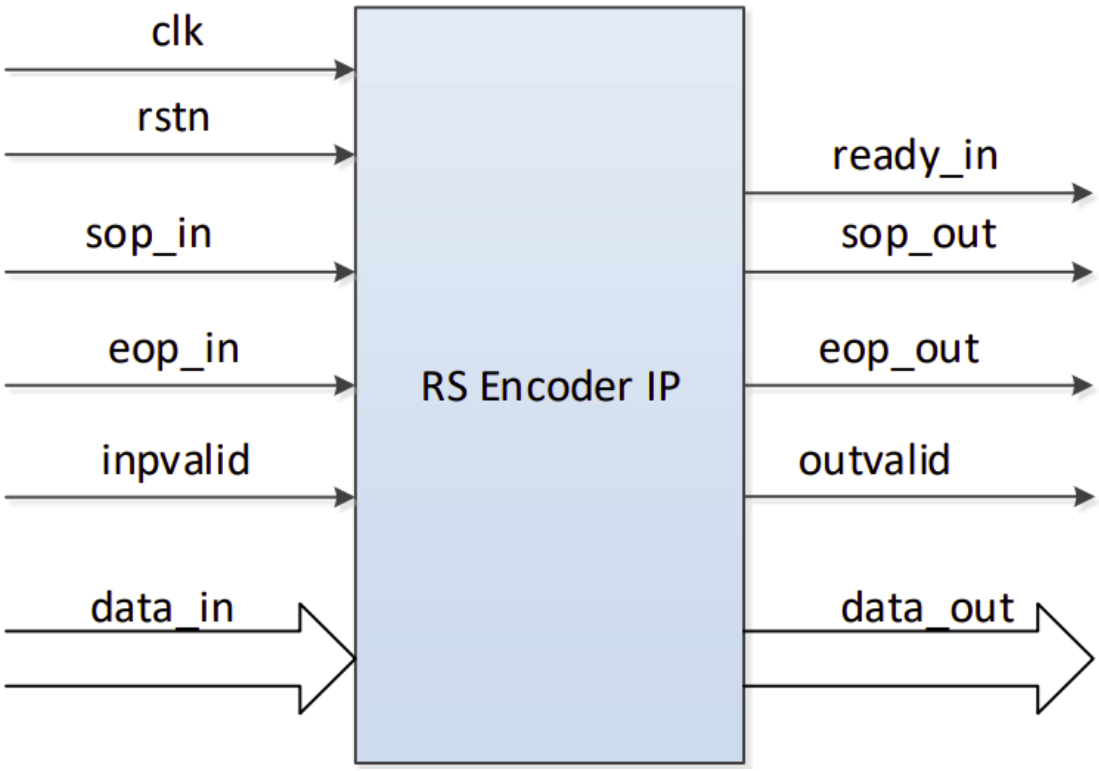
Encoder IP resource utilization is as shown in Table 2-2.

Functional Description

System Block Diagram
Gowin Reed-Solomon Encoder IP computes check codes based on the input data and produces the output, and

the block diagram is shown in Figure 3-1.

Figure 3-1 Gowin Reed-Solomon IP Block Diagram



Algorithm Introduction

The Reed-Solomon Code is a non-binary BCH code. Due to its simple structure, short decoding delay, rich structural characteristics, and strong error-correction capabilities, Reed-Solomon codes are well-suited for correcting both random and burst errors. They are particularly suitable for channels with burst errors, making Reed-Solomon codes indispensable in the field of error control coding. Reed-Solomon codes find widespread applications in digital storage, deep space communication, optical fiber communication, and various other domains.

The encoding algorithm of Reed-Solomon codes can be implemented

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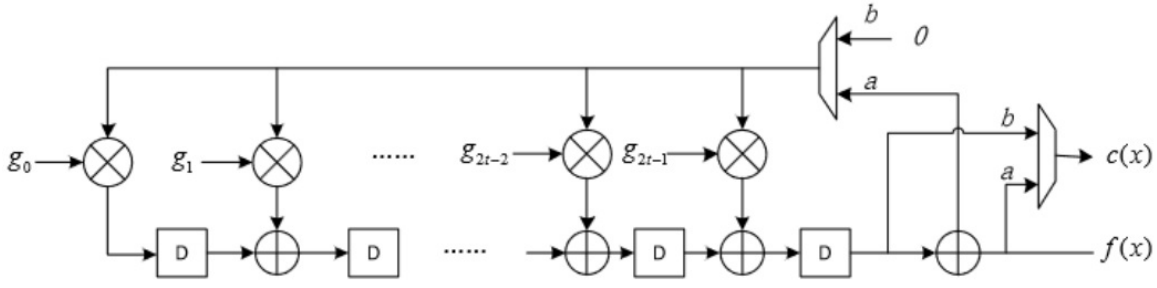


Port Description

The IO ports of Gowin Reed-Solomon Encoder IP are shown in Figure

4-1. For the details, you can see Table 4-1.

Figure 4-1 Gowin Reed-Solomon Encoder IP I/O Port Diagram

Table 4-1 I/O List of Gowin Reed-Solomon Encoder IP

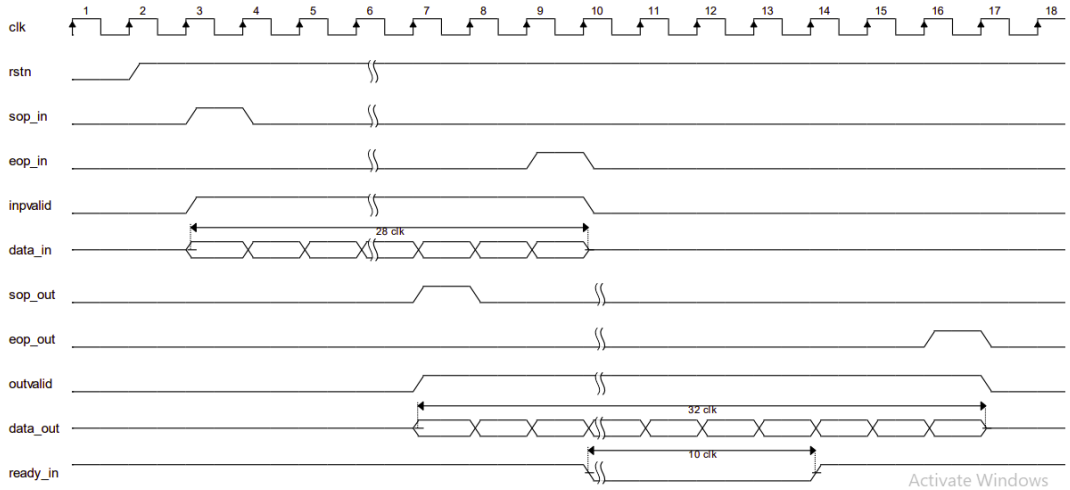
Signal	I/O	Data Width	Description
clk	I	1	Input clock signal
rstn	I	1	Reset signal, active-low
sop_in	I	1	Start signal for input data
eop_in	I	1	End signal for input data
inpvalid	I	1	Input data valid signal
data_din	I	Variable	Input data signal
sop_out	O	1	Start signal for output data
eop_out	O	1	End signal for output data
outvalid	O	1	Output valid signal, active-high.

Signal	I/O	Data Width	Description
data_out	O	Variable	Output data signal
ready_in	O	Variable	Ready signal

Timing Description

This chapter mainly introduces the timing of Gowin Reed-Solomon Encoder IP. Under the default configuration, the input valid data cycle is 28, and the output valid data cycle is 32. After Gowin Reed-Solomon Encoder IP operation, the data will be output with a delay of 7 clock cycles. For the IP timing, see Figure 5-1.

Figure 5-1 Gowin Reed-Solomon Encoder IP Timing Diagram

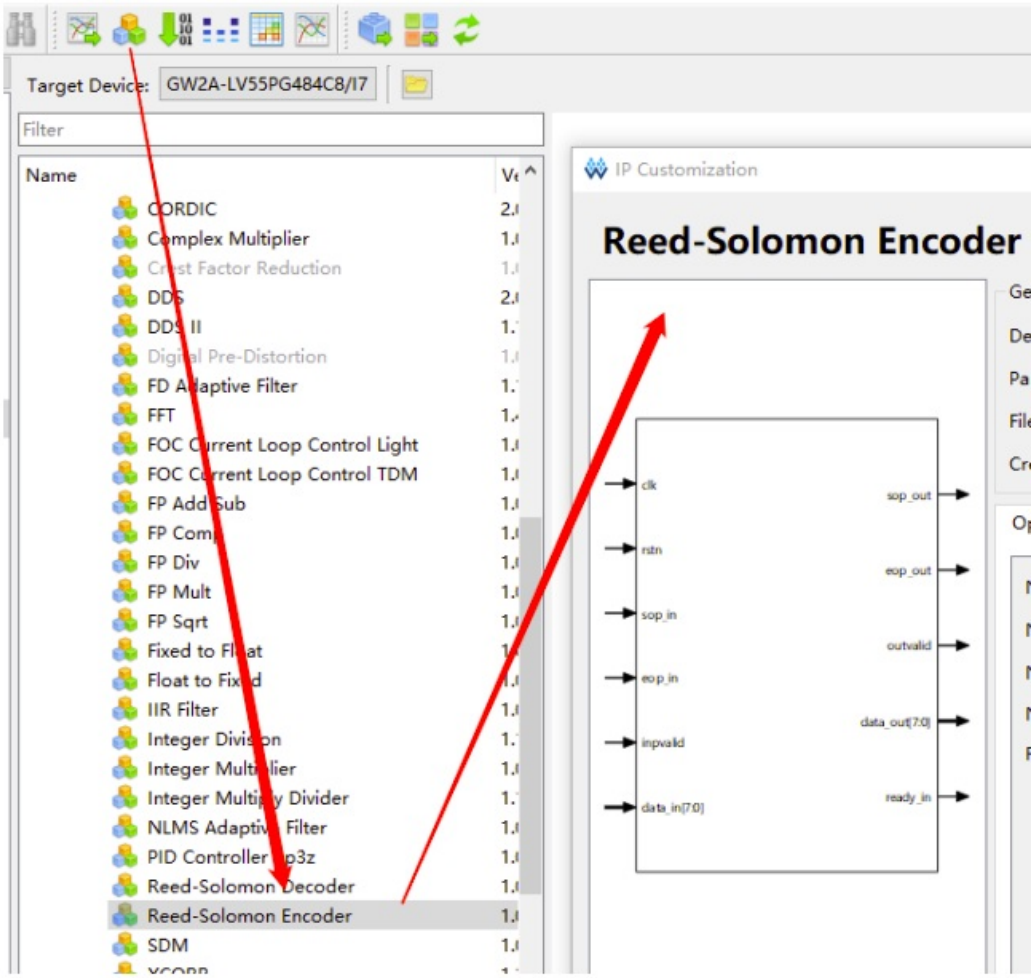


As shown in the Figure 5-1, when data enters the IP, the sop_in signal needs to be pulled high during the first clock cycle of input, and the eop_in signal needs to be pulled high during the last clock cycle. For the rest of the time, these signals should be kept low. The inpvalid signal should remain high throughout the periods of valid data. The ready_in signal is high by default, and will be pulled low after the eop_in signal becomes high, and will not be pulled high again until the next set of data can be input. When the IP outputs data, the sop_out signal will be pulled high in the first cycle of the output, and the eop_in signal will be pulled high in the last cycle; For the rest of the time, these signals should be kept low. The outvalid signal will be continuously pulled high during the cycle when the data is valid.

Interface Configuration

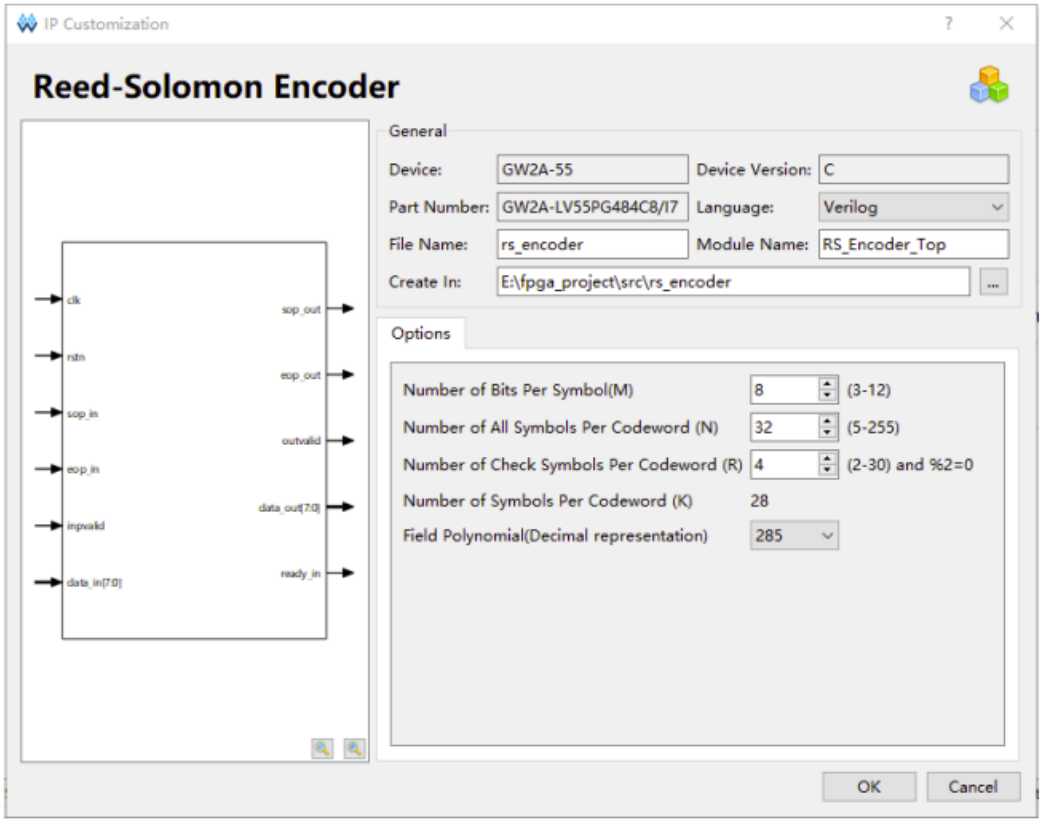
Click “Tools > IP Core Generator > DSP and Mathematics” to call and configure Reed-Solomon Encoder; toolbar icon is also available as shown in Figure 6-1.

Figure 6-1 Open GUI Via Icon



Gowin Reed-Solomon Encoder IP configuration interface is shown in Figure 6-2.

Figure 6-2 Gowin Reed-Solomon Encoder IP Configuration Interface



- You can configure the generated file name in “File Name” text box.
- You can configure the module name in “Module Name” text box.
- You can configure IP working mode and other under “Options” tab. Gowin Reed-Solomon Encoder IP configuration options are as shown

Table 6-1 Gowin Reed-Solomon Encoder IP Configuration

Options	Description
Number of Bits Per Symbol	Data width, 3-12 bits
Number of All Symbol Per Codeword	Number of codeword, 5-255
Number of Check Symbols Per Codeword	Number of check symbols, 2-30
Codeword Length	Codeword length, determined by Galois field
Field Polynomial	Field polynomial, determined by Galois field

Reference Design

Please refer to the related test cases in RefDesign.

File Delivery

The delivery file of Gowin Reed Solomon Encoder IP includes documentation and reference design.

Documentation

The folder contains the user guide in PDF version.

Table 8-1 Document List

Name	Description
IPUG1082, Gowin Reed Solomon Encoder IP User Guide	Gowin IP User Guide, namely this one.

Reference Design

The Ref. Design folder contains the netlist file, the user reference design, the constraints file, the top file, and the project folder, etc. Table 8-2 Ref. Design File List

Name	Description
RS_exp.v	Top module and stimulus generation module of reference design
rs_encoder.vo	Reed-Solomon Encoder IP netlist file
demo.cst	Reed-Solomon Encoder IP constraints file
fpga_project.gao	Capture output data of Reed-Solomon Encoder IP
rs_encoder	Reed-Solomon Encoder IP project folder

Documents / Resources

	GOWIN IPUG1082 Reed Solomon Encoder IP [pdf] User Guide IPUG1082 Reed Solomon Encoder IP, IPUG1082, Reed Solomon Encoder IP, Solomon Encoder IP, Encoder IP

References

- Home|GOWIN Semiconductor
- Home|GOWIN Semiconductor
- IP and Reference Design | Gowin
- User Manual