GOWIN GW5AS Series FPGA Products Package and Pinout User Guide

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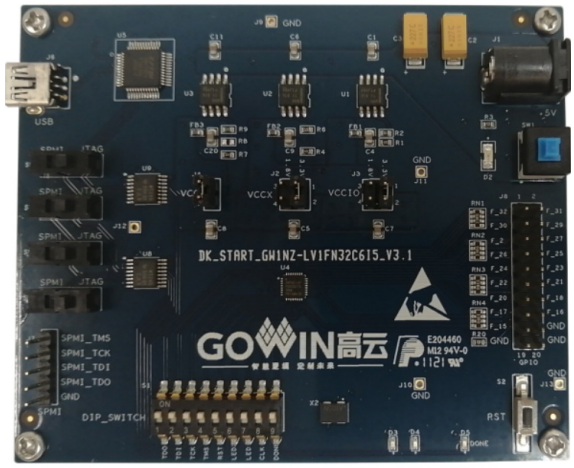


About This Guide

Purpose

This manual introduces Gowin GW5AS series of FPGA product package and provides pin definitions, a list of pin numbers, pin distribution view, and package diagrams.

Related Documents

The latest user guides are available on the GOWINSEMI Website.
You can find the related documents at **www.gowinsemi.com**:

- **DS1114, GW5AS-138 Data Sheet**
- **UG1107, GW5AS-138 Pinout**
- **DS1105, GW5AS-25 Data Sheet**
- **UG1115, GW5AS-25 Pinout**

Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in **Table 1-1**.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
UG	UBGA Package

Support and Feedback

Gowin Semiconductor provides customers with comprehensive
technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.
Website: **www.gowinsemi.com**
E-mail: **support@gowinsemi.com**

Overview

GOWINSEMI GW5AS-138 devices are the 5th-generation of Arora family, with abundant internal resources, a new-architecture and high-

performance DSP supporting AI operations, high-speed LVDS interfaces, and abundant BSRAM resources. At the same time, GW5AS-138 devices integrate a hardcore processor RiscV AE350_SOC, self-developed DDR3, and provide a variety of packages. They are suitable for applications such as low power, high performance and compatibility designs.

Gowin provides a new generation of FPGA hardware development environment that supports FPGA synthesis, placement & routing, bitstream generation and download, etc.

PB-Free Package

GW5AS series of FPGA products are PB free in line with the EU RoHS environmental directives. The substances used in the GW5AS series of FPGA products are in full compliance with the IPC-1752 standards.

Package and Max. User I/O Information

Table 2-1 Package, Max. User I/O Information, and LVDS Pairs

Package	Pitch (mm)	Size (mm)	E-pad Size (mm)	GW5AS-25	GW5AS-138
UG324A	0.8	15 x 15	–	–	221 (106)
UG256	0.8	14 x 14	–	144 (68)	–

Note!

For package type abbreviations employed in this manual, see 1.3 Terminology and Abbreviations.

Power Pins

Table 2-2 GW5AS Power Pins

VCCIO0	VCCIO1	VCCIO2	VCCIO3
VCCIO4	VCCIO5	VCCIO6	VCCIO7
VCCIO10	VCC	VCCX	VCC_EXT
VCCC	VCC_REG	M0_VDDX	M1_VDDX
M0_VDD_12	VQPS	VSS	–

Pin Quantity

Quantity of GW5AS-138 Pins

Table 2-3 Quantity of GW5AS-138 Pins

Pin Type		GW5AS-138
		UG324A
Single-ended IO/ Differential pair/LVDS[1]	BANK0	0/0/0
	BANK1	0/0/0
	BANK2	50/24/24
	BANK3	0/0/0
	BANK4	50/24/24
	BANK5	50/24/24
	BANK6	50/24/24

	BANK7	10/4/4
	BANK10	12/6/6
	BANK11	0/0/0
Max. User I/O[2]		221
Differential Pair		106
True LVDS Output		106
VCCIO2		6
VCCIO4		6
VCCIO5		6
VCCIO6		6
VCCIO7		1
VCC/VCCC		14
VCC_REG		1
VCCIO10		1
VCCX/M0_VDDX/M1_VDDX		4
VSS		48
MODE0		1
MODE1		1
MODE2		1

Pin Type	GW5AS-138
	UG324A
NC	5

Note!

- [1] Single-ended/Differential I/O quantity includes CLK pins and download
- [2] RECONFIG_N pin cannot be multiplexed as I/O.

Quantity of GW5AS-25 Pins

Table 2-4 Quantity of GW5AS-25 Pins

Pin Type		GW5AS-25
		UG256
Single-ended IO/ Differential pair/LVDS[1]	BANK0	1/0/0
	BANK1	8/4/4
	BANK2	19/9/9
	BANK3	28/14/14
	BANK4	35/17/17
	BANK5	27/13/13
	BANK6	12/6/6
	BANK7	10/5/5
	BANK10	4/2/0
	BANK11	0/0/0
Max. User I/O		144

Differential Pair	70
True LVDS Output	68
VCCIO0/VCCIO1/VCCIO10/VCCIO2/ VCCIO6/VCCIO7	3
VCCIO3/VCCIO4	2
VCCIO5	2
M0_VDDX/VCCX	1
M0_VDD_12	1
VCC_EXT	8
VCC_REG	1
VQPS	1
VSS	23
MODE0	1
MODE1	1
MODE2	1
NC	0
MCU	30

Note!

[1] Single-ended/Differential I/O quantity includes CLK pins and download pins.

I/O BANK Introduction

GW5AS-25 has eight GPIO Banks. In addition, Bank 10 is JTAG Bank, Bank 11 is a Reserved Bank.
See ***DS1105, GW5AS-25 Data Sheet*** *> 2.3 Input/Output Blocks* for details.
GW5AS-138 has six GPIO Banks (Bank2~7) and a Bank for configuration (Bank 10).
See ***DS1114, GW5AS-138 Data Sheet*** *> 2.3 Input/Output Blocks* for details.

This manual provides the pin distribution view of GW5AS series of FPGA products. For details, please refer to Chapter **3 View of Pin Distribution**. The I/O Banks that form GW5AS series of FPGA products are marked with different colors. Various symbols and colors are used for the user I/O, power, and ground. The various symbols and colors used for the various pins are defined as follows:

- " " denotes the I/O in BANK0
- " " denotes the I/O in BANK1
- " " denotes the I/O in BANK2
- " " denotes the I/O in BANK3
- " " denotes the I/O in BANK4
- " " denotes the I/O in BANK5
- " " denotes the I/O in BANK6
- " " denotes the I/O in BANK7
- " " denotes the I/O in BANK10
- " " denotes the I/O in BANK11
- " " denotes the DIO in MIPI and ADC
- " " denotes VCC, VCCX, VCCIO, and the filling color does not change
- " " denotes VSS, and the filling color does not change
- " " denotes NC

View of Pin Distribution

View of GW5AS-138 Pin Distribution

View of UG324A Pin Distribution

Figure 3-1 View of GW5AS-138 UG324A Pin Distribution (Top View)

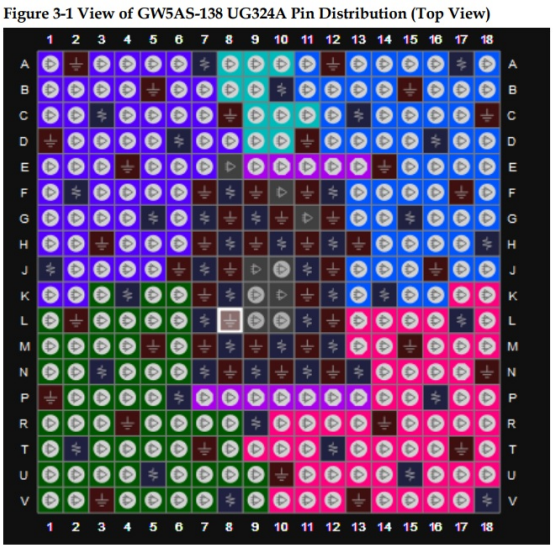


Table 3-1 Other Pins in GW5AS-138 UG324A

VCCIO2	C13,H18,G15,K14,A17,D16
VCCIO4	N13,U15,T12,P16,L17,V18
VCCIO5	K4,V8,T2,N3,U5P6
VCCIO6	D6,F2,G5,A7,J1,C3
VCCIO7	B10
VCCIO10	R9
VCC/VCCC	N7,F8,G7,L7,H8,L11,N9,M10,J11,K8,J7,G9,N11,M 8
VCC_REG	H10
VCCX/M0_VDDX/M1_VDDX	H12,K12,F12,M12
VSS	A12,A2,B15,B5,C18,C8,D11,D1,E14,E4,F17,F11,F 9,F7,G12,G10,G 8,H13,H11,H7,H3,J16,J12,J8,J6, K11,K7,L12,L8,L2,M15,M11,M9,M7,M5,N18,N12,N 10,N8,P1,R14,R 4,T17,T7,U10,V13,H9,V3

View of GW5AS-25 Pin Distribution

View of UG256 Pin Distribution

Figure 3-2 View of GW5AS-138 UG324A Pin Distribution (Top View)

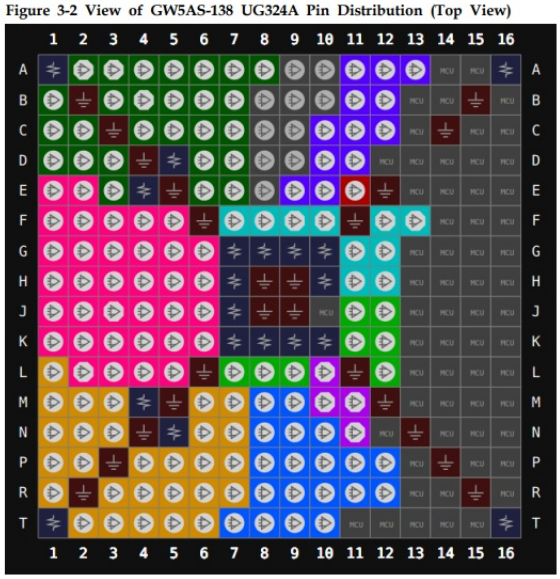


Table 3-2 Other Pins in GW5AS-25 UG256

VCCIO0/VCCIO1/VCCIO10/ VCCIO2/VCCIO6/VCCIO7	H10,K9,G9
VCCIO3/VCCIO4	M4,N5
VCCIO5	D5,J7
M0_VDDX/VCCX	G8
M0_VDD_12	E4
VCC_EXT	G10,A1,G7,T16,T1,K10,K7,A16
VCC_REG	H7
VQPS	K8
VSS	B15,C3,C14,D4,E5,E12,F6,F11,H8,H9,J8,J9,L6,L 11,M5,M12,N4,N13,P3,P14,R2,R15,B2

4.1 UG324A Package Outline (15mm x 15mm, GW5AS-138)

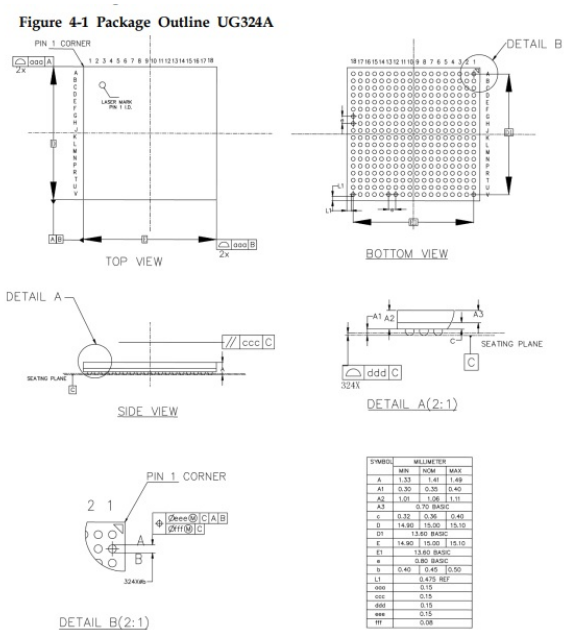
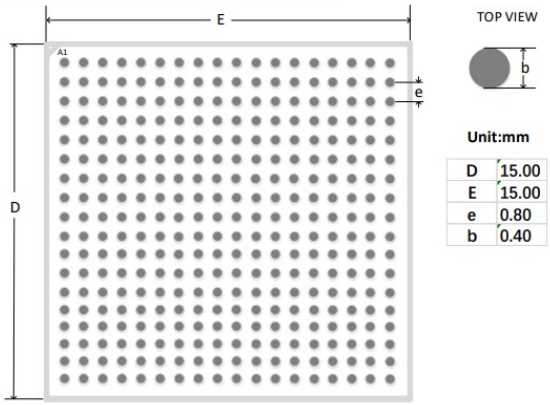


Figure 4-2 Recommended PCB Layout UG324A

Figure 4-2 Recommended PCB Layout UG324A

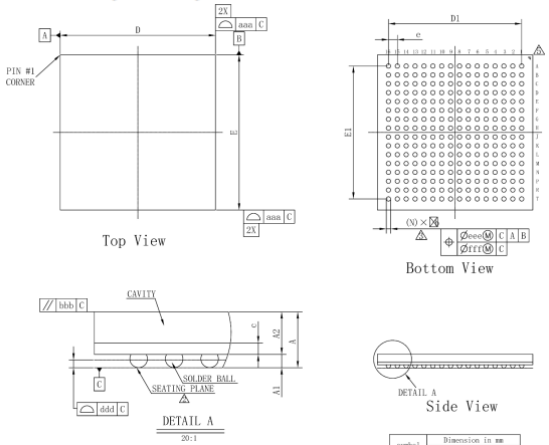


Unit:mm

D	15.00
E	15.00
e	0.80
b	0.40

4.2 UG256 Package Outline (14mm x 14mm, GW5AS-25)

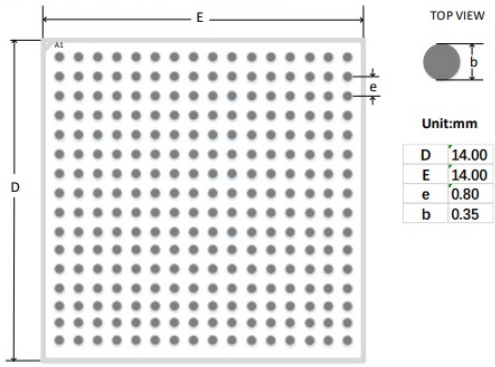
Figure 4-3 Package Outline UG256



symbol	Dimension in mm		
	MIN	NOM	MAX
A	----	----	1.360
A1	0.250	0.300	0.350
A2	0.910	0.960	1.010
c	0.220	0.260	0.300
D	13.900	14.000	14.100
E	13.900	14.000	14.100
D1	----	12.000	----
E1	----	12.000	----
e	----	0.800	----
b	0.350	0.400	0.450
aaa	0.150		
bbb	0.200		
ddd	0.100		
eee	0.150		
fff	0.080		
Ball Diam	0.400		
N	256		
MD/ME	16/16		

Figure 4-4 Recommended PCB Layout UG256

Figure 4-4 Recommended PCB Layout UG256



Unit:mm

D	14.00
E	14.00
e	0.80
b	0.35

Documents / Resources

	GOWIN GW5AS Series FPGA Products Package and Pinout [pdf] User Guide GW5AS-25, GW5AS-138, GW5AS Series of FPGA Products Package and Pinout, GW5AS Series, GW5AS Series FPGA Products, FPGA Products Package and Pinout, FPGA Products, FPGA

References

- Home|GOWIN Semiconductor
- Home|GOWIN Semiconductor
- User Manual