GOWIN GW1NRF Series Bluetooth FPGA Products Package and Pinout User Guide

Contents

GOWIN GW1NRF Series Bluetooth FPGA Products Package and Pinout

Specifications

- **Product Name:** GW1NRF series of Bluetooth FPGA Products
- **Package & Pinout User Guide:** UG893-1.0.1E
- **Trademark:** Guangdong Gowin Semiconductor Corporation
- **Registered Trademarks:** China, U.S. Patent and Trademark Office, and other countries

About This Guide

1. **Purpose**
   This manual provides an introduction to the GW1NRF series of Bluetooth FPGA products. It includes information about the pins, pin numbers, pin distribution, and package diagrams.
2. **Related Documents**
   This guide should be used in conjunction with the following documents:
   - GOWINSEMI Terms and Conditions of Sale

Overview

1. GW1NRF Series of Bluetooth FPGA Products
   The GW1NRF series is a range of Bluetooth FPGA products developed by Guangdong Gowin Semiconductor Corporation. These products combine the flexibility of FPGA technology with Bluetooth connectivity, allowing users to create custom Bluetooth-enabled applications.

View of Pin Distribution

1. **View of GW1NRF-4B Pins Distribution**
   The GW1NRF-4B package has a specific pin distribution. Refer to Table 2-4 in Chapter 2.5 for the definition of each pin.

2. **View of QN48 Pins Distribution**

   The QN48 package has a specific pin distribution. Refer to Table 2-4 in Chapter 2.5 for the definition of each pin.

    1. **View of QN48E Pins Distribution**

       The QN48E package has a specific pin distribution. Refer to Table 2-4 in Chapter 2.5 for the definition of each pin.

Package Diagrams

1. QN48 Package Outline (6mm x 6mm)

   The QN48 package is a square outline measuring 6mm x 6mm. It contains the pins necessary for the GW1NRF series of Bluetooth FPGA products.
2. QN48E Package Outline (6mm x 6mm)

   The QN48E package is a square outline measuring 6mm x 6mm. It contains the pins necessary for the GW1NRF series of Bluetooth FPGA products.

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GW1NRF series of Bluetooth FPGA Products Package & Pinout User Guide

- UG893-1.0.1E, 12/15/2022
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Revision History

Date	Version	Description
11/12/2019	1.0E	Initial version published.
12/15/2022	1.0.1E	1. Package diagrams updated. 2. The note of Table 2-4 "Definition of the Pins in the GW1NRF series of Bluetooth FPGA products" in Chapter 2.5 "Pin Definitions" added.

About This Guide

Purpose
This manual contains an introduction to the GW1NRF series of Bluetooth FPGA products together with a definition of the pins, list of pin numbers, distribution of pins, and package diagrams.

Related Documents
The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com :

1. DS891, GW1NRF series of Bluetooth FPGA products Data Sheet
2. UG290, Gowin FPGA Products Programming and Configuration User Guide
3. UG893, GW1NRF series of Bluetooth FPGA products Package and Pinout
4. UG892, GW1NRF-4B Pinout

Terminology and Abbreviations
The terminology and abbreviations used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviation and Terminology

Terminology and Abbreviations	Full Name
FPGA	Field Programmable Gate Array
SIP	System in Package
GPIO	Gowin Programmable IO
QN48	QFN48
QN48E	QFN48E

Support and Feedback
Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

- **Website:** www.gowinsemi.com

- **E-mail:** support@gowinsemi.com

Overview

The GW1NRF series of FPGA products are the first generation products in the LittleBee® family and represent one form of SoC FPGA. The GW1NRF series of FPGA products integrate 32 bits hardcore processor and support Bluetooth 5.0 Low Energy radio. They have abundant logic units, IOs, built-in B-SRAM and DSP resources, power management module, and security module. The GW1NRF series provides low power consumption, instant on, low cost, non-volatile, high security, various packages, and flexible usage.

PB-Free Package
The GW1NRF series of Bluetooth FPGA products are PB free in line with the EU ROHS environmental directives. The substances used in the GW1NRF series of Bluetooth FPGA products are in full compliance with the IPC-1752 standards.

Package, Max. User I/O Information, and LVDS Paris
Table 2-1 Package, Max. User I/O Information, and LVDS Paris

Package	Pitch (mm)	Size (mm)	GW1NRF-4B
QN48	0.4	6 x 6	25(4)
QN48E	0.4	6 x 6	25(4)

Note

- In this manual, abbreviations are employed to refer to the package types. See 1.3Terminology and Abbreviations.
- See GW1NRF series of Bluetooth FPGA Products Data Sheet for more details.
- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;

Power Pin
Table 2-2 Other Pins in the GW1NRF Series

VCC	VCCO0	VCCO1	VCCO2
VCCO3	VCCX	VSS	

Pin Quantity
Quantity of GW1NRF-4B Pins

Table 2-3 Quantity of GW1NRF-4B Pins

Pin Type		GW1NRF-4B	
		QN48	QN48E
	BANK0	9/4/0	9/4/0

I/O Single end / Differential pair / LVDS[1]	BANK1	4/1/1	4/1/1
	BANK2	8/4/3	8/4/3
	BANK3	4/1/0	4/1/0
Max. User I/O[2]		25	25
Differential Pair		10	10
True LVDS output		4	4
VCC		2	2
VCCX		1	1
VCCO0/VCCO3[3]		1	1
VCCO1/VCCO2[3]		1	1
VSS		2	1
MODE0		0	0
MODE1		0	0
MODE2		0	0
JTAGSEL_N		1	1
Pin Type		GW1NRF-4B	
		QN48	QN48E
I/O Single end / Differential pair / LVDS[1]	BANK0	9/4/0	9/4/0
	BANK1	4/1/1	4/1/1
	BANK2	8/4/3	8/4/3
	BANK3	4/1/0	4/1/0
Max. User I/O[2]		25	25
Differential Pair		10	10
True LVDS output		4	4
VCC		2	2
VCCX		1	1
VCCO0/VCCO3[3]		1	1
VCCO1/VCCO2[3]		1	1
VSS		2	1
MODE0		0	0
MODE1		0	0
MODE2		0	0
JTAGSEL_N		1	1

Note!

- [1] The number of single end/ differential/LVDS I/O includes CLK pins and download pins.
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O; When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously, and the Max. user I/O plus one.
- [3] Pin multiplexing.

Pin Definitions

The location of the pins in the GW1NRF series of Bluetooth FPGA products varies according to the different packages.

Table 2-4 provides a detailed overview of user I/O, multi-function pins, dedicated pins, and other pins.

Table 2-4 Definition of the Pins in the GW1NRF series of Bluetooth FPGA products

Pin Name	I/O	Description
Max. User I/O		
IO[End][Row/Column Number][A/B]	I/O	• [End] indicates the pin location, including L(left) R(right) B(bottom), and T(top) • [Row/Column Number] indicates the pin Row/Column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the Row number of the corresponding CFU. • [A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. These pins can be used as user I/O when the functions are not used.
RECONFIG_N	I, internal weak pull-up	Start new GowinCONFIG mode when low pulse
READY	I/O	• High level indicates the device can be programmed and configured currently • Low level indicates the device cannot be programmed and configured currently
DONE	I/O	• High level indicates successful program and configure • Low level indicates incomplete or failed to program and configure

FASTRD_N /D3	I/O	• In MSPI mode, FASTRD_N is used as Flash access speed port. Low indicates high-speed Flash access mode; high indicates regular Flash access mode. • Data port D3 in CPU mode
MCLK /D4	I/O	Clock output MCLK in MSPI mode Data port D4 in CPU mode
MCS_N /D5	I/O	Enable signal MCS_N in MSPI mode, active-low Data port D5 in CPU mode
MI /D7	I/O	MISO in MSPI mode: Master data input/Slave data output Data port D7 in CPU mode
MO /D6	I/O	MISO in MSPI mode: Master data output/Slave data input Data port D6 in CPU mode
SSPI_CS_N/D0	I/O	Enable signal SSPI_CS_N in SSPI mod,

Pin Name	I/O	Description
		active-low, Internal Weak Pull Up Data port D0 in CPU mode
SO /D1	I/O	• MISO in MSPI mode: Master data input/Slave data output • Data port D1 in CPU mode
SI /D2	I/O	• MISO in MSPI mode: Master data output/Slave data input • Data port D2 in CPU mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode, which needs to be connected with 4.7 K drop-down resistance on PCB
TDI	I, internal weak pull-up	Serial data input in JTAG mode
TDO	O	Serial data output in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Select signal in JTAG mode, active-low
SCLK	I	Clock input in SSPI, SERIAL, and CPU mode
DIN	I, internal weak pull-up	Input data in SERIAL mode

DOUT	O	Output data in SERIAL mode
CLKHOLD_N	I, internal weak pull-up	High level, SCLK will be connected internally in SSPI mode or CPU mode Low level, SCLK will be disconnected from SSPI mode or CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode
GCLKT_[x]	I	Global clock input pin, T(True), [x]: global clock No.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x]: global clock No.[1]
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pins, T(True)
LPLL_C_fb/RPLL_C_fb	I	Left/Right PLL feedback input pins, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin.
Other Pins		
NC	NA	Reserved.
VSS	NA	Ground pins
VCC	NA	Power supply pins for internal core logic.
VCCO#	NA	Power supply pins for the I/O voltage of I/O BANK#.

Pin Name	I/O	Description
VCCX	NA	Power supply pins for auxiliary voltage.

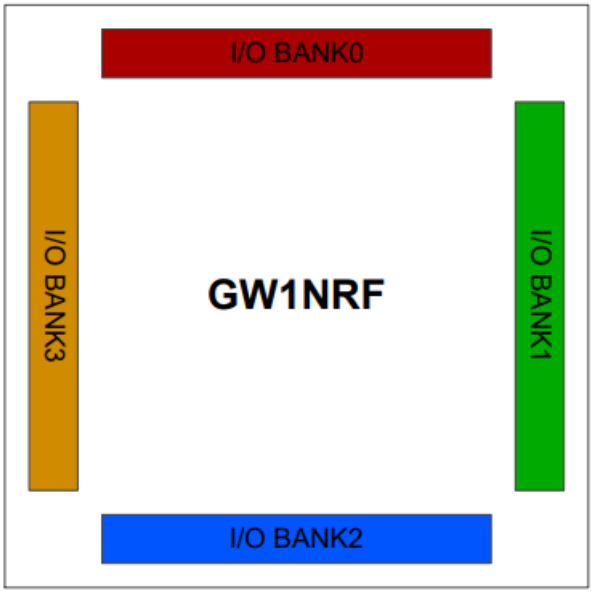
Note!

When the input is single-ended, GCLKC_[x] pin is not a global clock.

6 I/O BANK Introduction

There are four I/O Banks in the GW1NRF series of FPGA products. The I/O BANK Distribution of the GW1NRF series of Bluetooth FPGA products is as shown in Figure 2-1.

Figure 2-1 GW1NRF series of Bluetooth FPGA products I/O Bank Distribution



- This manual provides an overview of the distribution view of the pins in the GW1NRF series of Bluetooth FPGA products. The four I/O Banks that form the GW1NRF series of
- Bluetooth FPGA products are marked with four different colors.

Various symbols are used for the user I/O, power, and ground. The various symbols and colors used for the various pins are defined as follows:

-  ” denotes the I/O in BANK0. The filling color changes with the BANK;
-  denotes the I/O in BANK1. The filling color changes with the BANK;
-  ” denotes the I/O in BANK2. The filling color changes with the BANK;
- ”  ” denotes the I/O in BANK3. The filling color changes with the BANK;
- ”  ” denotes VCC, VCCX, and VCCO. The filling color does not change;
- ”  ” denotes VSS, the filling color does not change;
- ”  ” denotes NC;

- “  ” denotes BLE, the filling color does not change

View of Pin Distribution

View of GW1NRF-4B Pins Distribution

View of QN48 Pins Distribution

Figure 3-1 View of GW1NRF-4B QN48 Pins Distribution (Top View)

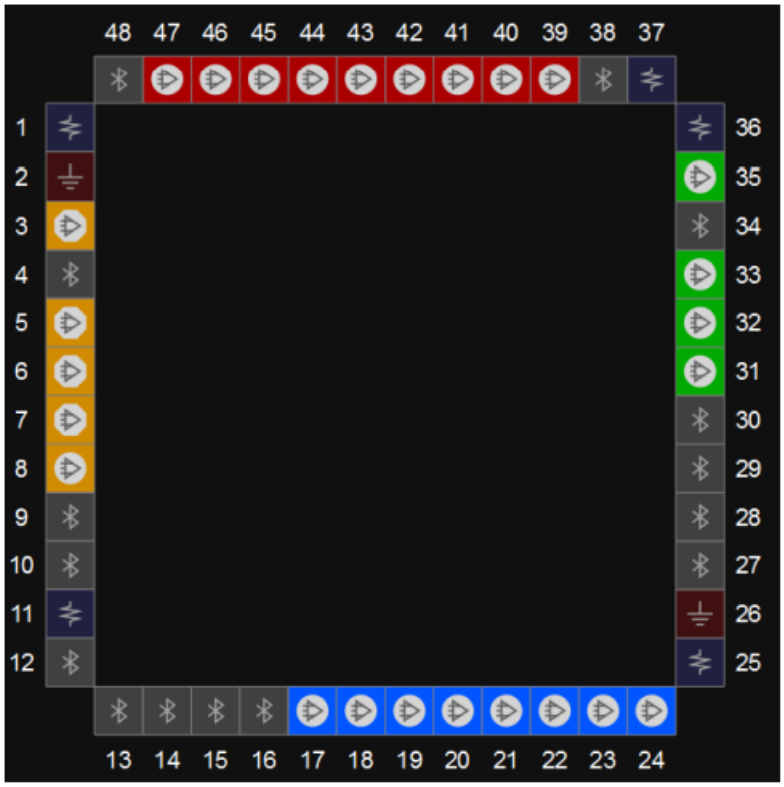


Table 3-1 Other pins in GW1NRF-4B QN48

VCC	11,37
VCCX	36
VCCO0/VCCO3	1
VCCO1/VCCO2	25
VSS	26,2

View of QN48E Pins Distribution

Figure 3-2 View of GW1NRF-4B QN48E Pins Distribution (Top View)

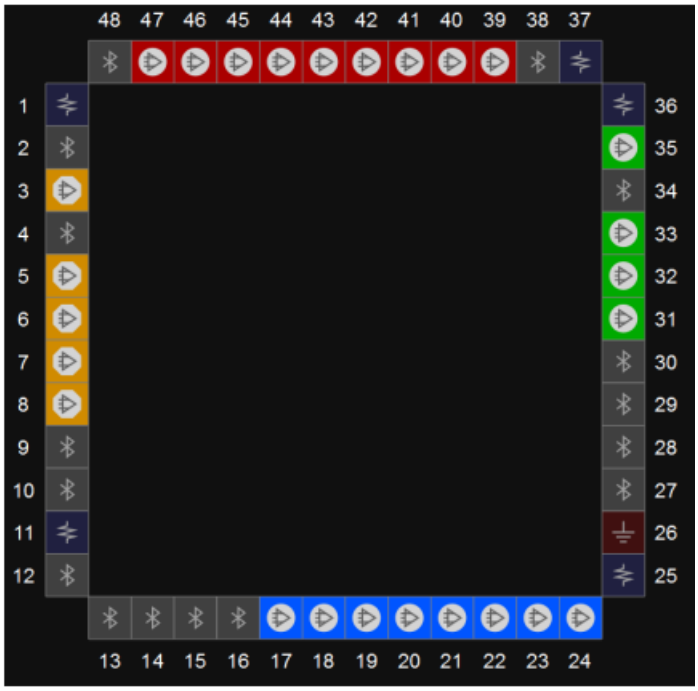


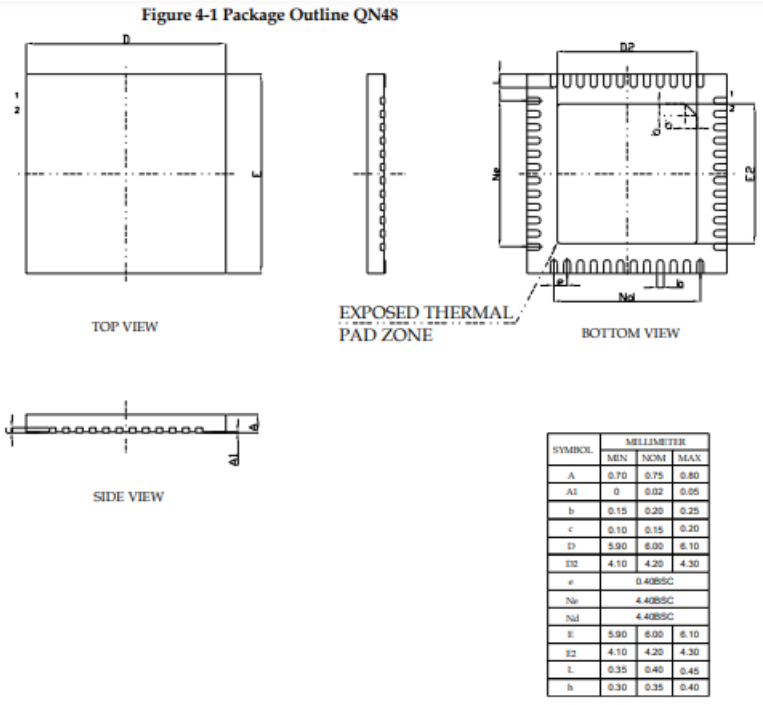
Table 3-2 Other pins in GW1NRF-4B QN48E

VCC	11,37
VCCX	36
VCCO0/VCCO3	1
VCCO1/VCCO2	25
VSS	26

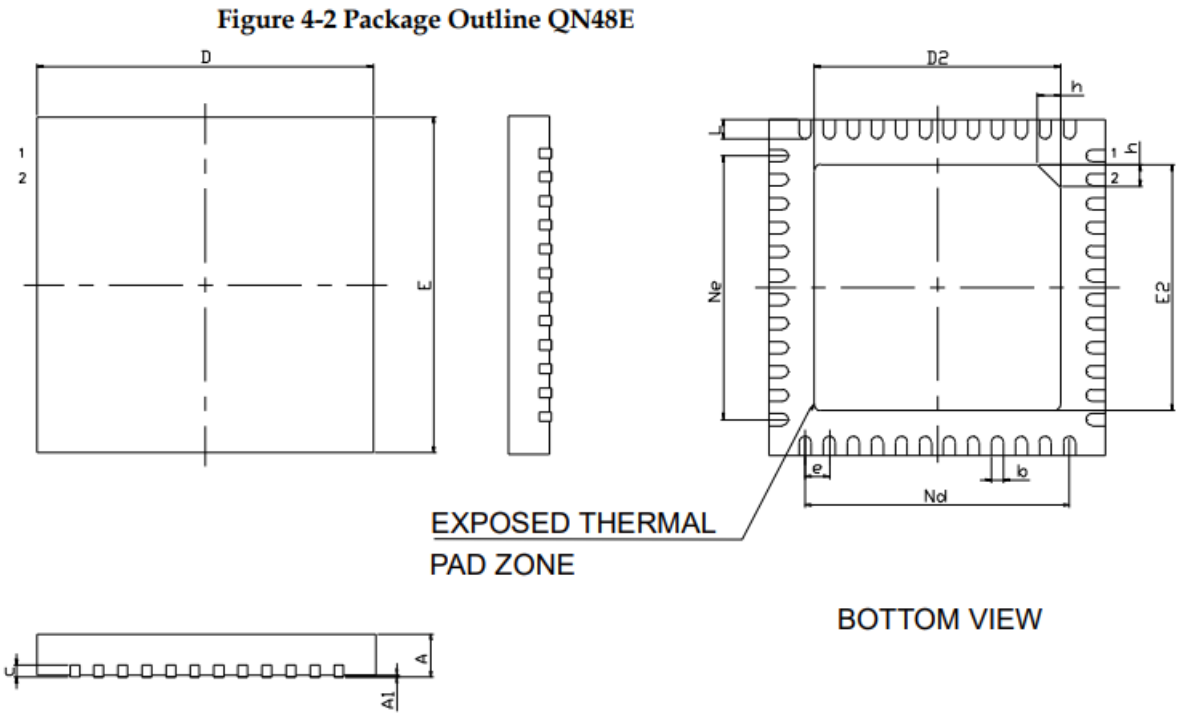
Package Diagrams

QN48 Package Outline (6mm x 6mm)

Figure 4-1 Package Outline QN48



QN48E Package Outline (6mm x 6mm)
Figure 4-2 Package Outline QN48E



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0 8.5	0.85
A1		0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D 2	4.10	4.20	4.30
e	0.40 BSC		
Ne	4.40BSC		
N d	4.40BSC		
E	5.90	6.00	6.10
E 2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Documents / Resources

	**GOWIN GW1NRF Series Bluetooth FPGA Products Package and Pinout** [pdf] User Guide GW1NRF Series Bluetooth FPGA Products Package and Pinout, GW1NRF Series, Bluetooth FPGA Products Package and Pinout, FPGA Products Package and Pinout, Products Package and Pinout, Package and Pinout, Pinout

References

- **Home|GOWIN Semiconductor**
- **Home|GOWIN Semiconductor**
- **User Manual**