GOWIN FP Comp IP and Reference Design User Guide

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GOWIN FP Comp IP and Reference Design User Guide

Gowin FP Comp IP
User Guide

IPUG1049-1.0E, 05/09/2024

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Revision History

Date	Version	Description
05/09/2024	1.0E	Initial version published.

About This Guide

Purpose

The purpose of Gowin FP Comp IP User Guide is to help you learn the features and usage of Gowin FP Comp IP by providing the descriptions of functions, ports, timing, GUI and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software V1.9.9 Beta-3. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at **www.gowinsemi.com**:

- **DS100, GW1N series of FPGA Products Data Sheet**
- **DS117, GW1NR series of FPGA Products Data Sheet**
- **DS821, GW1NS series of FPGA Products Data Sheet**
- **DS861, GW1NSR series of FPGA Products Data Sheet**
- **DS102, GW2A series of FPGA Products Data Sheet**
- **DS226, GW2AR series of FPGA Products Data Sheet**
- **DS971, GW2AN-18X & 9X Data Sheet**

- DS976, GW2AN-55 Data Sheet
- SUG100, Gowin Software User Guide

Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ALU	Arithmetic Logical Unit
LUT	Look-up Table
IP	Intellectual Property

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

Overview

Gowin FP Comp IP is designed to realize integer addition and division operations with less logic resources. Gowin FP Comp IP can compare two single-precision floating-point numbers. This IP supports optional output ports such as A=B, A!=B, A>B, A>=B, A<B, A<=B, and NaN (Not a Number).

Table 2-1 Gowin FP Comp IP Overview

Gowin FP Comp IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.Beta-3 and above)

Note!

For the devices supported, you can click **here** to get the information.

Features

Supports optional output ports such as A=B, A!=B, A>B, A>=B, A<B, A<=B, and NaN (Not a Number).

Max. Frequency

The max. frequency of Gowin FP Comp IP is mainly determined by speed grade of the selected devices.

Latency

The latency of Gowin FP Comp IP is determined by the configuration parameters.

Resource Utilization

Gowin FP Comp IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW2A 55 series of FPGA as an instance, the resource utilization is as shown in Table 2-2. For the resource utilization of other devices, please refer to later release information.

Table 2-2 Resource Utilization

Device	Speed Grade	Resource Name	Resource Utilization
GW2A-55	C8/I7	Registers	5
		LUTs	110
		ALUs	38
		I/O Buffer	13

Functional Description

Gowin FP Comp IP can implement the comparison of two single precision floating-point numbers. Users can configure parameters according to their requirements when generating this module.

Port List

The details of Gowin FP Comp IP IO port are shown in Table 4-1, and the port diagram is as shown in Figure 4-1.

Figure 4-1 Gowin FP Comp IP IO Port Diagram

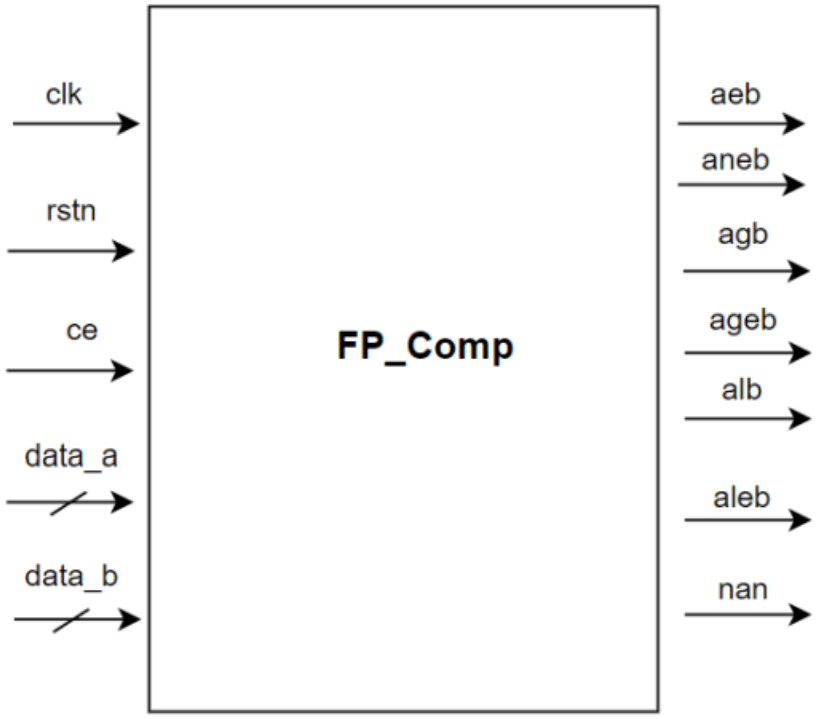


Table 4-1 Gowin FP Comp IP IO Port List

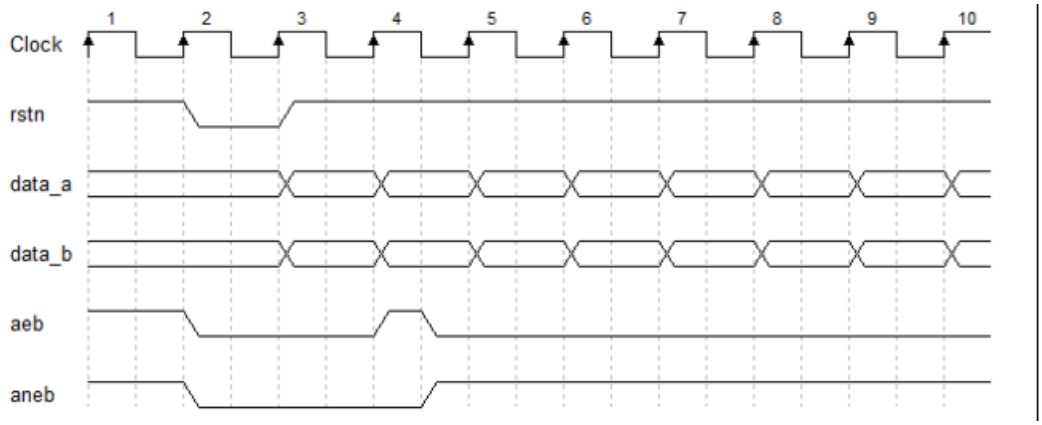
Signal	I/O	Description
clk	Input	Clock signal
rstn	Input	Reset signal, active-low
ce	Input	Clock enable signal, active-high (optional)
data_a	Input	Input a
data_b	Input	Input b
aeb	Output	a=b (optional)
aneb	Output	a!=b (optional)

Signal	I/O	Description
agb	Output	a> b (optional)
ageb	Output	a> = b (optional)
alb	Output	a< b (optional)
aleb	Output	a< = b (optional)
unorder	Output	NaN (optional)
result	Output	Output result

Timing Description

This section describes the timing of Gowin FP Comp IP. The timing of Gowin FP Comp IP is shown in Figure 5-1.

Figure 5-1 Gowin FP Comp IP Signal Timing



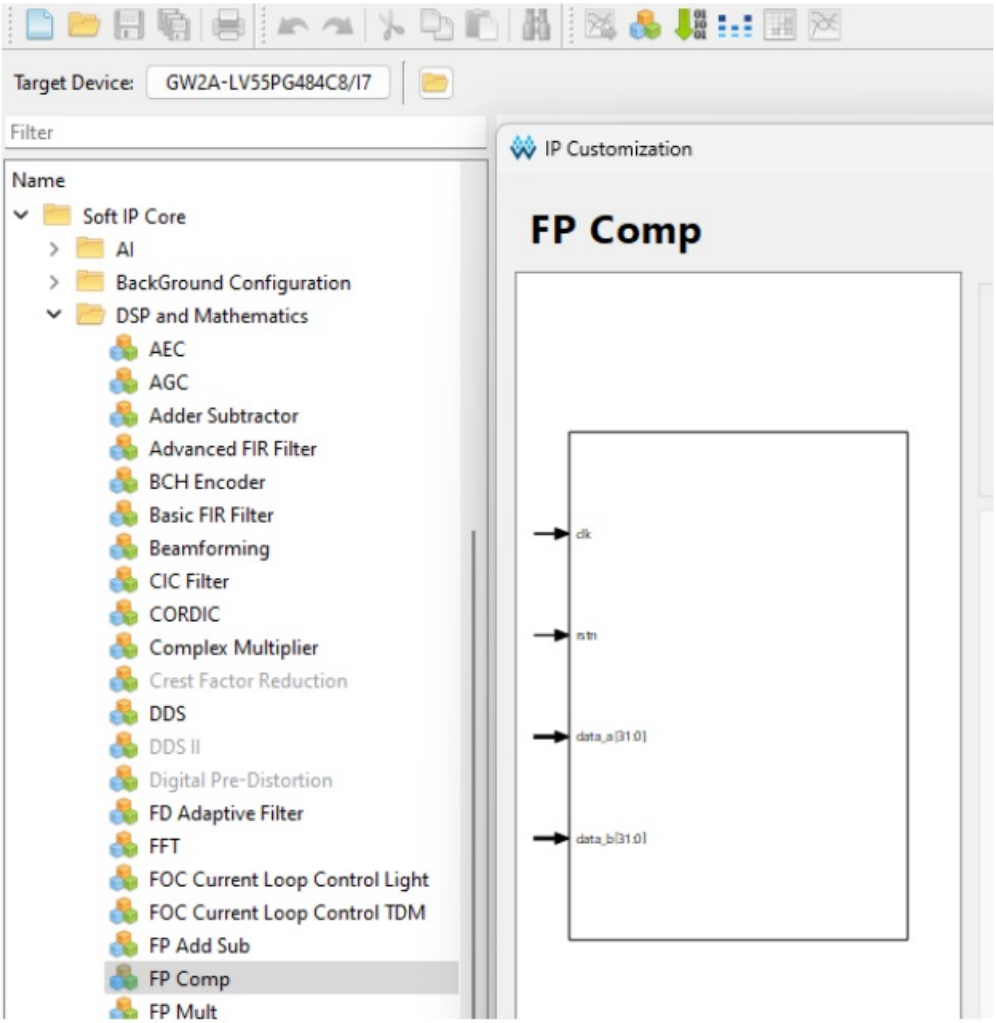
As shown in the figure above, after inputting two single-precision floating-point data, the result of comparison is output with a delay of one clock cycle.

GUI Configuration

IP Generation

Click “Tools > IP Core Generator > DSP and Mathematics” to call and configure FP Comp; toolbar icon is also available to open the IP as shown in Figure 6-1.

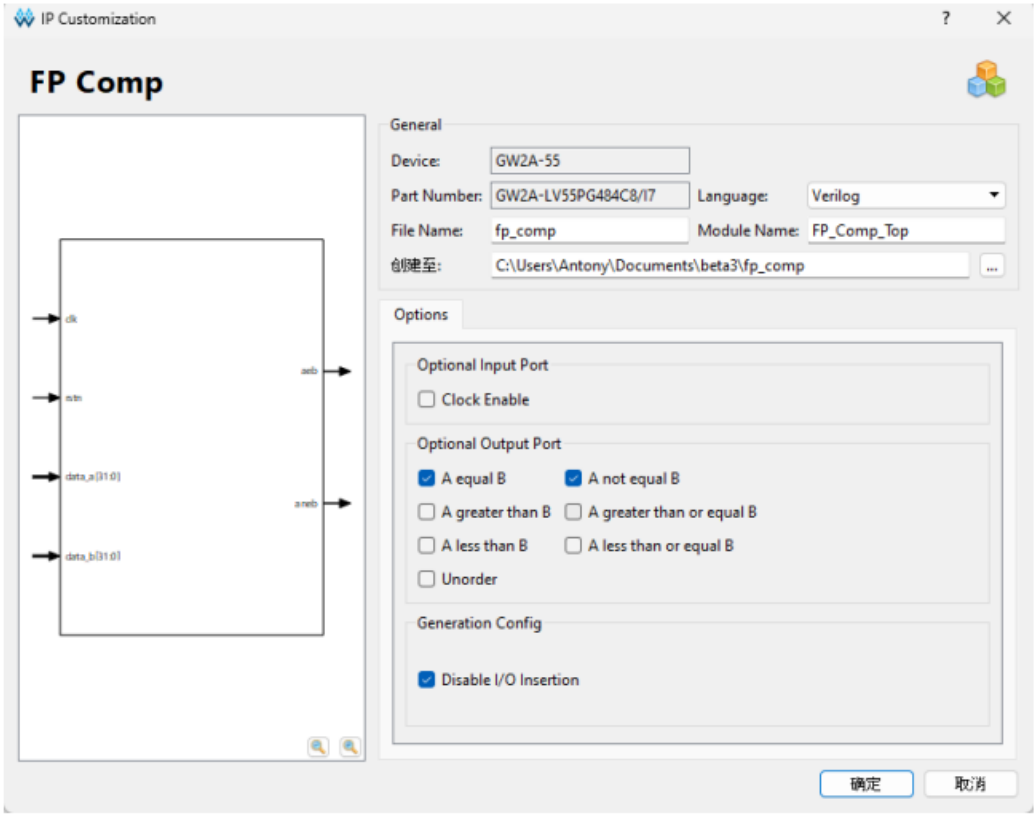
Figure 6-1 Open GUI Via Icon



Configuration Interface

Gowin FP Comp IP configuration interface is shown in Figure 6-2.

Figure 6-2 Gowin FP IP Configuration Interface



This manual takes GW2A-55 chip and GW2A-LV55PG484C8/I7 part number as an example.

- You can configure the path of generated IP core folder in the “Create In” text box.
- You can configure the generated IP file name in the “File Name” text box.
- You can configure the generated IP module name in the “Module Name” text box.

Reference Design

Please see Gowin FP Comp IP **Reference Design** for details at Gowinsemi website.

File Delivery

The delivery file of Gowin FP Comp IP includes documentation and reference design.

Documentation

The folder mainly contains the user guide in PDF version.

Table 8-1 Document List

Name	Description
IPUG1049 Gowin FP Comp IP User Guide	Gowin FP Comp IP User Guide, namely this one

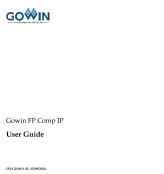
Reference Design

Gowin FP Comp IP RefDesign folder contains the netlist file, user reference design, constraints file, top-level file, and project file, etc.

Table 8-2 Gowin FP Comp IP RefDesign Folder Content List

Name	Description
top.v	The top module of reference design
FP_Comp.cst	Project physical constraints file
FP_Comp.sdc	Project timing constraints file
FP_Comp.rao	Online logic analyzer file
fp_comp.v	Generate FP Comp IP top-level file, encrypted

Documents / Resources

	GOWIN FP Comp IP and Reference Design [pdf] User Guide IPUG1049-1.0E, FP Comp IP and Reference Design, Comp IP and Reference Design, IP and Reference Design, Reference Design, Design

References

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