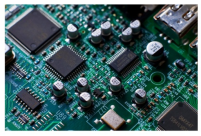
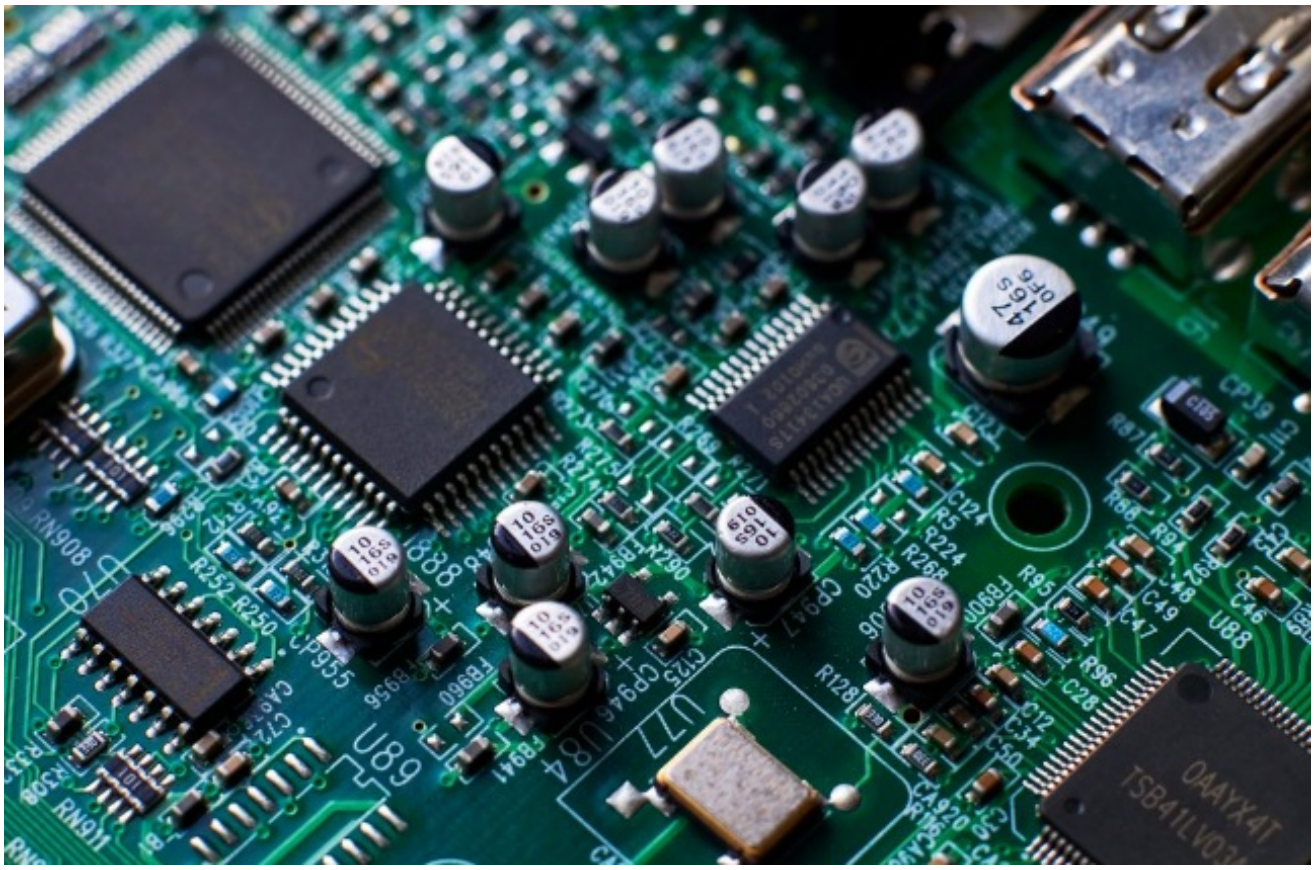


GOWIN Arora V PCI Express Controller IP User Guide

Contents

GOWIN Arora V PCI Express Controller IP



Product Information

The Arora PCI Express Controller IP is a product developed by Guangdong Gowin Semiconductor Corporation. It is a registered trademark in China, the U.S. Patent and Trademark Office, and other countries. The product is designed to provide users with a functional and feature-rich solution for PCI Express connectivity.
GOWINSEMI assumes no liability and provides no warranty for any damage incurred to hardware, software, data, or property resulting from the usage of the materials or intellectual property, except as outlined in the GOWINSEMI Terms and Conditions of Sale.
The user guide provides comprehensive information about the Arora PCI Express Controller IP, including its features, functional description, configuration, and usage.

Product Usage Instructions

To use the Arora PCI Express Controller IP effectively, follow these instructions

Step 1: Obtain the User Guide
Visit the GOWINSEMI website (**www.gowinsemi.com**) to access the latest user guides. Look for the user guide titled “Arora PCI Express Controller IP User Guide” to download and refer to it throughout the usage process.

Step 2: Familiarize Yourself with the Features
Read section 2 of the user guide, titled “Overview.” This section provides detailed information about the features of the Arora PCI Express Controller IP. Understanding these features will
help you make the most of the product.

Step 3: Understand the Functional Description
In section 2.2 of the user guide, titled “Functional Description,” you will find a detailed explanation of how the Arora PCI Express Controller IP works. This section will give you insights into the internal structure and operation of the product.

Step 4: Configure the PCI Express Controller

Section 4 of the user guide, titled “PCI Express Controller Configuration and Call,” provides instructions for configuring the Arora PCI Express Controller IP. Follow the steps outlined in subsections 4.1, 4.2, and 4.3 to perform basic configuration, BAR configuration, and function configuration, respectively.

Step 5: Additional Information
If you require detailed information about the PCIe configuration registers, refer to Appendix A of the user guide titled “PCIe Configuration Register Information.”
For any further assistance or clarification, please contact GOWINSEMI for the most up-to-date documentation and any potential updates or corrections.

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Revision History

Date	Version	Description
05/25/2023	1.0E	Initial version published.

Purpose
Arora V PCI Express Controller IP User Guide mainly functional features, structure, port descriptions, configuration calls, etc. It is designed to help users quickly understand the features, characteristics and usage of Arora V PCI Express Controller IP.

Related Documents
The latest user guides are available on the GOWINSEMI website. You can find the related documents at **www.gowinsemi.com**

- DS981, GW5AT series of FPGA Products Data Sheet
- DS1103, GW5A series of FPGA Products Data Sheet
- DS1104, GW5AST series of FPGA Products Data Sheet

Terminology and Abbreviations
The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
PCIe	Peripheral Component Interconnect Express
BAR	Base Address Register
TLP	Transaction Layer Packet
LTSSM	Link Training and Status State Machine
MSI	Message Signaled Interrupt
MAC	Media Access Control

Support and Feedback
Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

- **Website:** www.gowinsemi.com
- **E-mail** support@gowinsemi.com
- **Tel +86** 755 8262 0391

Overview

Arora V FPGA products include the PCIe integrated interface module, which is compliant with the PCIe Gen2 (5GT/s) specification as defined by the PCI Express Base Specification, V2.1, and can support x1, x2, x4, and x8 lanes.
PCI Express protocol enables custom FPGA-to-FPGA communication and attaches ASSP endpoint devices, such as Ethernet Controllers or Fiber Channel HBAs (Host Bus Adapter,HBA), to the FPGA. The PCIe controller module provides a high performance and low cost solution.

Features
The main features of Gowin PCI Express Controller IP are as follows

- Compliant to the PCI Express Base Specification 2.0
- Supports x1, x2, x4, x8 lanes
- Supports End Point
- Supports Gen1 (2.5Gb/s), Gen2 (5Gb/s)
- Up to six BARs (Base Address Register), resizable
- Supports up to 4KB data payload transfer
- Supports Autonomous link speed/width change
- Supports advanced configuration options, Advanced Error Reporting (AER), and End-to-End Cyclic Redundancy Check (ECRC)
- **Configurable parameters**: channel width, maximum payload size, FPGA logical interface speeds, reference clock frequency, base address register decoding and filtering, etc.

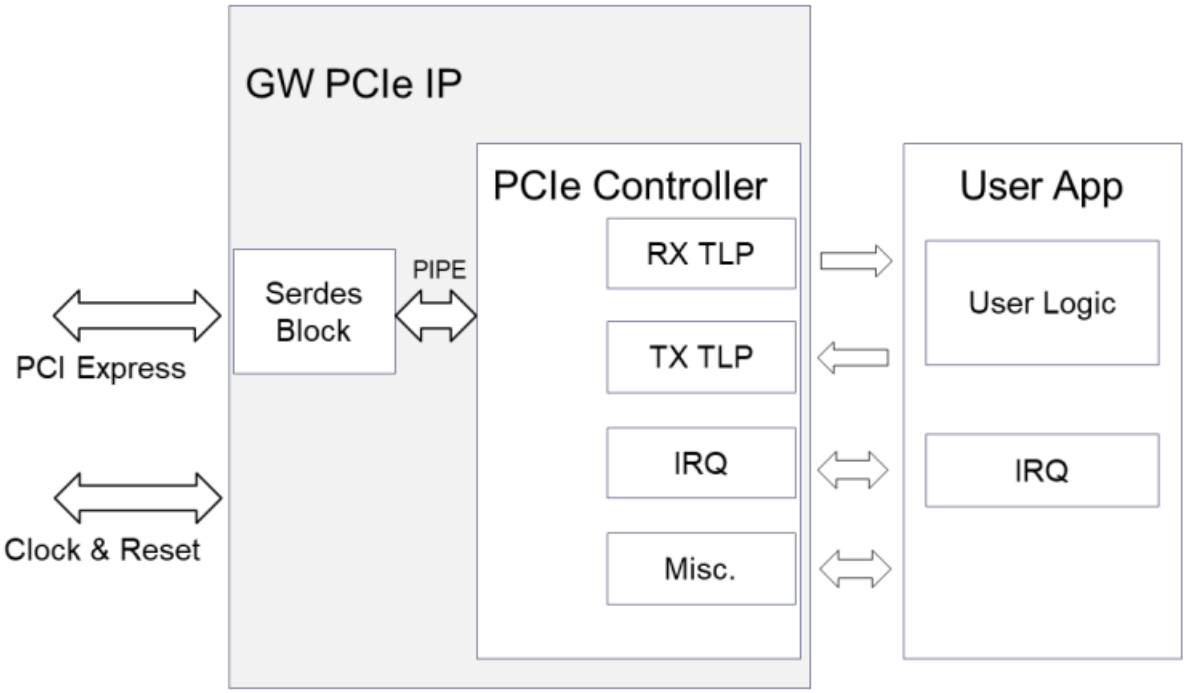
Functional Description

- The basic functions of the PCIe controller integrated in the Gowin devices are shown in Figure 2-1.
- The controller uses GOWIN's 12G Serdes module as the physical layer to connect with external PCIe hosts or

devices for data communication.

- The PCIe controller provides the full functionality of the transaction Layer, data link layer and MAC.
- For the user logic, the PCIe controller provides the TLP receive and transmit interfaces for data and common command transfers.

The controller supports interrupt modes such as MSI. Figure 2-1 PCIe Controller Function Block Diagram



PCI Express Controller

This chapter mainly introduces the ports of the PCIe controller module. According to the practical applications, this chapter divides the controller ports into physical interfaces, transmission interfaces, interrupt interfaces, and configuration interfaces according to their functions.

Physical Layer Interface

Depending on the number of Lanes used by the PCIe controller, x1, x2, x4, you need to choose the specified IO pins and the fixed lane sequence design according to Pinout. PCIE uses Q0 Lane0 or Q1 Lane0 for X1 pin. Q0 (or Q1) Ref0 is the reference clock input and the reference clock frequency is 100MHz.

Clock and Reset

Table 3-1 Gowin PCI Express Controller IP Clock and Reset

Port	I/O	Description
pcie_tl_clk_i	input	PCIe TLP user clocks
pcie_tl_rst_i	input	PCIe TLP user reset signal

Transaction Layer Interface

TLP Receive Interface

Table 3-2 Gowin PCI Express Controller IP Receive Interface

Port	I/O	Description
pcie_tl_rx_sop_o	output	Receive the TLP Start packet, marking the first data packet of the TLP.
pcie_tl_rx_eop_o	output	Receive the TLP End packet, marking the last data packet of the TLP.
pcie_tl_rx_data_o [255:0]	output	Receive TLP data, 256 bit width by default
pcie_tl_rx_valid_o [7:0]	output	The validity flag of receiving the TLP data, each bit flag corresponds to whether the Dwords are valid or not. Bit 7 corresponds to pcie_tl_rx_data[255:224] and Bit 0 corresponds to pcie_tl_rx_data[31:0].
pcie_tl_rx_bardec_o [5:0]	output	Receive the target BAR decoding signal of the TLP, indicating the functional channel corresponding to the received data, as shown in Table Table 3-3.
pcie_tl_rx_err_o[7:0]	output	Receive data error signal. Bit 0: ECRC Error. **Bit 1**: Invalid TLP, including TLP packet with wrong identification bits in RX buffer TLP payload size does not match the actual data received **Bit 2**: RX buffer read error Bit 3: RX Config data packet **Bit 4**: Unsupported TLP formats Bit 5 ACS Violation **Bits 7:6** reserved
pcie_tl_rx_wait_i	input	Receive wait signal, indicating that the RX buffer is not ready to receive data.
pcie_tl_rx_masknp_i	input	The mask signal of Non-posted TLP packet If the signal is set high, enables the controller to stop receiving the subsequent non-posted TLPs after the current TLP transmission is finished.

Table 3-3 The Function Channel Corresponding to The Received Data

Bit	BAR
0	BAR0
1	BAR1*
2	BAR2
3	BAR3*
4	BAR4
5	BAR5*

Note!
*, Bit1 is invalid when BAR0 is set to 64bit, Bit3 is invalid when BAR2 is set to 64bit, and Bit5 is invalid when

BAR4 is set to 64bit.

Receive Interface Timing

Figure 3-1 shows the TLP receive timing. The figure shows the TLP data reception timing for a Header length of 4DWORD, a payload length of 15DWORD, and a target BAR0. The pcie_tl_rx_wait signal is set to 1 during reception.

Figure 3-1 TLP Receiving Timing

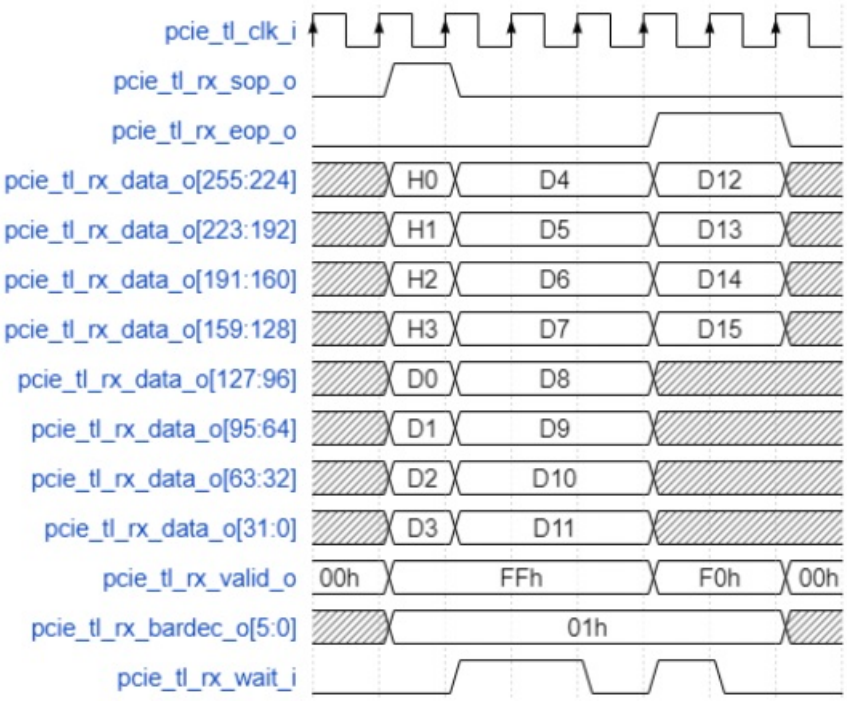
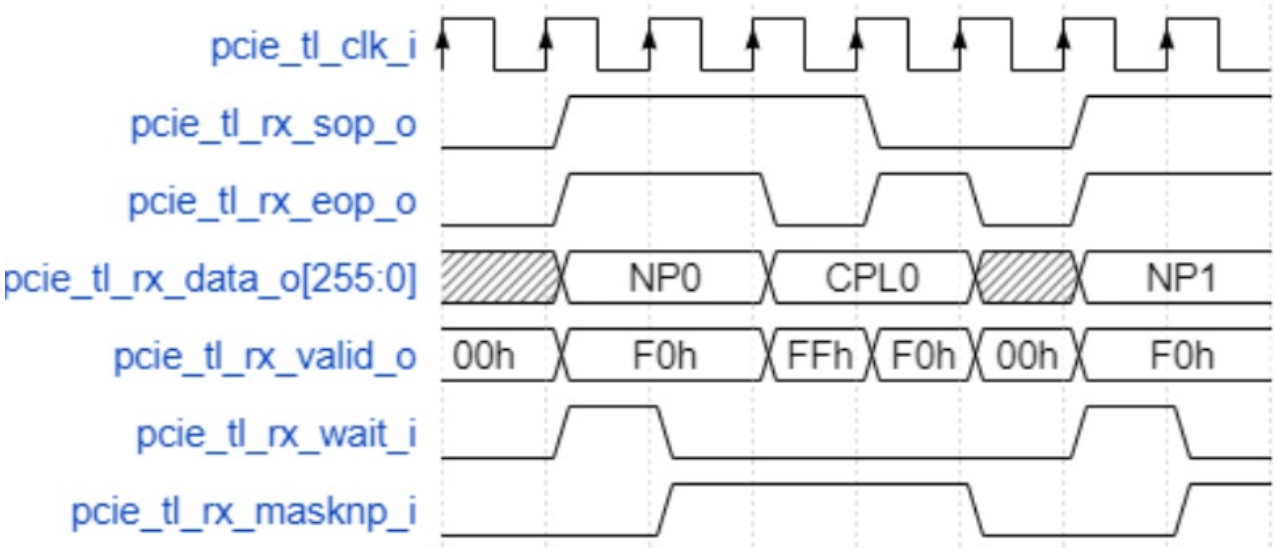


Figure 3-2 is the Receive Timing of the Non-posted TLP packet. During TLP reception, pcie_tl_rx_wait_i is set to 1 for one clock cycle. During the reception of the first TLP packet, pcie_tl_rx_masknp_i is set to 1, preventing the controller from receiving the subsequent non-posted TLP packets and only receiving the output completion packet (Completion TLP). The controller restarts receiving Non-posted TLP only after pcie_tl_rx_masknp_i is pulled down.

Figure 3-2 Receive Timing of Non-posted TLP



TLP Transmit Interface

Table 3-4 Transmit Interface of Gowin PCI Express Controller IP Controller

Port	I/O	Description
pcie_tl_tx_sop_i	input	Transmitting the TLP Start packet, marking the first data packet of t he TLP packet.
pcie_tl_tx_eop_i	input	Transmitting the TLP End packet, marking the last data packet of th e TLP packet.
pcie_tl_tx_data_i[255:0]	input	Transmit TLP Data.
pcie_tl_tx_valid_i[7:0]	input	A signal to indicate whether the TLP data transmission is valid or n ot. Each bit indicates whether the Dwords are valid or not. Bit 7 corr esponds to pcie_tl_rx_data[255:224] and Bit 0 corresponds to pcie_tl_rx_data[31:0].
pcie_tl_tx_wait_o	output	Transmitting wait signal, indicating that the TX buffer is not ready to transmit data.

Transmit Interface Timing

Figure 3-3, Figure 3-4, and Figure 3-5 are the control timing when pcie_tl_tx_wait_o is set high during the TLP transmission. When the controller does not have enough TLP transmit space, pcie_tl_tx_wait_o is pulled up. A valid TLP packet transmission needs to be recognized by the controller when the pcie_tl_tx_wait_o signal is 0.

Figure 3-3 pcie_tl_tx_wait_i and Transmitting Timing 1

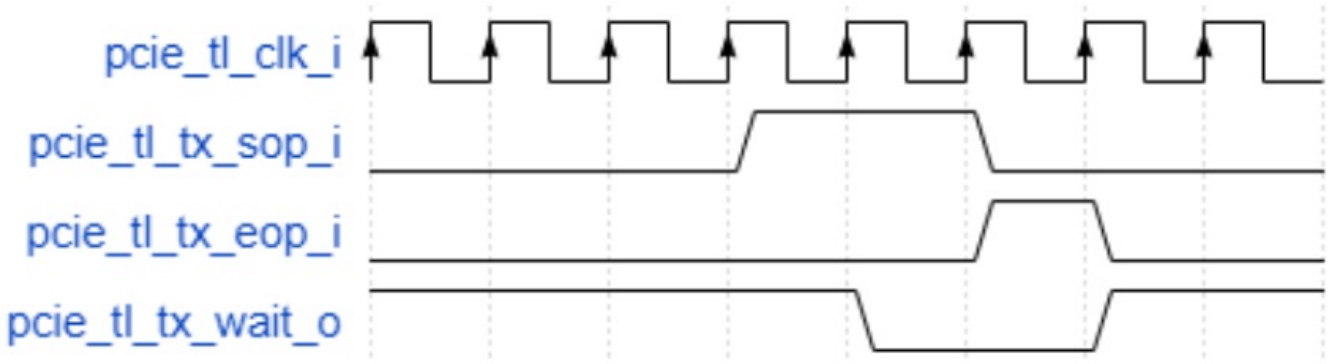


Figure 3-4 pcie_tl_tx_wait_i and Transmitting Timing 2

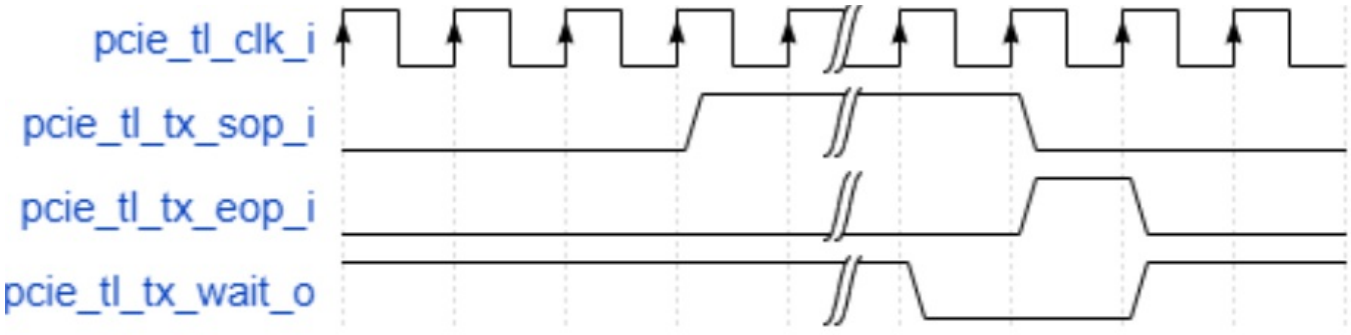


Figure 3-5 pcie_tl_tx_wait_i and Transmitting Timing 3

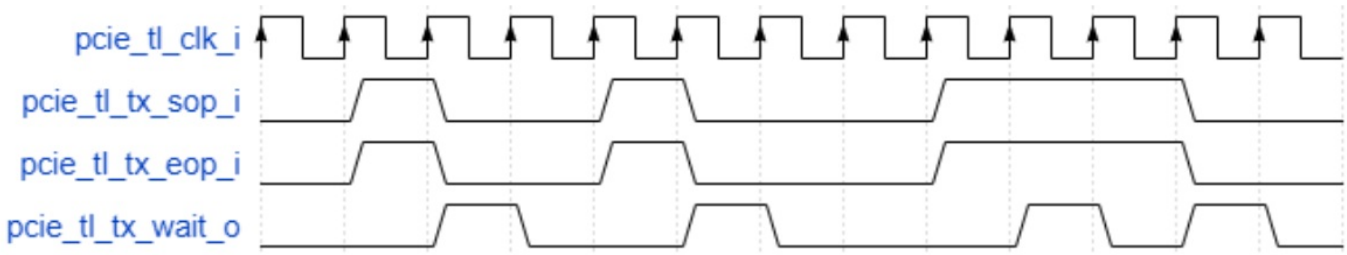
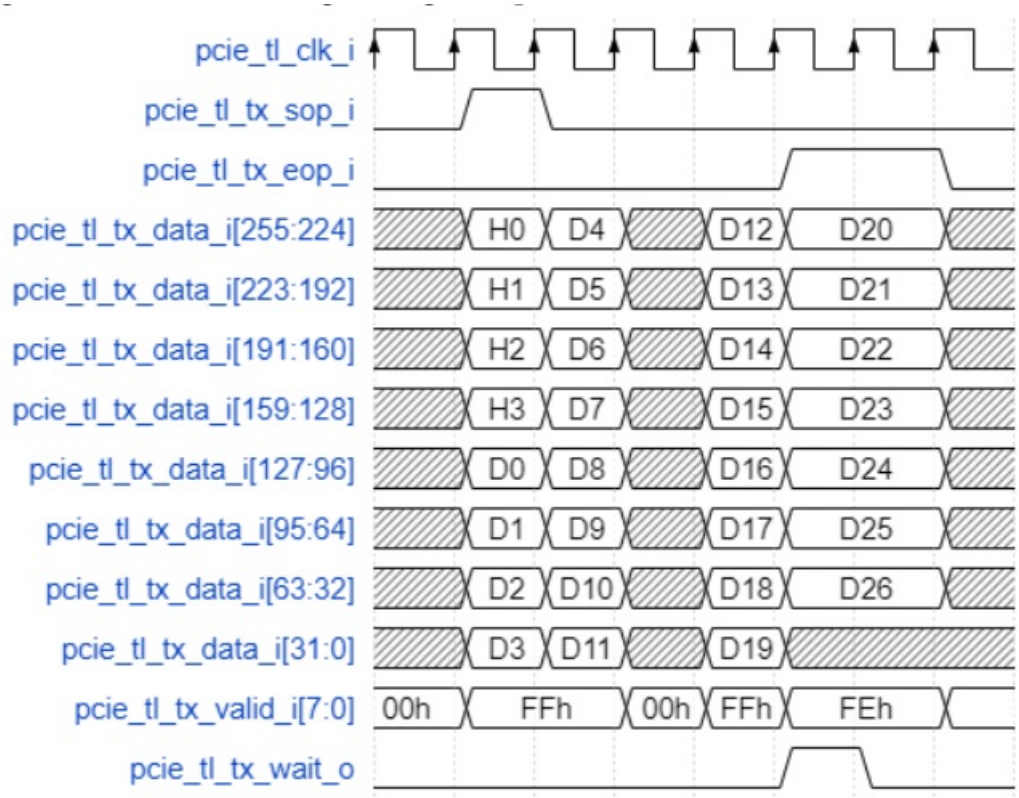


Figure 3-6 shows the complete timing reference for TLP Transmitting. The figure below shows the transmitting control timing for a Header length of 4DW and a payload length of 27DW. The controller identifies the valid transmit data by pcie_tl_tx_valid_i the feedback signal pcie_tl_tx_wait_o.

Figure 3-6 TLP Transmitting Timing Examples



Interrupt Interface

Table 3-5 Gowin PCIe Controller IP Controller Interrupt Interface

Parameter	I/O	Description
pcie_tl_int_status_i	input	Physical function interrupt status
pcie_tl_int_req_i	input	Interrupt request signal. A valid interrupt request is issued by setting one clock cycle high. The user side must wait for the pcie_tl_int_ack signal to be set high before issuing the next interrupt request.
pcie_tl_int_msinum_i[4:0]	input	The number of MSI interrupts. Indicates the number of MSI numbers corresponding to the interrupt request. If the MSI interrupt is not enabled, this signal needs to be set to 0.
pcie_tl_int_ack_o	output	The response of interrupt signal Indicates that a valid

Parameter	I/O	Description
		pcie_tl_int_req request was received by the controller and sent successfully.

Interrupt Interface Timing

See Figure 3-7 for the interrupt interface timing. When enabling the interrupt of the physical function, the user pulls up the pcie_tl_int_status_i signal and issues the pcie_tl_int_req_i request while simultaneously issuing pcie_tl_int_msinum_i. After the first interrupt request is sent and the response pcie_tl_int_ack_o is received, the second interrupt request can continue to be sent. When all interrupt requests required by the application have been sent and responded to, the pcie_tl_int_status_i signal is pulled low and the interrupt is cleared.

Figure 3-7 Single Interrupt Control Timing

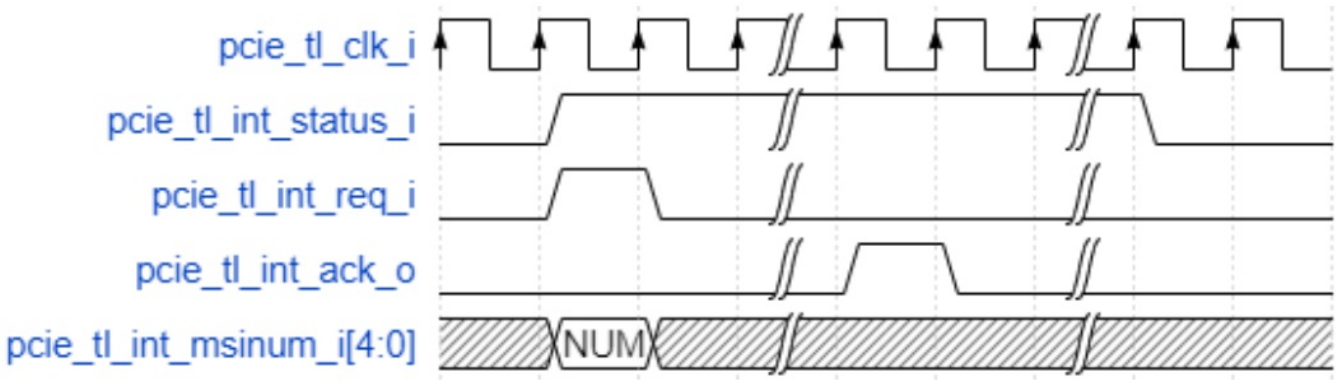
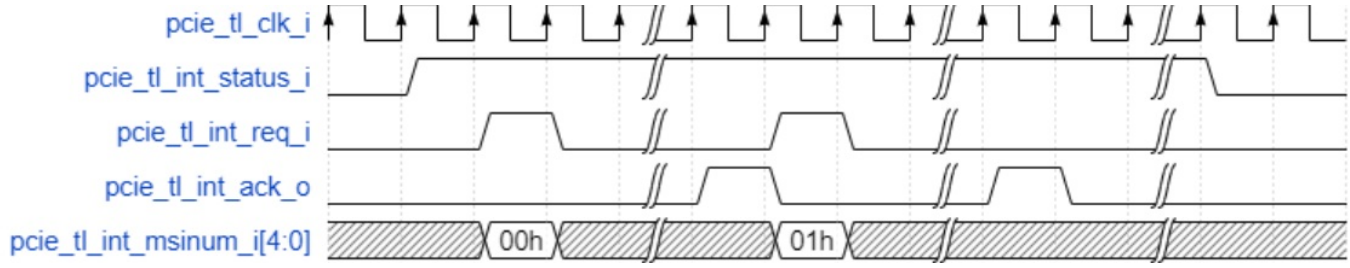


Figure 3-8 Multiple Interrupt Control Timing



Controller Status Interface

Table 3-6 Gowin PCIe Controller IP Controller Status Interface

Parameter	I/O	Description
ltssm_o[4:0]	output	LTSSM status • **00h**: detect.quiet • **01h**: detect.active • **02h**: polling.active • **03h**: **polling.compliance** • **04h**: polling.configuration • **05h**: config.linkwidthstart • **06h**: config.linkwidthaccept • **07h**: config.lanenumwait • **08h**: config.lanenumaccept • **09h**: **config.complete** • **0Ah**: config.idle • **0Bh**: recovery.receiverlock • **0Ch**: recovery.equalization • **0Dh**: recovery.speed • **0Eh**: recovery.receiverconfig • **0Fh**: recovery.idle • **10h**: L0 • **11h**: L0s • **12h**: L1.entry • **13h**: L1.idle • **14h**: L2.idle/L2.transmitwake • **15h**: reserved • **16h**: disable • **17h**: loopback.entry • **18h**: loopback.active • **19h**: loopback.exit • **1Ah**: hotreset
pcie_tl_tx_data_i[31:0]	output	Posted TLP controls the number of credits sent. **[14:0]**: the number of valid data **credits [26:16]:** the numb er of valid **header credits [31]**: sufficient number of credits to send TLP packets of max payload size
pcie_tl_tx_creditsnp_o[31:0]	output	Non-Posted TLP controls the number of

Parameter	I/O	Description
		credits sent. **[14:0]**: the number of valid data **credits [26:16]**: the number of valid **header credits [31]**: sufficient number of credits to send TLP packets of max payload size
pcie_tl_tx_creditscpl_o[31:0]	output	Completion TLP controls the number of credits sent. **[14:0]**: the number of valid data **credits [26:16]**: the number of valid **header credits [31]**: sufficient number of credits to send TLP packets of max payload size
pcie_tl_cfg_busdev_o[12:0]	output	Bus Number and DeivceNumber information for PCIe devices. [12:5] **Bus Number [4:0]** Device Number

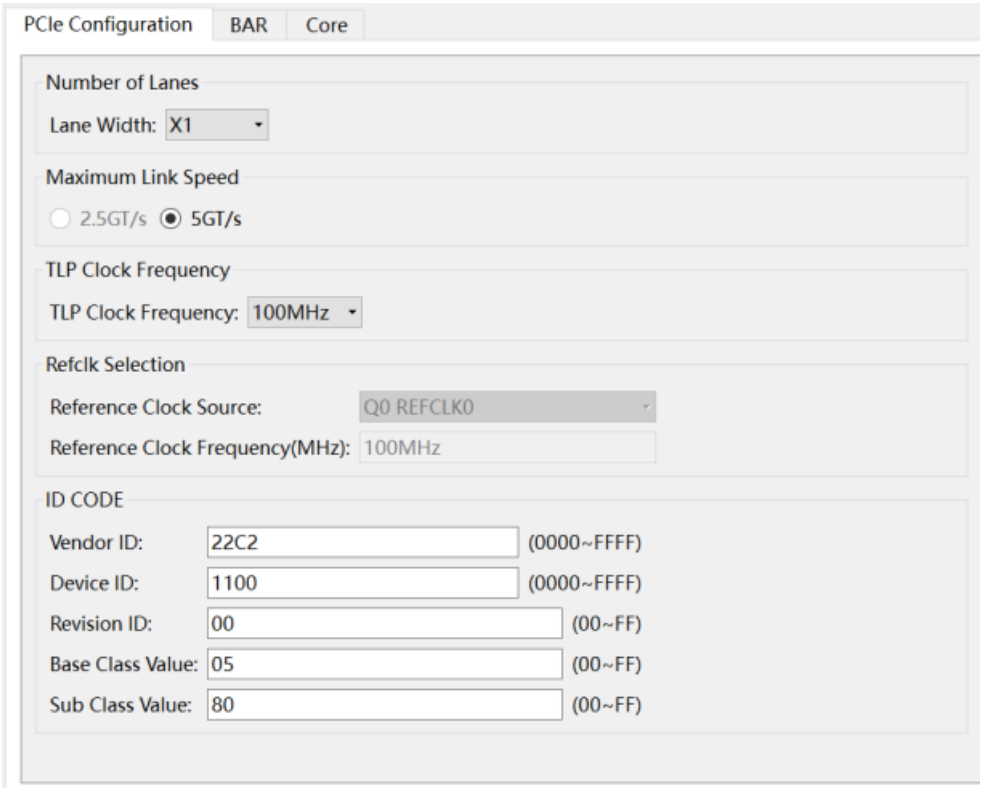
PCI Express Controller Configuration and Call
In “Tools” menu bar of Gowin Software interface, you can start the “IP Core Generator” tool to call and configure the PCI Express Controller.
The PCI Express Controller configuration interface includes the following sections

- Page 1 shows the basic configuration of the PCIe controller, including basic parameters such as operating speed, number of channels, and device ID.
- Page 2 is the BAR configuration for PCIe, you can configure the space size of BAR0-BAR5 used, and the corresponding IO and Memory attributes, etc.
- Page 3 is the interrupt support for PCIe to configure other configurations such as MSI mode.

Basic Configuration of PCI Express Controller
The basic configuration of PCI Express is as shown in Figure 4-1.

- **Lane Width**: The number of lanes that need to be configured for PCIe. You can select x1, x2, x4 from the drop-down list.
- **Maximum Link Speed**: The current configuration is fixed at 5GT/s and supports PCIe 2.0.
- **Reference Clock Frequency**: The configuration is fixed at 100MHz.
- **TLP Clock Frequency**: The user clock used by the TLP layer. The clock source is the user logic input to the PCIe controller. Select the actual configured clock frequency. The drop-down list includes 100MHz/125MHz/150MHz.
- **Vendor ID**: User-defined Vendor ID of PCIe register space, the default value is 22C2h, which is the registered Vendor ID of GOWIN Semiconductor.
- **Device ID**: User-defined.
- **Revision ID**: User-defined.
- **Base Class Value**: User-defined.
- **Sub Class Value**: User-defined.

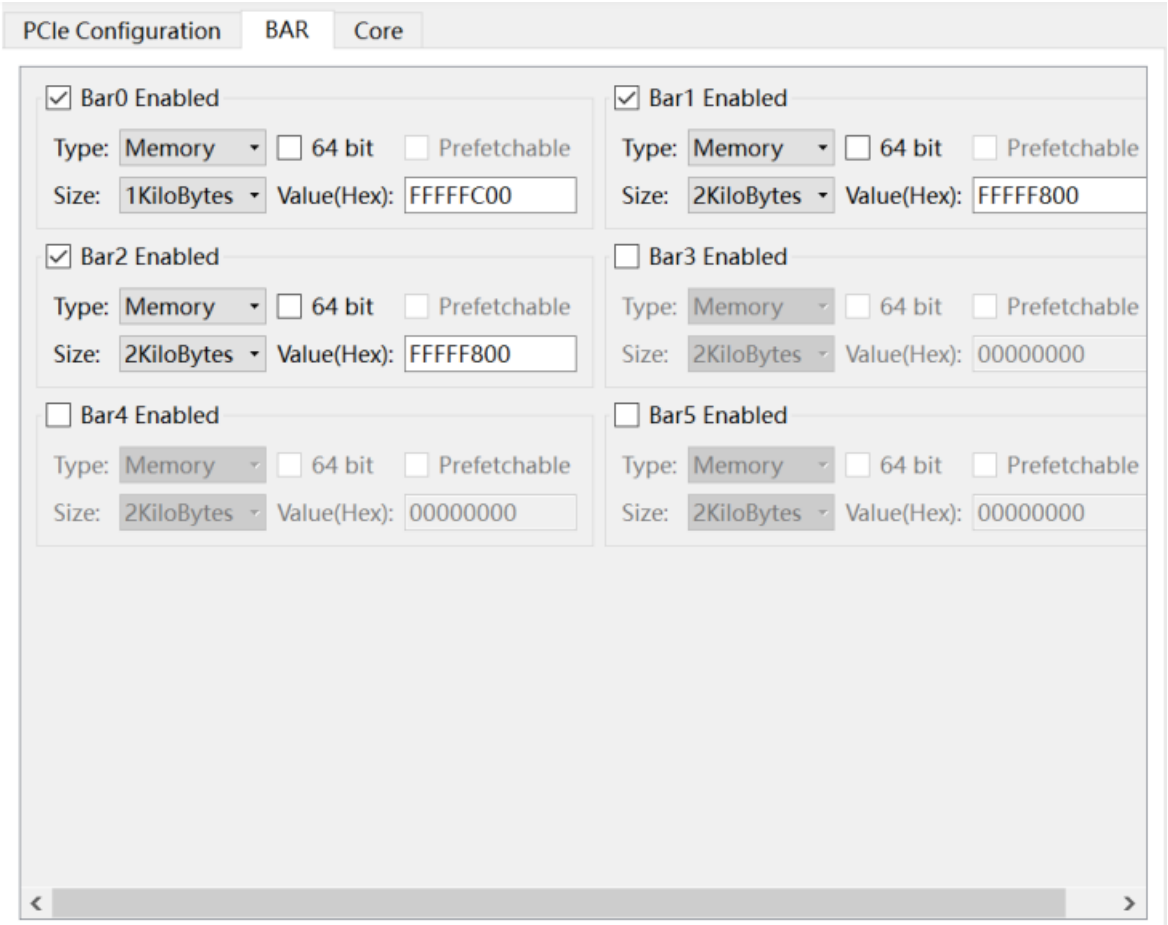
Figure 4-1 Basic Configuration of PCIe Controller



BAR Configuration of PCI Express Controller
Users can configure the application information of BAR space in this page. The PCIe controller supports flexible configuration of BAR0-BAR5.

- **BAR Enable**: Check to enable the BAR space.
- **64 bit**: 64 bit address space is optional, if checked, the nearest BAR space will be occupied at the same time for sharing address space.
- **Prefetchable:** Valid only when 64bit address space is enabled.
- **Size:** Select the BAR configuration space size. The maximum value is 1Mbytes.

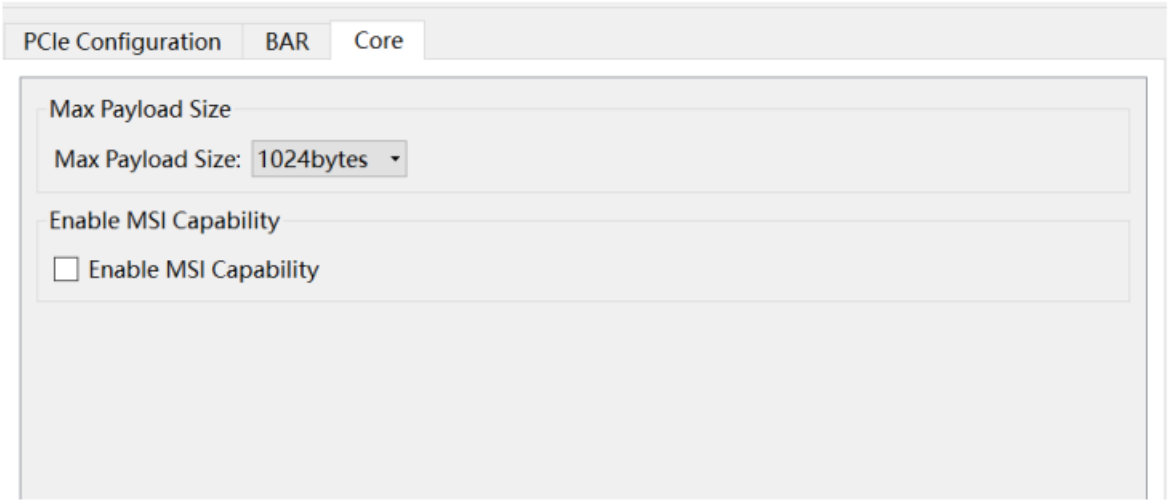
Figure 4-2 BAR Configuration of PCI Express Controller configuration



Function Configuration of PCI Express Controller Core
Users can configure the application information of the PCIe Core in this page.

- **Max Payload Size**: Supports Payload size up to 4K Bytes. Select via the drop-down menu, the size options include 128 Bytes/256 Bytes/512 Bytes/1024 Bytes /2048 Bytes /4096 Bytes.
- **MSI Capabilities**: Interrupt support, enable or disable the interrupt interface of MSI by checking the box.

Figure 4-3 BAR Configuration of PCIe Controller

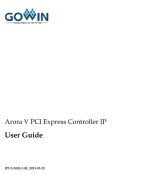


Appendix PCIe Configuration Register Information

Table A-1 PCIe Capability

31:24	23:16	15:8	7:0	Byte Offset
Capabilities Register		Net Cap PTR	Capability ID	080h
Device Capabilities				084h
Device Status		Device Control		088h
Link Capabilities				08Ch
Link Status		Link Control		090h
Slot Capabilities				094h
Slot Status		Slot Control		098h
Root Capabilities		Root Control		09Ch
Root Status				0A0h
Device Capabilities 2				0A4h
Device Status 2		Device Control 2		0A8h
Link Capabilities				0ACh
Link Status		Link Control		0B0h
Slot Capabilities				0B4h
Slot Status		Slot Control		0B8h

Documents / Resources

	GOWIN Arora V PCI Express Controller IP [pdf] User Guide Arora PCI Express Controller IP, Arora, PCI Express Controller IP, Express Controller IP, Controller IP

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