

FUTEK QIA128 SPI Communication Power Digital Controller User Guide

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FUTEK QIA128 SPI Communication Power Digital Controller

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General Description

The QIA128 is a single channel ultra-low power digital controller with UART and SPI outputs. The QIA128 (slave device) can be used to communicate with any master devices through an SPI bus.

Pin Configurations and Function Descriptions for QIA128

























6	-Excitation	Sensor excitation return (connected to Ground).	2
7	-Signal	Sensor negative Input.	5
8	+Excitation	Sensor excitation.	3
9	+Signal	Sensor positive Input.	4
10	VIN	Voltage input 3 – 5V	9
11	CS	Active low chip-select. Do not drive the CS line low until the device has booted up completely. Also ensure that the CS line is not driven low unless the RD is low.	14
12	SCLK	Serial clock generated by master.	13
13	MISO	Master-In-Slave-Out.	12
14	MOSI	Master-Out-Slave-In.	11
15	INT	Active low INT pin is used to keep all communication synchronized. It notifies the master device when new data from the sampling system is ready. This ensures that the master is always collecting the latest data. When the INT pin goes low, it indicates that the data is ready to be clocked out. This pin can be used to externally interrupt the master. The pin returns high when the system is in a conversion state and returns low once new data is ready. *Note: The pin does not return high once data is read—it will only return high once the system enters a conversion state.	–
16	VDD	Digital rail (2.5V).	–
17	NTRST	JTAG NTRST/BM Reset/Boot Mode. Input pin used for debug and download only and boot mode (CS).	–
18	TDO	JTAG TDO (Data Out). Input pin used for debug and download.	–
19	TDI	JTAG TDI (Data In). Input pin used for debug and download.	–
20	TCK	JTAG TCK (Clock Pin). Input pin used for debug and download.	–

QIA128 SPI Configuration

Table 2.









Serial Word Length	8-Bit			
SPI Mode	Mode 0 (CPOL = 0, CPHA = 0)			
SCLK Frequency	Min	1 MHz	Max	2 MHz
Internal Clock Frequency of MCU	10.24 MHz			
Operation Mode	Slave			
Voltage Level	1.8 VDC (compatible with 3.3 VDC)			
















QIA128 Internal Design Algorithm

When the 
 
 
    pin goes high, it means the device is in the process of A/D conversion, calculating the CRC8 (See
CRC
Calculations and References) and generating the packet that needs to be sent per the master device’s request.
  
 
 
 goes
low as soon as it fills out the SPI TX buffer. The following algorithm is being executed while   
 
  is high:

- Receives the latest ADC data from the highest interrupt priority
- Slave Service Function
 - o Keeps reading the RX FIFO until it is empty
 - o Saves all the bytes in a software buffer
 - o If the buffer is empty, creates a mock-up GADC command to go to the default state
 - o Checks the CRC8 byte and CMD byte
 - If either the CRC8 or the CMD are incorrect
- Goes to the default state
 - Else
- Replies with the corresponding packet (See Table 5.)

Default State:

- Restarts the SPI module
- Calculates the CRC8
- Loads 4 bytes of data (including the latest ADC data and the CRC8 byte) into the TX FIFO buffe
- 
-  
-  
-    goes low

It is important to note that when a packet is clocked into the QIA128 via the MOSI line, the response to that packet
must be
clocked out in the very next 
 
 
 
 period. If it is not clocked out in the next   
 
 

?? period, the response will be lost, and the system will go back to clocking out the ADC data.

SPI Packet Structure

The packet structure stays consistent during all transactions and always includes four bytes of data for both receiving and transmitting.

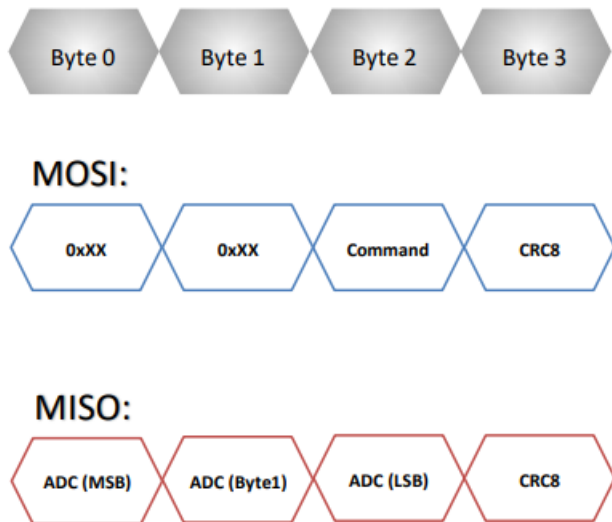


Figure 2.

“Continuous Read” Mode

GADC Command may be sent for each

period to continuously get the ADC data.

*Note: If the CRC or the CMD bytes are incorrect, the device still fills out the buffer with the ADC data followed by the CRC8.

Timing Diagrams

Packet Structure (Get ADC Data):

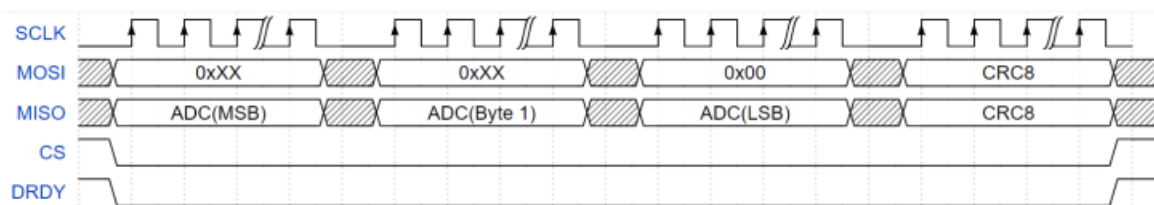


Figure 3.

*Note: Each clock in Figure 3. represents 8-bits.

*Note: Each word (8-bits) can be clocked out with or without delay, but the entire transaction must be completed within a single

period.

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