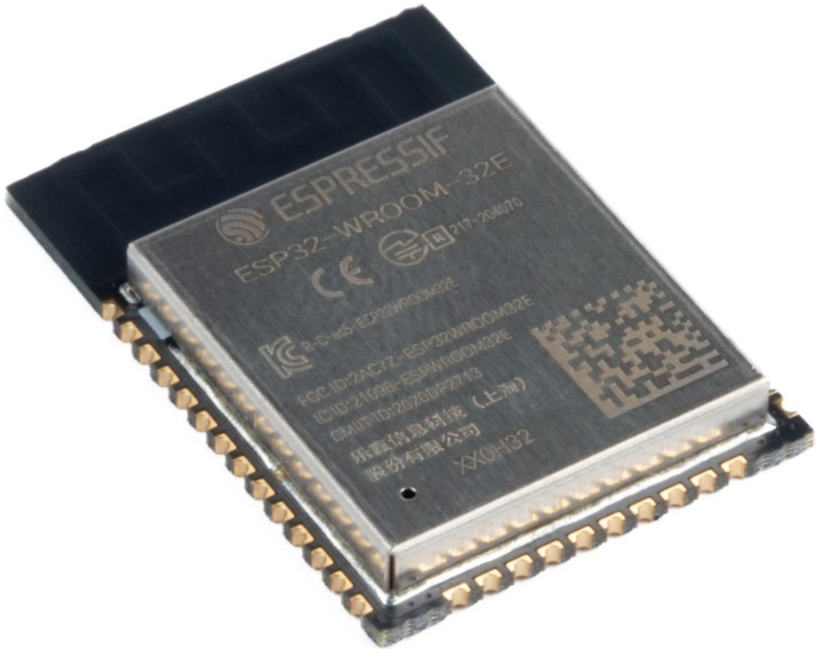
espressif ESP32-WROOM-32E Bluetooth Low Energy WiFi User Manual

espressif ESP32-WROOM-32E Bluetooth Low Energy WiFi User Manual



Contents

Overview

ESP32 -WROOM -32E is a powerful, generic WiFi -BT -BLE MCU module that targets a wide variety of applications, ranging from low -power sensor networks to the most demanding tasks, such as voice encoding, music streaming and MP3 decoding. This is a SMD Module with 2.4 GHz PCB antenna on board. It reserves π tuning circuit for antenna impedance matching. It is with all GPIOs on the pin -out except the ones already used for connecting flash. The Module's working voltage can be range from 3.0 V to 3.6 V. Frequency range is 2400 MHz to 2483.5 MHz. External 40 MHz as clock source for system. There is also a 4 MB SPI flash for storing user programs and data. The ordering information of ESP32 -WROOM -32E is listed as follows:

Module	Chip embedded	Flash	PSRAM	Module dimensions (mm)
ESP32-WROOM-32E	ESP32-D0WD-V3	4 MB 1	/	(18.00 ± 0.10) X (25.50 ± 0.10) X(3.10 ± 0.10) mm (including metallic shield)
Notes:1. ESP32-WROOM-32E (PCB) with 8 MB flash or 16 MB flash is available for custom order.2. For detailed ordering information, please see *Espressif Product Ordering Information*.3. For dimensions of the IPEX connector, please see Chapter 10.				

At the core of the module is the ESP32 -D0WD -V3 chip*. The chip embedded is designed to be scalable and adaptive. There are two CPU cores that can be individually controlled, and the CPU clock frequency is adjustable from 80 MHz to 240 MHz. The user may also power off the CPU and make use of the low power co -processor to constantly monitor the peripherals for changes or crossing of thresholds. ESP32 integrates a rich set of peripherals, ranging from capacitive touch sensors, Hall sensors, SD card interface, Ethernet, highspeed SPI, UART, I²S and I²C

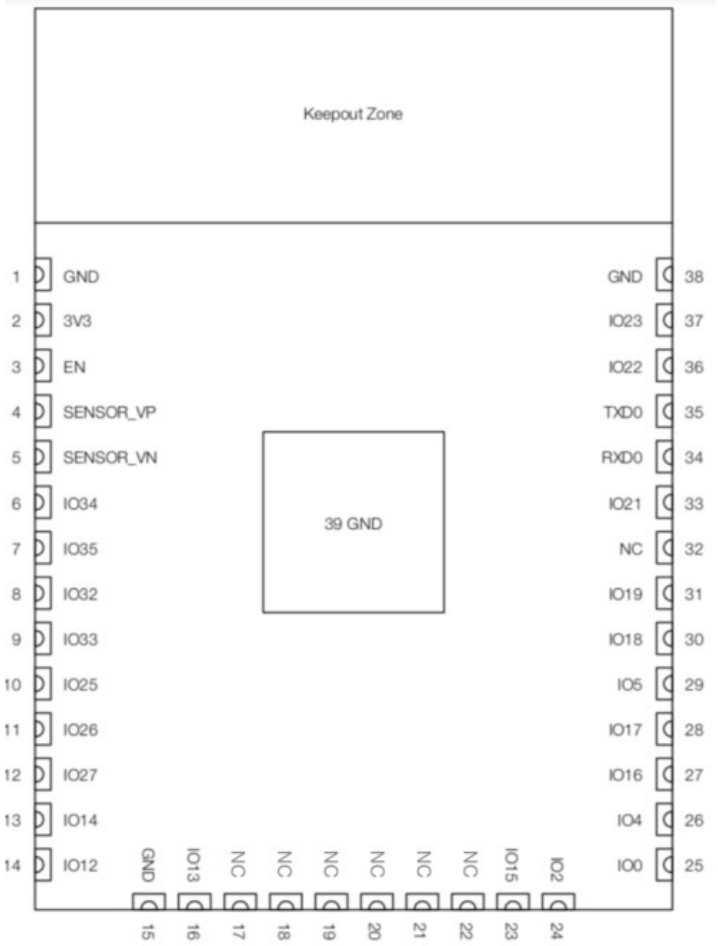
The operating system chosen for ESP32 is freeRTOS with LwIP; TLS 1.2 with hardware acceleration is built in as well. Secure (encrypted) over the air (OTA) upgrade is also supported, so that users can upgrade their products even after their release, at minimum cost and effort. Table 2 provides the specifications of ESP32 WROOM 32E.

Table 2: ESP32-WROOM-32E Specifications

Categories	Items	Specifications
Test	Reliablity	HTOL/HTSL/uHAST/TCT/ESD
Wi-Fi	Protocols	802.11 b/g/n20/n40
		A-MPDU and A-MSDU aggregation and 0.4 s guard in-terv al support
	Frequency range	2.412 GHz ~ 2.462GHz
Bluetooth	Protocols	Bluetooth v4.2 BR/EDR and BLE specification
	Radio	NZIF receiver with –97 dBm sensitivity
		Class-1, class-2 and class-3 transmitter
		AFH
	Audio	CVSD and SBC
Hardware	Module interfaces	SD card, UART, SPI, SDIO, I2C, LED PWM, Motor PWM,I 2S, IR, pulse counter, GPIO, capacitive touch sensor, ADC , DAC
	On-chip sensor	Hall sensor
	Integrated crystal	40 MHz crystal
	Integrated SPI flash	4 MB
	Integrated PSRAM	–
	Operating voltage/Power supply	3.0 V ~ 3.6 V
	Minimum current delivered bypower supply	500 mA
	Recommended operating tem-pe rature range	–40 °C ~ 85 °C
	Package size	(18.00±0.10) mm × (31.40±0.10) mm × (3.30±0.10) mm
	Moisture sensitivity level (MSL)	Level 3

Pin Definitions

Pin Layout



Pin Description

ESP32 WROOM 32E has 38 pins. See pin definitions in Table 3.

Name	No.	Type	Function
GND	1	P	Ground
3V3	2	P	Power supply
EN	3	I	Module-enable signal. Active high.
SENSOR_VP	4	I	GPIO36, ADC1_CH0, RTC_GPIO0
SENSOR_VN	5	I	GPIO39, ADC1_CH3, RTC_GPIO3
IO34	6	I	GPIO34, ADC1_CH6, RTC_GPIO4
IO35	7	I	GPIO35, ADC1_CH7, RTC_GPIO5
IO32	8	I/O	GPIO32, XTAL_32K_P (32.768 kHz crystal oscillator input), ADC1_CH4,TOUCH9, RTC_GPIO9
IO33	9	I/O	GPIO33, XTAL_32K_N (32.768 kHz crystal oscillator output),ADC1_CH5, TOUCH8, RTC_GPIO8

IO25	10	I/O	GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
IO26	11	I/O	GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1
IO27	12	I/O	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV
IO14	13	I/O	GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK,HS2_CLK, SD_CLK, EMAC_TXD2
IO12	14	I/O	GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ,HS2_DATA2, SD_DATA2, EMAC_TXD3
GND	15	P	Ground
IO13	16	I/O	GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID,HS2_DATA3, SD_DATA3, EMAC_RX_ER
NC	17	–	–
NC	18	–	–
NC	19	–	–
NC	20	–	–
NC	21	–	–
NC	22	–	–
IO15	23	I/O	GPIO15, ADC2_CH3, TOUCH3, MTDO, HSPICS0, RTC_GPIO13,HS2_CMD, SD_CMD, EMAC_RXD3
IO2	24	I/O	GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0,SD_DATA0
IO0	25	I/O	GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1,EMAC_TX_CLK
IO4	26	I/O	GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1,SD_DATA1, EMAC_TX_ER
IO16	27	I/O	GPIO16, HS1_DATA4, U2RXD, EMAC_CLK_OUT
IO17	28	I/O	GPIO17, HS1_DATA5, U2TXD, EMAC_CLK_OUT_180 –
IO5	29	I/O	GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK
IO18	30	I/O	GPIO18, VSPICLK, HS1_DATA7

Strapping Pins

ESP32 has five strapping pins, which can be seen in Chapter 6 Schematics:

- MTDI
- GPIO0
- GPIO2
- MTDO
- GPIO5

  Software can read the values of these five bits from register ”GPIO_STRAPPING”

Each strapping pin is connected to its internal pull -up/pull -down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high -impedance, the internal weak pull -up/pull –down will determine the default input level of the strapping pins. To change the strapping bit values, users can apply the external pull -down/pull-up resistances, or use the host MCU’s GPIOs to control the voltage level of these pins when powering on ESP32. After reset release, the strapping pins work as normal -function pins. Refer to Table 4 for a detailed boot -mode configuration by strapping pins

Booting Mode					
Pin	Default	SPI Boot		Download Boot	
GPIO 0	Pull-up	1		0	
GPIO 2	Pull-down	Don’t-care		0	
Enabling/Disabling Debugging Log Print over U0TXD During Booting					
Pin	Default	U0TXD Active		U0TXD Silent	
MTDO	Pull-up	1		0	
Timing of SDIO Slave					
Pin	Default	Falling-edge SamplingFalling-edge Output	Falling-edge SamplingRising-edge Output	Rising-edge SamplingFalling-edge Output	Rising-edge SamplingRising-edge Output
MTDO	Pull-up	0	0	1	1
GPIO 5	Pull-up	0	1	0	1

Note:

- Firmware can configure register bits to change the settings of ”Voltage of Internal LDO (VDD_SDIO)” and”Timing of SDIO Slave” after booting.
- Internal pull up resistor (R9) for MTDI is not populated in the module, as the flash and SRAM in ESP32 -32E only support a power voltage of 3.3 V (output by VDD_SDIO)

Functional Description

This chapter describes the modules and functions integrated in ESP32 -WROOM -32E

CPU and Internal Memory
ESP32 D0WD V3 contains two low power Xtensa ® 32 bit LX6 microprocessors. The internal memory includes: • 448 KB of ROM for booting and core functions.

- 520 KB of on chip SRAM for data and instructions.
- 8 KB of SRAM in RTC, which is called RTC FAST Memory and can be used for data storage; it is accessed by the main CPU during RTC Boot from the Deep sleep mode.
- 8 KB of SRAM in RTC, which is called RTC SLOW Memory and can be accessed by the co processor during the Deep sleep mode.
- 1 Kbit of eFuse: 256 bits are used for the system (MAC address and chip configuration) and the remaining 768 bits are reserved for customer applications, including flash -encryption and chip -ID.

External Flash and SRAM
ESP32 supports multiple external QSPI flash and SRAM chips. More details can be found in Chapter SPI in the ESP32 Technical Reference Manual . ESP32 also supports hardware encryption/decryption based on AES to pro - tect developers' programs and data in flash. ESP32 can access the external QSPI flash and SRAM through high - speed caches.

- The external flash can be mapped into CPU instruction memory space and read -only memory space simul- taneously. – When external flash is mapped into CPU instruction memory space, up to 11 MB + 248 KB can be mapped at a time. Note that if more than 3 MB + 248 KB are mapped, cache performance will be reduced due to speculative reads by the CPU. – When external flash is mapped into read-only data memory space, up to 4 MB can be mapped at a time. 8 -bit, 16 -bit and 32 -bit reads are supported.
- External SRAM can be mapped into CPU data memory space. Up to 4 MB can be mapped at a time. 8- bit, 16 - bit and 32 -bit reads and writes are supported. ESP32 -WROOM -32E integrates a 4 MB SPI flash more memory space.

RTC and Low -Power Management
With the use of advanced power -management technologies, ESP32 can switch between different power modes. For details on ESP32's power consumption in different power modes, pleas e refer to section "RTC and Low – Power Management" in ESP32 User Manua

Peripherals and Sensors

Note:
External connections can be made to any GPIO except for GPIOs in the range 6 -11, 16, or 17. GPIOs 6 -11 are connected to the module's integrated SPI flash. For details, please see Section 6 Schematics.

Electrical Characteristics

Absolute Maximum Ratings
Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device that should follow the recommended operating conditions.

1. The module worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in three domains (VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO) output high logic level to ground.
2. Please see Appendix IO_MUX of ESP32 Datasheet for IO's power

Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I*V DD*	Current delivered by external power supply	0.5	–	–	A
T	Operating temperature	–40	–	85	°C

DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter		Min	Typ	Max	Unit
C*IN*	Pin capacitance		–	2	–	pF
V*IH*	High-level input voltage		0.75×VDD1	–	VDD1+0.3	V
V*IL*	Low-level input voltage		–0.3	–	0.25×VDD1	V
I*IH*	High-level input current		–	–	50	nA
I*IL*	Low-level input current		–	–	50	nA
V*OH*	High-level output voltage		0.8×VDD1	–	–	V
V*OL*	Low-level output voltage		–	–	0.1×VDD1	V
I*OH*	High-level source current (VDD1 = 3.3 V, V*OH* >= 2.64 V,output drive strength set to themaximum)	VDD3P3_CPU power domain 1*;* 2	–	40	–	mA
		VDD3P3_RTC power domain 1*;* 2	–	40	–	mA
		VDD_SDIO power domain 1*;* 3	–	20	–	mA

Symbol	Parameter	Min	Typ	Max	Unit
I*OL*	Low-level sink current(VDD1 = 3.3 V, V*OL* = 0.495 V,output drive strength set to the maximum)	–	28	–	mA
R*P U*	Resistance of internal pull-up resistor	–	45	–	kΩ
R*P D*	Resistance of internal pull-down resistor	–	45	–	kΩ
V*IL_nRST*	Low-level input voltage of CHIP_PU to power off the chip	–	–	0.6	V

Notes:

1. Please see Appendix IO_MUX of ESP32 Datasheet for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.

2. For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, VOH>=2.64 V, as the number of current-source pins increases.
3. Pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

Wi-Fi Radio

Parameter	Condition	Min	Typical	Max	Unit
Operating frequency range *note* 1	–	2412	–	2462	MHz
RF Power	802.11b:26dBm802.11g:25.42dBm802.11n20:25.48dBm802.11n40:25.78dBm				dBm
Sensitivity	11b, 1 Mbps	–	–98	–	dBm
	11b, 11 Mbps	–	–89	–	dBm
	11g, 6 Mbps	–	–92	–	dBm
	11g, 54 Mbps	–	–74	–	dBm
	11n, HT20, MCS0	–	–91	–	dBm
	11n, HT20, MCS7	–	–71	–	dBm
	11n, HT40, MCS0	–	–89	–	dBm
	11n, HT40, MCS7	–	–69	–	dBm
Adjacent channel rejection	11g, 6 Mbps	–	31	–	dB
	11g, 54 Mbps	–	14	–	dB
	11n, HT20, MCS0	–	31	–	dB
	11n, HT20, MCS7	–	13	–	dB

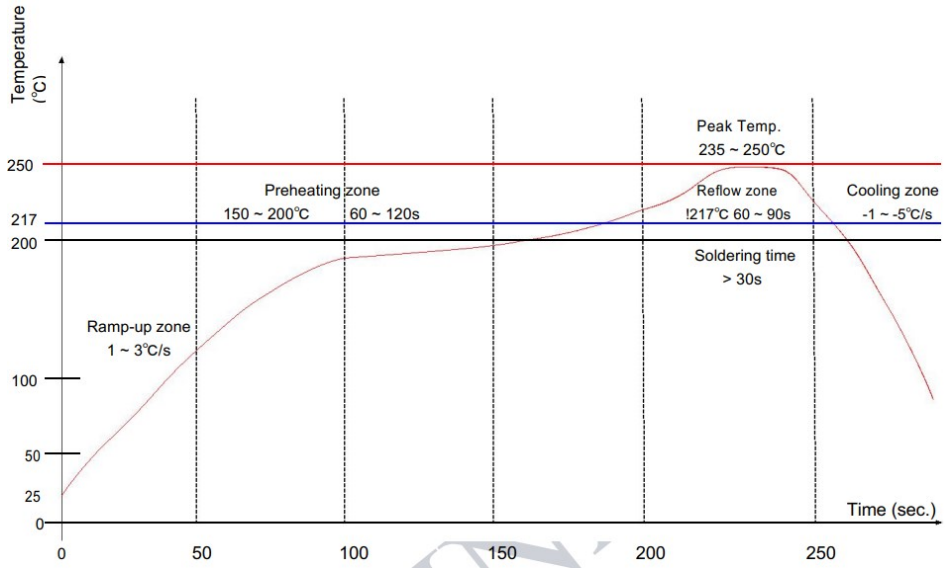
Bluetooth/BLE Radio

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	–	–	–97	–	dBm
Maximum received signal @30.8% PER	–	0	–	–	dBm
Co-channel C/I	–	–	+10	–	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	–	–5	–	dB
	F = F0 – 1 MHz	–	–5	–	dB
	F = F0 + 2 MHz	–	–25	–	dB
	F = F0 – 2 MHz	–	–35	–	dB
	F = F0 + 3 MHz	–	–25	–	dB
	F = F0 – 3 MHz	–	–45	–	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	–10	–	–	dBm
	2000 MHz ~ 2400 MHz	–27	–	–	dBm
	2500 MHz ~ 3000 MHz	–27	–	–	dBm
	3000 MHz ~ 12.5 GHz	–10	–	–	dBm
Intermodulation	–	–36	–	–	dBm

Transmitter

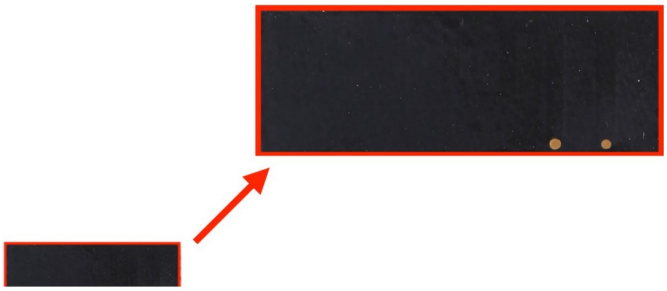
Parameter	Conditions	Min	Typ	Max	Unit
RF Frequency	–	2402	–	2480	MHz
Gain control step	–	–	3	–	dBm
RF power control range	–	–12	–	+10	dBm
Adjacent channel transmit power	F = F0 ± 2 MHz	–	–52	–	dBm
	F = F0 ± 3 MHz	–	–58	–	dBm
	F = F0 ± > 3 MHz	–	–60	–	dBm
Δ *f*1avg	–	–	–	265	kHz
Δ *f*2max	–	247	–	–	kHz
Δ *f*2avg/Δ *f*1avg	–	–	–0.92	–	–
ICFT	–	–	–10	–	kHz
Drift rate	–	–	0.7	–	kHz/50 s
Drift	–	–	2	–	kHz

Reflow Profile

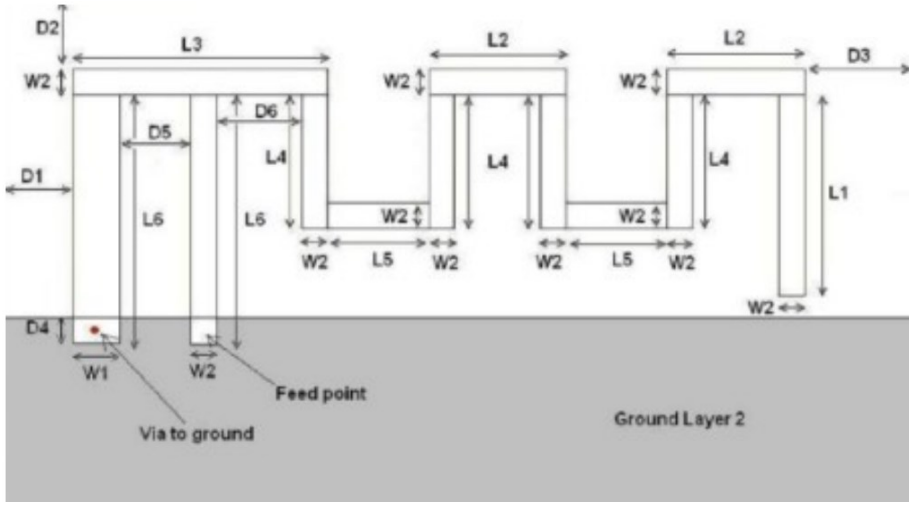


Ramp -up zone — Temp.: <150 Time: 60 ~ 90s Ramp -up rate: 1 ~ 3 /s **Preheating zone — Temp.:** 150 ~ 200 Time: 60 ~ 120s Ramp -up rate: 0.3 ~ 0.8 /s
Reflow zone — Temp.: >217 7LPH60 ~ 90s; Peak Temp.: 235 ~ 250 (<245 recommended) Time: 30 ~ 70s
Cooling zone — Peak Temp. ~ 180 Ramp -down rate: -1 ~ -5 /s

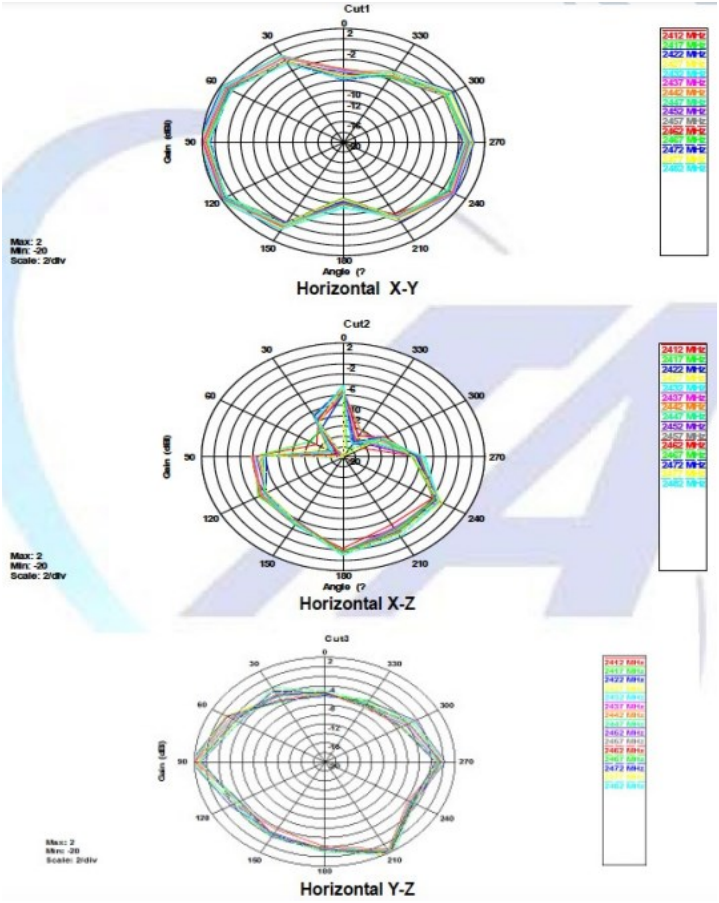
Antenna Specifications

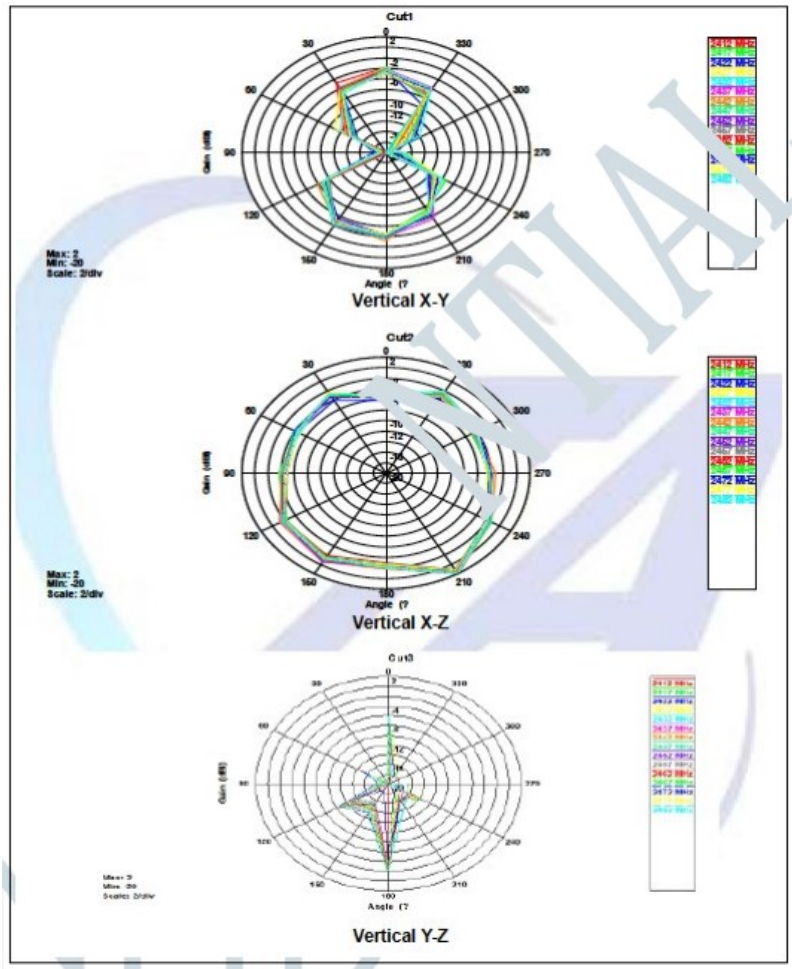


Dimensions:



Pattern Plots:





Revision History

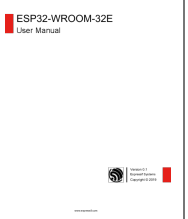
Date	Version	Release notes
2020.02	V0.1	Preliminary release for certification CE& FCC.

OEM Guidance

1. Applicable FCC rules This module is granted by Single Modular Approval. It complies to the requirements of FCC part 15C, section 15.247 rules.
2. The specific operational use conditions This module can be used in IoT devices. The input voltage to the module is nominally 3.3V-3.6 V DC. The operational ambient temperature of the module is -30 to 85 degree C. Only the embedded PCB antenna is allowed. Any other external antenna is prohibited.
3. Limited module procedures N/A
4. Trace antenna design N/A
5. RF exposure considerations
   The equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. The equipment has the additional RF exposure evaluation necessary for portable usage of the Bluetooth radio < 20cm between the radiator and body. For the change in the module's RF exposure condition from mobile to portable, the Wi-Fi radio is disabled.
6. Antenna Antenna type: PCB antenna; Peak gain: 3.40dBi
7. Label and compliance information An exterior label on OEM's end product can use wording such as the following: "Contains Transmitter Module FCC ID: 2A9ZM-WROOM32E" or "Contains FCC ID: 2A9ZM-WROOM32E."
8. Information on test modes and additional testing requirements
   a)The modular transmitter has been fully tested by the module grantee on the required number of channels,modulation types, and modes, it should not be necessary for the host installer to re-test all the available transmitter modes or settings. It is recommended that the host product manufacturer, installing the modular transmitter,perform some investigative measurements to confirm that the resulting composite system does not exceed the spurious emissions limits or band edge limits (e.g., where a different antenna may be causing additional emissions).
   b)The testing should check for emissions that may occur due to the intermixing of emissions with the other transmitters, digital circuitry, or due to physical properties of the host product (enclosure). This investigation is especially important when integrating multiple modular transmitters where the certification is based on testing each of them in a stand-alone configuration. It is important to note that host product manufacturers should not assume that because the modular transmitter is certified that they do not have any responsibility for final product compliance.
   c)If the investigation indicates a compliance concern the host product manufacturer is obligated to mitigate the issue. Host products using a modular transmitter are subject to all the applicable individual technical rules as well as to the general conditions of operation in Sections 15.5, 15.15, and 15.29 to not cause interference. The operator of the host product will be obligated to stop operating the device until the interference have been corrected .
9. Additional testing, Part 15 Sub part B disclaimer The final host / module combination need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

FCC Warning:
Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation

Documents / Resources

	espressif ESP32-WROOM-32E Bluetooth Low Energy WiFi [pdf] User Manual ESP32-WROOM-32E Bluetooth Low Energy WiFi, ESP32-WROOM-32E, Bluetooth Low Energy WiFi, Low Energy WiFi, Energy WiFi, WiFi

References

- Wi-Fi & Bluetooth MCUs and AIoT Solutions I Espressif Systems