



EMBUX SOM4019 Module with Dual Band Dual Concurrent Wi-Fi User Manual

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EMBUX SOM4019 Module with Dual Band Dual Concurrent Wi-Fi



Product Information

Specifications:

• Processor: ARM Cortex-A7, 716.8MHz, 256KB L2 Cache

• Memory: DRAM NOR FLASH

• Wi-Fi:

- IEEE 802.11 b/g/n 2×2 2.4GHz 20/40 MHz
- IEEE 802.11 an/ac 2×2 5GHz 20/40/80 MHz
- Peripherals: PCle 2.0, USB 2.0, USB 3.0, UART, SPI (Master), I2C, GPIO, JTAG, Copper 10BASE-Te/100BASE-TX/1000BASE-T, Reset, SDIO3.0/eMMC, Antenna connector
- Operating temperature: [Specify operating temperature]
- Storage temperature: [Specify storage temperature]

Product Overview:

The SOM4019 module is based on an IPQ4019/IPQ4029 SoC from Qualcomm, which incorporates a powerful quad-core ARM Cortex A7 processor. It is ideal for resource demanding applications including routers, gateways, and access points. The SOM4019 comes with a high-power, dual-band concurrent radio supporting 802.11ac Wave2 technology (2×2 MIMO). It also has USB ports and supports other miscellaneous interfaces, which can be configured as general-purpose I/O pins.

Block Diagram:	
Block Diagram	

Pin Definition:

Pin ID	Pin Name	Туре	Description
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1. Installation:

[Step-by-step installation process]

2. Configuration:

[Step-by-step configuration instructions]

3. Maintenance:

[Maintenance tips and guidelines]

4. Troubleshooting:

[Common issues and solutions]

FAQ (Frequently Asked Questions)

- Q: How do I reset the device to factory settings?
 - A: [Answer to the question about resetting the device]
- Q: Can I upgrade the Wi-Fi data rate on this module?
 - A: [Answer to the question about upgrading Wi-Fi data rate]

SOM4019

IPQ4019 SOM module with dual band dual concurrent Wi-Fi

FCC Warning

Note:

- Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user authority to operate the equipment.
- To comply with FCC RF exposure compliance requirements, a separation distance of at least 20 cm must be maintained between the antenna of this device and all persons.
- This Transmitter must not be co-located or operating in conjunction with any other antenna or transmitter

This device is intended only for OEM integrators under the following conditions:

- 1. The antenna must be installed such that 20 cm is maintained between the antenna and users. For laptop installations, the antenna must be installed to ensure that the proper spacing is maintained in the event the users places the device in their lap during use (i.e. positioning of antennas must be placed in the upper portion of the LCD panel only to ensure 20 cm will be maintained if the user places the device in their lap for use) and
- 2. The transmitter module may not be co-located with any other transmitter or antenna. As long as the 2 conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

This transmitter module is authorized only for use in devices where the antenna may be installed such that 20 cm may be maintained between the antenna and users (for example access points, routers, wireless ASDL modems, certain laptop configurations, and similar equipment). The final end product must be labeled in a visible area with the following: "Contains TX **FCC ID:** 2AVW3-SOM4019.

RF Exposure Manual Information That Must be Included

The users manual for end users must include the following information in a prominent location "IMPORTANT NOTE: To comply with FCC RF exposure compliance requirements, the antenna used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter."

Additional Information That Must be Provided to OEM Integrators

The end user should NOT be provided any instructions on how to remove or install the device.

Main Features

• Chipset: industrial-grade IPQ4019 chipset

• Standard: 802.11ABGN/AC

PCB mounting with normal pin header

Antenna: 2 x IPEX connectors, 2T2R
Data rate up to 300 Mbps + 866 Mbps

• Enhanced wireless security: WEP, WPA, WPA2

· High RF power for longer communication range



Product Overview

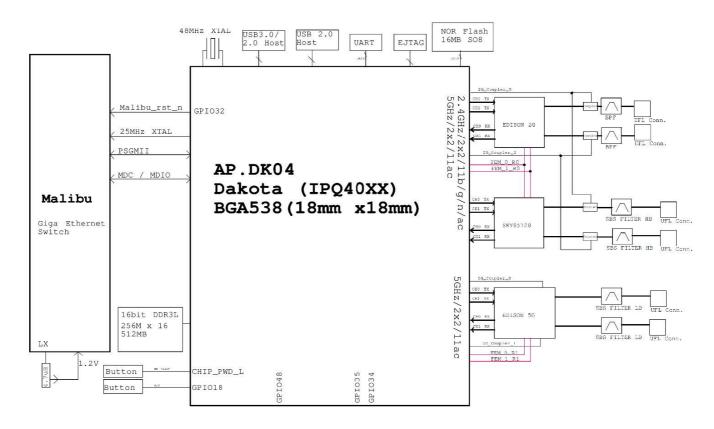
SOM4019 module is based on an IPQ4019/IPQ4029 SoC from Qualcomm, which incorporates a powerful quadcore ARM Cortex A7 processor. It is ideal for resource demanding applications including routers, gateways and access points. SOM4019 comes with a high-power, dual-band concurrent radio supporting 802.11ac Wave2 technology (2×2 MIMO). It also has USB ports and supports other miscellaneous interfaces, which can be configured as general-purpose I/O pins.

Specification

Item	Description	SOM4019
Processor	ARM Cortex-A7, 716.8MHz, 256KB L2 Cache	IPQ4019
Memory	DRAM	DDR3L 512 MB
Wellioty	NOR FLASH	32MB
	IEEE 802.11 b/g/n 2×2 2.4GHz 20/40 MHz	2412MHz – 2482MHz
Wi-Fi	IEEE 802.11 an/ac 2×2 5GHz 20/40/80 MHz	5180MHz – 5240MHz 5745MHz – 5825MHz
	PCle 2.0	1
	USB 2.0	1
	USB 3.0	1
	UART	2
	SPI (Master)	1
Peripherals	I2C	2
	GPIO	14
	JTAG	1
	Copper 10BASE-Te/100BASE-TX/1000BASE-T	2
	Reset	1
	SDIO3.0/eMMC	1
RF Interface	Antenna connector	IPEX
Temperature	Operating temperature	-40~75°C
Tomperature	Storage temperature	-40 °C ~ 85 °C

Block diagram

Functional Block Diagram



Pin Definition

Pin ID	Pin Name	Туре	Description
P1	GND	GND	Ground
P2	GND	GND	Ground
P3	P3_TRX0+	AI/AO	PHY3 Media Dependent Interface pair 0, connect to XFMR
P4	P3_TRX0-	AI/AO	Firms Media Dependent interface pair 0, confiect to XI Min
P5	P3_TRX1+	AI/AO	PHY3 Media Dependent Interface pair 1, connect to XFMR
P6	P3_TRX1-	AI/AO	PH 13 Media Dependent interface pair 1, connect to ArMh
P7	P3_TRX2+	AI/AO	PHY3 Media Dependent Interface pair 2, connect to XFMR
P8	P3_TRX2-	AI/AO	11113 Media Dependent interface pair 2, confiect to XI With
P9	P3_TRX3+	AI/AO	PHY3 Media Dependent Interface pair 3, connect to XFMR
P10	P3_TRX3-	AI/AO	1 1113 Media Dependent interface pair 3, confiect to XI Mit
P11	GND	GND	Ground
P12	GND	GND	Ground
P13	P4_TRX0+	AI/AO	PHY4 Media Dependent Interface pair 0, connect to XFMR
P14	P4_TRX0-	AI/AO	T TTT T MICGIA Dependent interiace pair 0, connect to XI WIT

P15	P4_TRX1+	AI/AO	
			PHY4 Media Dependent Interface pair 1, connect to XFMR

P4_TRX2+	P16	P4_TRX1-	AI/AO	
P18 P4_TRX2- AI/AO PHY4 Media Dependent Interface pair 2, connect to XFMR P19 P4_TRX3+ AI/AO PHY4 Media Dependent Interface pair 3, connect to XFMR P20 P4_TRX3- AI/AO PHY4 Media Dependent Interface pair 3, connect to XFMR P21 GND GND Ground P22 GND GND Ground P23 PCIE_TXP AO Clock to PCIe end point P24 PCIE_TXN AO Clock to PCIe end point P25 PCIE_RXP AI PCIe receive lane – positive P26 PCIE_RXN AI PCIe receive lane – negative P27 PCIE_CLKOUT_P AO PCIe transmit lane – negative P28 PCIE_CLKOUT_N AO PCIe transmit lane – negative P29 GND GND Ground P30 GND GND Ground P31 USB2_DP AI, AO USB HS data plus P33 GND GND Ground P34 GND GND Ground		_		
P19 P4_TRX3+ Al/AO PHY4 Media Dependent Interface pair 3, connect to XFMR P20 P4_TRX3- Al/AO GND Ground P21 GND GND Ground P22 GND GND Ground P23 PCIE_TXP AO Clock to PCIe end point P24 PCIE_TXN AO Clock to PCIe end point P25 PCIE_TXN AI PCIe receive lane – positive P26 PCIE_RXN AI PCIe receive lane – negative P27 PCIE_CLKOUT_P AO PCIe transmit lane – negative P28 PCIE_CLKOUT_N AO PCIe transmit lane – negative P29 GND GND Ground P30 GND GND Ground P31 USB2_DP AI, AO USB HS data plus P32 USB2_DM AI, AO USB HS data negative P33 GND GND Ground P34 GND GND Ground P35 USB3_SS_TX_P <		_		PHY4 Media Dependent Interface pair 2, connect to XFMR
PHY4 Media Dependent Interface pair 3, connect to XFMR		_		
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P22 GND Ground P23 PCIE_TXP AO Clock to PCIe end point P24 PCIE_TXN AO Clock to PCIe end point P25 PCIE_RXP AI PCIe receive lane – positive P26 PCIE_RXN AI PCIe receive lane – negative P27 PCIE_CLKOUT_P AO PCIe transmit lane – positive P28 PCIE_CLKOUT_N AO PCIe transmit lane – negative P29 GND GND Ground P30 GND GND Ground P31 USB2_DP AI, AO USB HS data plus P32 USB2_DM AI, AO USB HS data negative P33 GND GND Ground P34 GND Ground P35 USB3_SS_TX_P AO SS USB transmit data positive P36 USB3_SS_TX_N AO USB SS receive data negative P37 USB3_SS_TX_N AI USB HS data positive P39 USB3_HS_DM AI, AO USB HS data negat		_		Outpured.
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P24 PCIE_TXN AO Clock to PCIe end point P25 PCIE_RXP AI PCIe receive lane – positive P26 PCIE_RXN AI PCIe receive lane – negative P27 PCIE_CLKOUT_P AO PCIe transmit lane – negative P28 PCIE_CLKOUT_N AO PCIe transmit lane – negative P29 GND GND Ground P30 GND GND Ground P31 USB2_DP AI, AO USB HS data plus P32 USB2_DM AI, AO USB HS data negative P33 GND GND Ground P34 GND Ground P35 USB3_SS_TX_P AO SS USB transmit data positive P36 USB3_SS_TX_N AO USB SS receive data positive P37 USB3_SS_RX_P AI USB SS receive data negative P39 USB3_HS_DP AI, AO USB HS data negative P40 USB3_HS_DM AI, AO USB HS data negative P41 GND	P22	GND	GND	Ground
P25 PCIE_RXP AI PCle receive lane – positive P26 PCIE_RXN AI PCle receive lane – negative P27 PCIE_CLKOUT_P AO PCle transmit lane – positive P28 PCIE_CLKOUT_N AO PCle transmit lane – negative P29 GND GND Ground P30 GND GND Ground P31 USB2_DP AI, AO USB HS data plus P32 USB2_DM AI, AO USB HS data negative P33 GND GND Ground P34 GND Ground P35 USB3_SS_TX_P AO SS USB transmit data positive P36 USB3_SS_TX_N AO USB SS receive data positive P37 USB3_SS_RX_P AI USB SS receive data negative P38 USB3_HS_DP AI, AO USB HS data negative P40 USB3_HS_DM AI, AO USB HS data negative P41 GND GND Ground P42 GND GND	P23	PCIE_TXP	AO	Clock to PCIe end point
P26 PCIE_RXN AI PCIe receive lane – negative P27 PCIE_CLKOUT_P AO PCIe transmit lane – positive P28 PCIE_CLKOUT_N AO PCIe transmit lane – negative P29 GND GND GND Ground P30 GND GND Ground P31 USB2_DP AI, AO USB HS data plus P32 USB2_DM AI, AO USB HS data negative P33 GND GND Ground P34 GND GND Ground P35 USB3_SS_TX_P AO SS USB transmit data positive P36 USB3_SS_TX_N AO USB SS transmit data negative P37 USB3_SS_RX_P AI USB SS receive data negative P38 USB3_HS_DP AI, AO USB HS data negative P39 USB3_HS_DP AI, AO USB HS data negative P40 USB3_HS_DM AI, AO USB HS data negative P41 GND GND Ground P42 GND GND Ground P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SSO_N I/O GPIO45 P45 BISP_SPI1_MISO I/O GPIO47 P47 GND GND GND Ground	P24	PCIE_TXN	AO	Clock to PCle end point
P27 PCIE_CLKOUT_P AO PCle transmit lane – positive P28 PCIE_CLKOUT_N AO PCle transmit lane – negative P29 GND GND Ground P30 GND GND Ground P31 USB2_DP AI, AO USB HS data plus P32 USB2_DM AI, AO USB HS data negative P33 GND GND Ground P34 GND GND Ground P35 USB3_SS_TX_P AO SS USB transmit data positive P36 USB3_SS_TX_N AO USB SS receive data positive P37 USB3_SS_RX_P AI USB SS receive data negative P38 USB3_HS_DP AI, AO USB HS data positive P40 USB3_HS_DP AI, AO USB HS data negative P41 GND GND Ground P42 GND GND Ground P43 BISP_SPI1_SCK I/O GPIO45 P44 BISP_SPI1_MOSI I/O GP	P25	PCIE_RXP	Al	PCIe receive lane – positive
P28 PCIE_CLKOUT_N AO PCIe transmit lane – negative P29 GND GND Ground P30 GND GND Ground P31 USB2_DP AI, AO USB HS data plus P32 USB2_DM AI, AO USB HS data negative P33 GND Ground P34 GND GND Ground P35 USB3_SS_TX_P AO SS USB transmit data positive P36 USB3_SS_TX_N AO USB SS transmit data negative P37 USB3_SS_TX_N AO USB SS receive data negative P38 USB3_SS_RX_P AI USB SS receive data negative P39 USB3_HS_DP AI, AO USB HS data negative P39 USB3_HS_DP AI, AO USB HS data negative P40 USB3_HS_DM AI, AO USB HS data negative P41 GND GND Ground P42 GND GND Ground P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SSO_N I/O GPIO45 P45 BISP_SPI1_MISO I/O GPIO47 P47 GND GND GROUND P47 GND GND GROUND	P26	PCIE_RXN	Al	PCIe receive lane – negative
P29 GND GND Ground P30 GND GND Ground P31 USB2_DP AI, AO USB HS data plus P32 USB2_DM AI, AO USB HS data negative P33 GND GND Ground P34 GND GND Ground P35 USB3_SS_TX_P AO SS USB transmit data positive P36 USB3_SS_TX_N AO USB SS receive data positive P37 USB3_SS_RX_P AI USB SS receive data negative P38 USB3_HS_DP AI, AO USB HS data positive P39 USB3_HS_DM AI, AO USB HS data negative P40 USB3_HS_DM AI, AO USB HS data negative P41 GND GND Ground P42 GND GND Ground P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_MOSI I/O GPIO45 P45 BISP_SPI1_MISO I/O GPIO47	P27	PCIE_CLKOUT_P	AO	PCIe transmit lane – positive
P30 GND Ground P31 USB2_DP AI, AO USB HS data plus P32 USB2_DM AI, AO USB HS data negative P33 GND GND Ground P34 GND GND Ground P35 USB3_SS_TX_P AO SS USB transmit data positive P36 USB3_SS_TX_N AO USB SS transmit data negative P37 USB3_SS_RX_P AI USB SS receive data positive P38 USB3_SS_RX_N AI USB HS data positive P39 USB3_HS_DP AI, AO USB HS data negative P40 USB3_HS_DM AI, AO USB HS data negative P41 GND GND Ground P42 GND GND Ground P43 BISP_SPI1_SCK I/O GPIO45 P44 BISP_SPI1_MOSI I/O GPIO46 P45 BISP_SPI1_MISO I/O GPIO47 P46 BISP_SPI1_MISO I/O GPIO47 <td< td=""><td>P28</td><td>PCIE_CLKOUT_N</td><td>AO</td><td>PCIe transmit lane – negative</td></td<>	P28	PCIE_CLKOUT_N	AO	PCIe transmit lane – negative
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P32 USB2_DM AI, AO USB HS data negative P33 GND GND Ground P34 GND GND Ground P35 USB3_SS_TX_P AO SS USB transmit data positive P36 USB3_SS_TX_N AO USB SS transmit data negative P37 USB3_SS_RX_P AI USB SS receive data positive P38 USB3_SS_RX_N AI USB HS data positive P39 USB3_HS_DP AI, AO USB HS data negative P40 USB3_HS_DM AI, AO USB HS data negative P41 GND GND Ground P42 GND Ground P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SSO_N I/O GPIO45 P45 BISP_SPI1_MOSI I/O GPIO47 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND Ground	P30	GND	GND	Ground
P33 GND GND Ground P34 GND GND Ground P35 USB3_SS_TX_P AO SS USB transmit data positive P36 USB3_SS_TX_N AO USB SS transmit data negative P37 USB3_SS_RX_P AI USB SS receive data positive P38 USB3_SS_RX_N AI USB SS receive data negative P39 USB3_HS_DP AI, AO USB HS data positive P40 USB3_HS_DM AI, AO USB HS data negative P41 GND GND Ground P42 GND Ground P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SSO_N I/O GPIO45 P44 BISP_SPI1_MOSI I/O GPIO46 P45 BISP_SPI1_MISO I/O GPIO47 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND Ground	P31	USB2_DP	AI, AO	USB HS data plus
P34 GND GND Ground P35 USB3_SS_TX_P AO SS USB transmit data positive P36 USB3_SS_TX_N AO USB SS transmit data negative P37 USB3_SS_RX_P AI USB SS receive data positive P38 USB3_SS_RX_N AI USB SS receive data negative P39 USB3_HS_DP AI, AO USB HS data positive P40 USB3_HS_DM AI, AO USB HS data negative P41 GND Ground P42 GND GND Ground P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SSO_N I/O GPIO45 P45 BISP_SPI1_MOSI I/O GPIO46 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND Ground	P32	USB2_DM	AI, AO	USB HS data negative
P35 USB3_SS_TX_P AO SS USB transmit data positive P36 USB3_SS_TX_N AO USB SS transmit data negative P37 USB3_SS_RX_P AI USB SS receive data positive P38 USB3_SS_RX_N AI USB SS receive data negative P39 USB3_HS_DP AI, AO USB HS data positive P40 USB3_HS_DM AI, AO USB HS data negative P41 GND GND Ground P42 GND GND Ground P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SSO_N I/O GPIO45 P45 BISP_SPI1_MOSI I/O GPIO46 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND GROUND	P33	GND	GND	Ground
P36 USB3_SS_TX_N AO USB SS transmit data negative P37 USB3_SS_RX_P AI USB SS receive data positive P38 USB3_SS_RX_N AI USB SS receive data negative P39 USB3_HS_DP AI, AO USB HS data positive P40 USB3_HS_DM AI, AO USB HS data negative P41 GND GND Ground P42 GND GND Ground P44 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SSO_N I/O GPIO45 P45 BISP_SPI1_MOSI I/O GPIO46 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND GROUND	P34	GND	GND	Ground
P37 USB3_SS_RX_P AI USB SS receive data positive P38 USB3_SS_RX_N AI USB SS receive data negative P39 USB3_HS_DP AI, AO USB HS data positive P40 USB3_HS_DM AI, AO USB HS data negative P41 GND GND Ground P42 GND GND Ground P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SSO_N I/O GPIO45 P45 BISP_SPI1_MOSI I/O GPIO46 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND GROUND	P35	USB3_SS_TX_P	AO	SS USB transmit data positive
P38 USB3_SS_RX_N AI USB SS receive data negative P39 USB3_HS_DP AI, AO USB HS data positive P40 USB3_HS_DM AI, AO USB HS data negative P41 GND GND Ground P42 GND GND Ground P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SSO_N I/O GPIO45 P45 BISP_SPI1_MOSI I/O GPIO46 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND Ground	P36	USB3_SS_TX_N	AO	USB SS transmit data negative
P39 USB3_HS_DP AI, AO USB HS data positive P40 USB3_HS_DM AI, AO USB HS data negative P41 GND GND Ground P42 GND GND Ground P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SS0_N I/O GPIO45 P45 BISP_SPI1_MOSI I/O GPIO46 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND Ground	P37	USB3_SS_RX_P	Al	USB SS receive data positive
P40 USB3_HS_DM AI, AO USB HS data negative P41 GND GND Ground P42 GND GND Ground P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SS0_N I/O GPIO45 P45 BISP_SPI1_MOSI I/O GPIO46 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND Ground	P38	USB3_SS_RX_N	Al	USB SS receive data negative
P41 GND GND Ground P42 GND GND Ground P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SS0_N I/O GPIO45 P45 BISP_SPI1_MOSI I/O GPIO46 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND Ground	P39	USB3_HS_DP	AI, AO	USB HS data positive
P42 GND GND Ground P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SS0_N I/O GPIO45 P45 BISP_SPI1_MOSI I/O GPIO46 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND Ground	P40	USB3_HS_DM	AI, AO	USB HS data negative
P43 BISP_SPI1_SCK I/O GPIO44 P44 BISP_SPI1_SS0_N I/O GPIO45 P45 BISP_SPI1_MOSI I/O GPIO46 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND Ground	P41	GND	GND	Ground
P44 BISP_SPI1_SS0_N I/O GPIO45 P45 BISP_SPI1_MOSI I/O GPIO46 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND Ground	P42	GND	GND	Ground
P45 BISP_SPI1_MOSI I/O GPIO46 P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND Ground	P43	BISP_SPI1_SCK	I/O	GPIO44
P46 BISP_SPI1_MISO I/O GPIO47 P47 GND GND Ground	P44	BISP_SPI1_SS0_N	I/O	GPIO45
P47 GND GND Ground	P45	BISP_SPI1_MOSI	I/O	GPIO46
	P46	BISP_SPI1_MISO	I/O	GPIO47
P48 GND GND Ground	P47	GND	GND	Ground
	P48	GND	GND	Ground

P49	12V	Al	12V Power Input
P50	12V	Al	12V Power Input

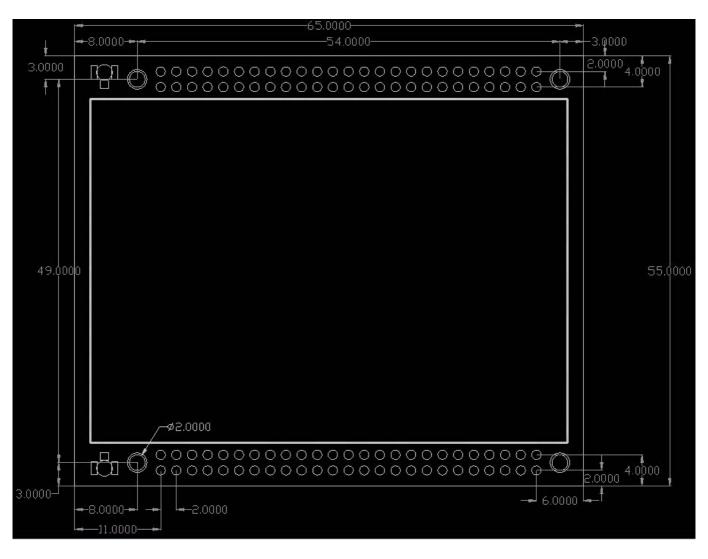
			I
P51	GND	GND	Ground
P52	GND	GND	Ground
P53	SDIO_CD	I/O	GPIO22
P54	SDIO_DATA0	I/O	GPIO23
P55	SDIO_DATA1	I/O	GPIO24
P56	SDIO_DATA2	I/O	GPIO25
P57	SDIO_DATA3	I/O	GPIO26
P58	SDIO_CLK	0	GPIO27
P59	SDIO_CMD	I/O	GPIO28
P60	SDIO_DATA4	I/O	GPIO29
P61	SDIO_DATA5	I/O	GPIO30
P62	SDIO_DATA6	I/O	GPIO31
P63	SDIO_DATA7	I/O	GPIO32
P64	GND	GND	Ground
P65	GND	GND	Ground
P66	GND	GND	Ground
P67	BLSP_I2C0_SCK	I/O	GPIO20
P68	BLSP_I2C0_SDA	I/O	GPIO21
P69	BLSP_I2C1_SCK	I/O	GPIO34
P70	BLSP_I2C1_SDA	I/O	GPIO35
P71	DVDD33	0	3.3V Power Output
P72	GND	GND	Ground
P73	UART0_RXD	1	GPIO16
P74	UART1_RXD	I/O	GPIO9
P75	UART0_TXD	0	GPIO17
P76	UART1_TXD	0	GPIO8
P77	GND	GND	Ground
P78	GND	GND	Ground
P79	WPS_SW_GPIO18	I	GPIO18
P80	CHIP_PWD_L	I	Chip power-on reset

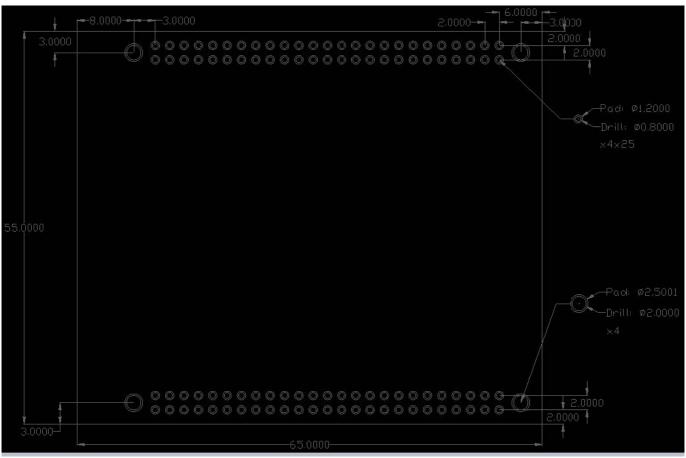
P81	GND	GND	Ground
P82	GND	GND	Ground
P83	GPIO10	I/O	GPIO10
P84	GPIO11	I/O	GPIO11
P85	GPIO36	0	GPIO36
P86	WLAN_ACTIVE	0	GPIO37/Boot

P87	PCIE_RST_N	0	GPIO38
P88	PCIE_CLK_REQ_N	I/O	GPIO39
P89	PCIE_WAKE_L	I/O	GPIO40
P90	GPIO42	I	GPIO42
P91	GPIO43	I	GPIO43
P92	GPIO48	0	GPIO48
P93	GPIO49	I/O	GPIO49
P94	GPIO50	I/O	GPIO50
P95	PCIE_WIFI_STRN_LED	0	GPIO51/BOOT
P96	QPIC_PAD_TE	I/O	GPIO52
P97	P3_1000_LED	I/O	Parallel LED output for 1000BASE-T of PHY3
P98	P4_1000_LED	I/O	Parallel LED output for 1000BASE-T or 1000BASE-X of PHY4
P99	GND	GND	Ground
P100	GND	GND	Ground

Mechanical characteristics

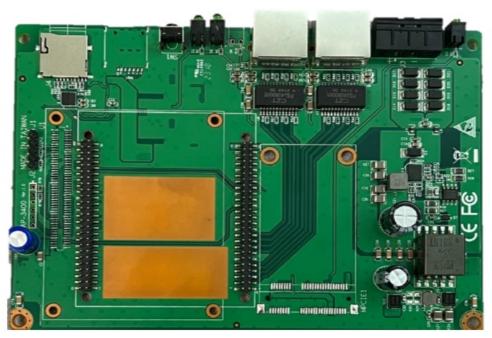
Mechanical drawing





SOM4019 module is easy to implement to your design. User only reserve commonly used pin headers as board-to-board connector to have SOM module integrated to your system. You may run the main program in SOM module while regarding the IO interface deployed in the bottom board. When designing with SOM4019, carefully follow the pin definition above for the power & interfaces connections. The following is SOM4019 together with a bottom board for reference.





This document is subject to change without notice.

Documents / Resources



EMBUX SOM4019 Module with Dual Band Dual Concurrent Wi-Fi [pdf] User Manual SOM4019 Module with Dual Band Dual Concurrent Wi-Fi, SOM4019, Module with Dual Band Dual Concurrent Wi-Fi, Band Dual Concurrent Wi-Fi, Dual Concurrent Wi-Fi, Concurrent Wi-Fi

References

User Manual

Manuals+, Privacy Policy

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