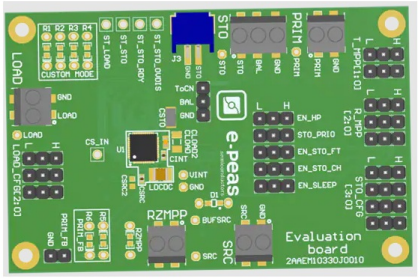

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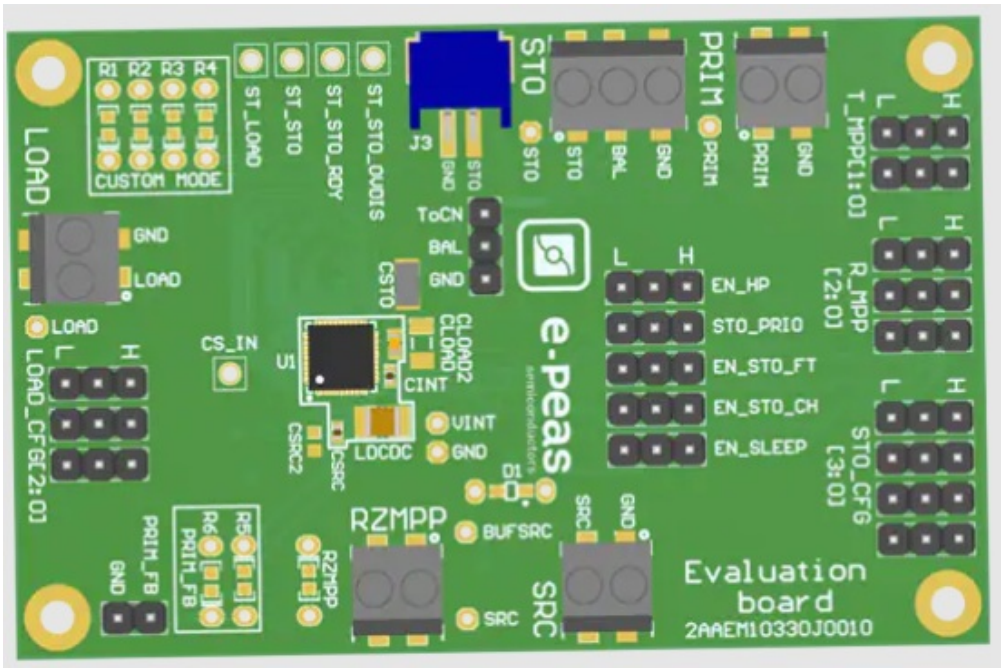


Contents

1 Description
2 Applications
3 Appearance
4 Features
5 Device Information
6 Connections Diagram
7 General Considerations
8 Functional Tests
9 Schematics
10 Documents / Resources
11 Related Posts

Description

The AEM10330 evaluation board is a printed circuit board (PCB) featuring all the needed components to operate the AEM10330 integrated circuit (IC).

The AEM10330 evaluation board allows users to test the epeas IC and analyse its performances in a laboratory-like setting.

It allows easy connections to the energy harvester the storage element. It also provides all the configuration access to set the device in any one of the modes described in the datasheet. The control and status signals are available on standard pin headers, allowing users to wire for any usage scenario and evaluate the relevant performances.

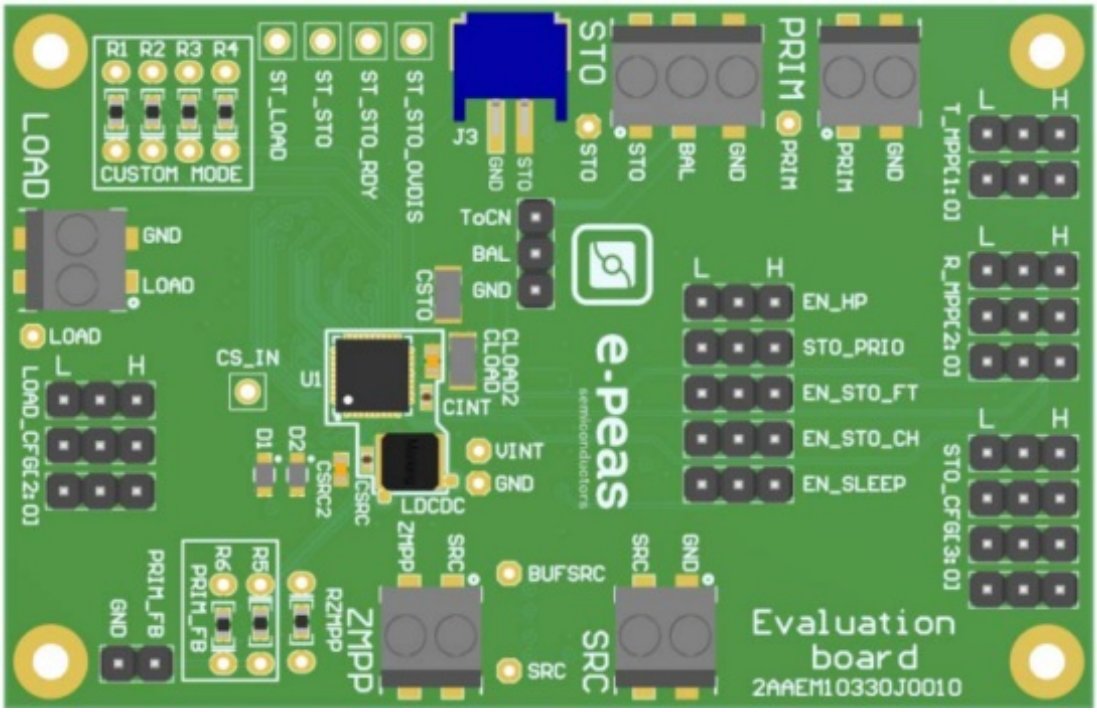
The AEM10330 evaluation board is a plug and play, intuitive and efficient tool for making the appropriate decisions (component selection, operating modes, etc) for the design of a highly efficient subsystem in your target application.

More detailed information about AEM10330 features can be found in the datasheet.

Applications

- Asset Tracking/Monitoring
- Industrial applications
- Retail ESL/Smart sensors
- Aftermarket automotive
- Smart home/building

Appearance



Features

our two-way screw terminals

- Source of energy (DC)
- Load
- ZMPP configuration

One three-way screw terminal

- Energy storage element (battery or (super)capacitor)

One 2-pin “Shrouded Header”

- Alternative connector for the storage element

3-pin headers

- Maximum power point ratio (R_MPP) configuration
- Maximum power point timing (T_MPP) configuration
- Energy storage element threshold configuration
- Load voltage configuration
- Dual-cell super capacitor configuration
- Modes configuration

Provision for seven resistors

- Custom mode configuration

- ZMPP configuration

Configuration by 0 Ohm resistors

- Cold start input configuration

Four 1-pin headers

- Access to status pins

Device Information

Device Information	Device Information
Device Information	Device Information

Connections Diagram

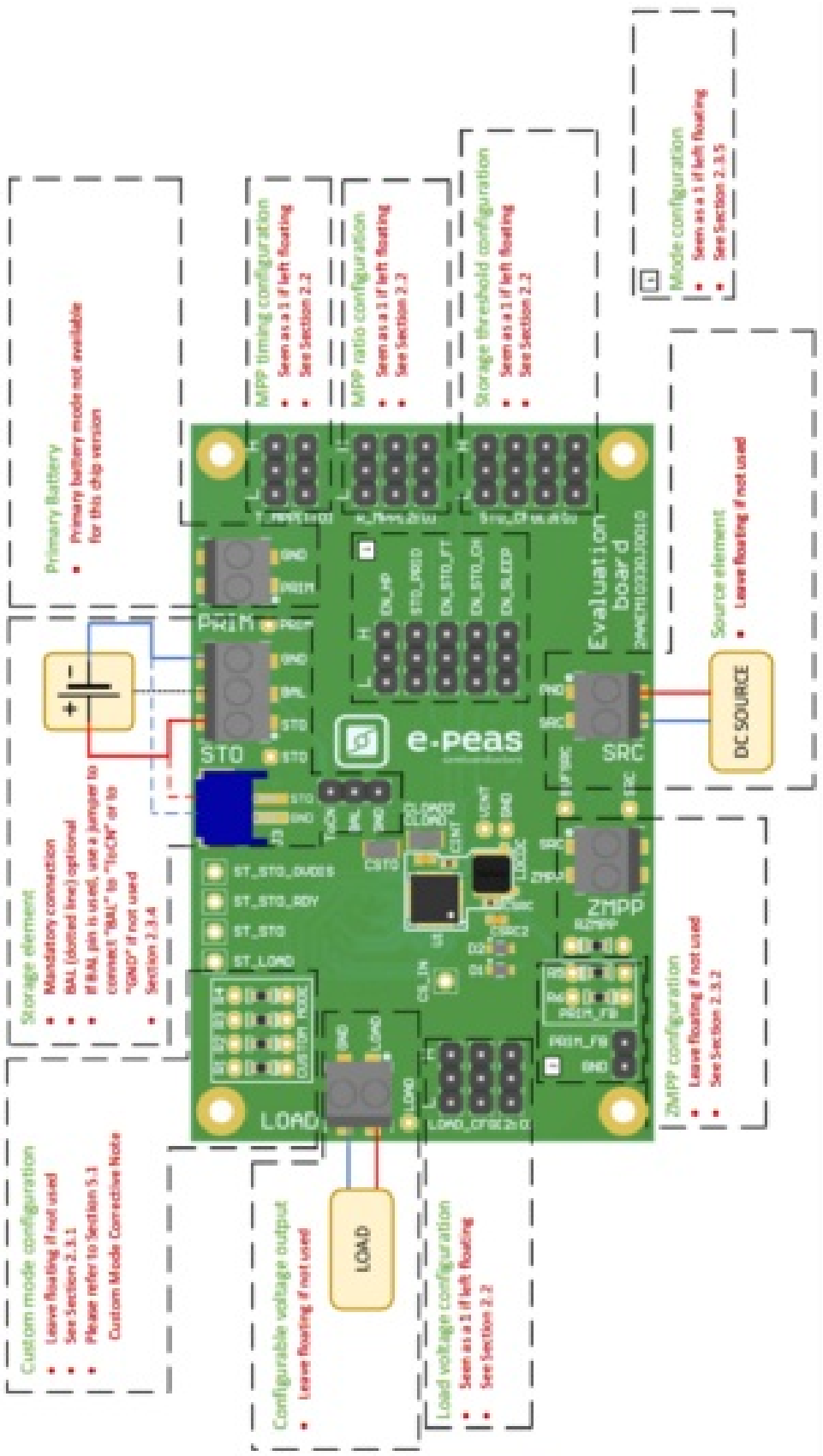


Figure 1: Connection diagram

Signals Description

NAME	FUNCTION	CONNECTION	
		If used	If not used

Power signals			
SRC	Connection to the harvested energy source.	Connect the source element.	
STO	Connection to the energy storage element.	Connect the storage element in addition to CSTO (150 µF).	Do not remove CSTO.
BAL	Connection to balancing of the dual-cell super capacitor.	Connect balancing and place a jumper shorting BAL and “ToCN”.	Use a jumper to connect “BAL” to “GND”.
LOAD	Connection to the load (Application).	Connect a load.	Leave floating.
Debug signals			
VINT	Internal voltage supply.		
BUFSRC	Connection to an external capacitor buffering the buck-boost converter input.		
Configuration signals			
R_MPP[2:0]	Configuration of the MPP ratio.	Connect jumper	Leave floating
T_MPP[1:0]	Configuration of the MPP timing	Connect jumper	Leave floating
STO_CFG[3:0]	Configuration of the threshold voltages for the energy storage element.	Connect jumper	Leave floating
LOAD_CFG[2:0]	Configuration of the load voltage	Connect jumper	
ZMPP	Configuration of the constant impedance MPP	Use resistor RZMPP	Leave floating
Control signals			
EN_HP	Enabling pin for the high-power mode	Connect jumper	
STO_PRIO	Pin for the storage/load priority	Connect jumper	
EN_STO_FT	Enabling pin for the feed-through feature	Connect jumper	
EN_STO_CH	Enabling pin for the storage charging	Connect jumper	
EN_SLEEP	Enabling pin for the sleep mode	Connect jumper	Can’t be left floating
Status signals			

ST_LOAD	Logic output. Asserted when the Load voltage rises above the VLOAD,TYP threshold. Reset when the LOAD voltage drops below VLOAD,MIN threshold. High level is VLOAD.
ST_STO	Logic output. Asserted when the storage device voltage rises above the VCHRDY threshold. Reset when the storage device voltage drops below VOVDIS threshold. High level is VSTO.
ST_STO_RDY	Logic output. Asserted when the storage element is above VCHRDY. High level is VLOAD.
ST_STO_OVDIS	Logic output. Asserted when the storage element voltage VSTO drops below VOVDIS. High level is VLOAD.

General Considerations

Safety Information

Always connect the elements in the following order:

1. Reset the board: Short VINT, LOAD, STO and SRC test points to GND.
2. Completely configure the PCB (Jumpers/resistors);
    - MPP configuration (Ratio/Timing)
    - Battery configuration
    - Load voltage configuration
    - Balancing circuit configuration
    - Mode configuration
3. Connect the storage elements on STO.
4. Connect the Load on LOAD
5. Connect the source (DC or AC) to the SRC connector.

To avoid damaging the board, users are required to follow this procedure. In fact, the pins PRIM_FB, PRIM, BAL and EN_SLEEP cannot remain floating.

Basic Configurations

Configuration pins				Storage element threshold voltages			Typical use
STO_CFG [3]	STO_CFG [2]	STO_CFG[1]	STO_CFG [0]	VOVCH	VCHRD Y	VOVDIS	
0	0	0	0	4.08 V	3.51 V	3.03 V	Li-ion battery
0	0	0	1	3.64 V	3.08 V	2.82 V	LiFePO4 battery
0	0	1	0	2.74 V	2.41 V	1.85 V	NiMH battery
0	0	1	1	4.65 V	1.00 V	0.20 V	Dual-cell supercapacitor
0	1	0	0	2.63 V	1.00 V	0.20V	Single-cell supercapacit or
0	1	0	1	2.99 V	1.20 V	1.00 V	Single-cell supercapacit or
0	1	1	0	2.63 V	2.30 V	1.85 V	NGK
0	1	1	1	Custom Mode			
1	0	0	0	1.49 V	1.25 V	1.1 V	Ni-Cd 1 cells
1	0	0	1	2.99 V	2.50 V	2.22 V	Ni-Cd 2 cells
1	0	1	0	4.65 V	2.00 V	1.49 V	Dual-cell super capacito r
1	0	1	1	2.63 V	1.20 V	1.00 V	Single-cell super capacit or
1	1	0	0	2.63 V	2.30 V	2.00 V	ITEN /Umal Murata
1	1	0	1	4.35 V	3.51 V	3.03 V	Li-Po battery
1	1	1	0	4.00 V	2.70 V	2.60 V	Tadiran TLI1020A
1	1	1	1	3.92 V	3.51 V	2.60 V	Tadiran HLC1020

Table 2: Storage Element Configuration Pins

Configuration pins			MPPT ratio
R_MPP[2]	R_MPP[1]	R_MPP[0]	VMPP / VOC
0	0	0	60%
0	0	1	65%
0	1	0	70%
0	1	1	75%
1	0	0	80%
1	0	1	85%
1	1	0	90%
1	1	1	ZMPP

Table 3: MPP Ratio Configuration Pins

Configuration pins		MPPT timing	
T_MPP[1]	T_MPP[0]	Sampling duration	Sampling period
0	0	5.19 ms	280 ms
0	1	70.8 ms	4.5 s
1	0	280 ms	17.87 s
1	1	1.12 s	71.7 s

Table 4: MPP Timing Configuration Pins

Configuration pins			LOAD output voltage			Use-case
LOAD_CFG[2]	LOAD_CFG[1]	LOAD_CFG[0]	MAX	MID	MIN	TYP
0	0	0	3.34 V	3.23 V	3.15 V	3.28 V
0	0	1	2.53 V	2.47 V	2.35 V	2.50 V
0	1	0	1.82 V	1.75 V	1.64 V	1.79 V
0	1	1	1.23 V	1.16 V	1.14 V	1.20 V
1	0	0	2.63 V	1.56 V	1.39 V	1.61 V
1	0	1	4.65 V	1.56 V	1.39 V	1.61 V
1	1	0	5.13 V	4.88 V	4.76 V	5.00 V

Table 5: Load Configuration Pins

Advanced Configurations

A complete description of the system constraints and configurations is available in Section 8 “System configuration” of the AEM10330 datasheet.
A reminder on how to calculate the configuration resistors value is provided below. Calculation can be made with the help of the spreadsheet found on the e-peas website.

Custom Mode
In addition to the pre-defined protection levels, the custom mode allows users to define their own levels via resistors R1 to R4.

By defining RT = R1 + R2 + R3 + R4 (1 M ≤ RT ≤ 100 M)

- R1 = RT (1 V / VOVCH)
- R2 = RT (1 V / VCHRDY – 1 V / VOVCH)
- R3 = RT (1 V / VOVDIS – 1 V / VCHRDY)
- R4 = RT (1 – 1 V / VOVDIS)

Make sure the protection levels satisfy the following conditions:

- VCHRDY + 0.05 V ≤ VOVCH ≤ 4.5 V
- VOVDIS + 0.05 V ≤ VCHRDY ≤ VOVCH – 0.05 V
- 1 V ≤ VOVDIS

If unused, leave the resistor footprints (R1 to R4) empty.

ZMPP Configuration

If this configuration is chosen (see Table 3), the AEM10330 regulates Vsrc at a voltage equals to the product of RZMPP times the current available at the source SRC.

- 10 Ω ≤ RZMPP ≤ 1 MΩ

If unused, leave the resistor footprint RZMPP empty.

Balancing Circuit Configuration

When using a dual-cell super capacitor (that does not already include a balancing circuit), enable the balun circuit configuration to ensure equal voltage on both cells. To do so:

- Connect the node between the two super capacitor cells to BAL (on STO connector)
- Use a jumper to connect “BAL” to “ToCN”

If unused, use a jumper to connect “BAL” to “GND”

Mode Configuration

- **EN_HP**
  When EN_HP is pulled up to VINT, the DCDC converter is set to HIGH POWER MODE. This allows higher

currents to be extracted from the buck-boost input (SRC) to the buck-boost output (STO or VINT).

- Use a jumper to connect EN_HP to 1 to enable the high-power mode.
- Use a jumper to connect EN_HP to 0 to disable the high-power mode.

STO_PRIO
It is possible to define a priority between STO and LOAD.

- Use a jumper to connect the STO_PRIO to 1 to supply the storage element to VCHRDY before start supplying the LOAD.
- Use a jumper to connect the STO_PRIO to 0 to supply in the first place the LOAD, charging the storage element with the remaining energy.

EN_STO_CH
To disable battery charging, the 3-pin header is available.

- Use a jumper to connect the EN_STO_CH to 1 to enable the charge of the storage element
- Use a jumper to connect the EN_STO_CH to 0 to disable the charge of the storage element

EN_SLEEP
The SLEEP STATE reduces the AEM10330 quiescent current by no longer extracting energy from the SRC and reducing VLOAD and VVINT monitoring period.

- Use a jumper to connect the EN_SLEEP to 1 to activate the feature.
- Use a jumper to connect the EN_SLEEP to 0 to disable the feature.

Do not leave EN_SLEEP floating, you risk damaging the AEM

EN_STO_FT
To disable the source to storage element feed-through, the 3- pin header is available.

- Use a jumper to connect the EN_STO_FT to 1 to activate the feature.
- Use a jumper to connect the EN_STO_FT to 0 to disable the feature.

Functional Tests

This section presents a few simple tests that allow the user to understand the functional behavior of the AEM10330. To avoid damaging the board, follow the procedure found in Section 2.1 “Safety Information”. If a test has to be restarted make sure to properly reset the system to obtain reproducible results.

The following functional tests were made using the following setup:

- Configuration: R_MPP[2:0] = LLL, T_MPP[1:0] = LH, STO_CFG[3:0] = LLLL, EN_HP = H, STO_PRIO = H, EN_STO_FT = L, EN_STO_CH = H, EN_SLEEP = L, EN_STO_FT = L
- Storage element: Capacitor (4.7 mF + CSTO)
- **Load:** 10kOhm on LOAD
- **SRC:** current source (1mA or 100uA) with voltage compliance (4V)

The user can adapt the setup to match your system as long as you respect the input and cold-start constraints (see Section 1 “Introduction” of AEM10330 datasheet).

Start-up

The following example allows the user to observe the behavior of the AEM10330 in the Wake-up state.

Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”.

Observations and measurements

- **STO:** Voltage rises as the power provided by the source is transferred to the storage element
- **LOAD:** Regulated when voltage on STO first rises above VCHRDY.
- **ST_STO** and ST_STO_RDY: Asserted when the voltage on STO rises above VCHRDY.
- **ST_LOAD:** Asserted when LOAD is supplied.

Shutdown

This test allows users to observe the behavior of the AEM10330 when the system is running out of energy.

Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1). Do not use a primary battery.
- Let the system reach a steady state (i.e. voltage on STO between VCHRDY and VOVCH and ST_STO asserted.
- Remove your source element and let the system discharge through quiescent current and load.

Observations and measurements

- **STO:** Voltage decreases as the system consumes the power accumulated in the storage element. The voltage reaches VOVDIS.
- **ST_STO_RDY:** De-asserted when the voltage on STO goes below VCHRDY.
  ST_STO: De-asserted when the storage element is running out of energy (VOVDIS).
- **ST_LOAD:** De-asserted when the load is no longer available.
- **ST_STO_OVDIS:** Asserted for 600 ms when the storage element voltage (STO) falls below VOVDIS.

Cold start

The following test allows the user to observe the minimum voltage required to cold start the AEM10330. To prevent leakage current induced by the probe the user should avoid probing any unnecessary node. Make sure to properly reset the board to observe the cold-start behavior.

Setup

- Place the probes on the nodes to be observed.
- Referring Figure 1, follow steps 1 and 2 explained . Configure the board in the desired state. Do not plug any storage element in addition to CSTO.
- **SRC:** Connect your source element.

Observations and measurements

- **SRC:** Equal to the cold-start voltage during the cold start phase. Regulated at the selected MPPT percentage of Voc when cold start is over. Be careful that the cold-start phase time will shorten with the input power. Limit it to ease the observation.
- **STO:** Starts to charge the storage element when the cold-start phase is over.

Dual-cell super capacitor balancing circuit

This test allows users to observe the balancing circuit behavior that maintains the voltage on BAL equilibrated.

Setup

- Following steps 1 and 2 explained in Section 2.1 and referring to Figure 1, configure the board in the desired state. Plug the jumper linking “BAL” to “ToCN”.
- **STO:** Plug capacitor C1 between the positive (+) and the BAL pins and a capacitor C2 between BAL and the negative (-) pins. Select C1 ≠ C2 such that:
- C1 & C2 > 1mF
- (C2 * VCHRDY)/C1 ≥ 0.9V
- SRC: Plug your source element to start the power flow to the system.

Observations and measurements

- **BAL:** Equal to half the voltage on STO

Do not leave BAL floating, you risk damaging the AEM

Source to Storage Element Feed

Through

This example allows users to observe the feed-through feature.

Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system.

- Let the system reach a steady state (i.e. voltage on STO between VCHRDY and VOVCH and ST_STO asserted.
- **EN_STO_FT:** Connect to H
- **SRC:** current source (1mA or 100uA) with voltage compliance (5V)
- Put a capacitor (>1mF) on SRC and STO to avoid perturbation due to the SMU behavior.

Observations and measurements

- **STO:** The current from the source is transferred directly to the storage element.

Schematics

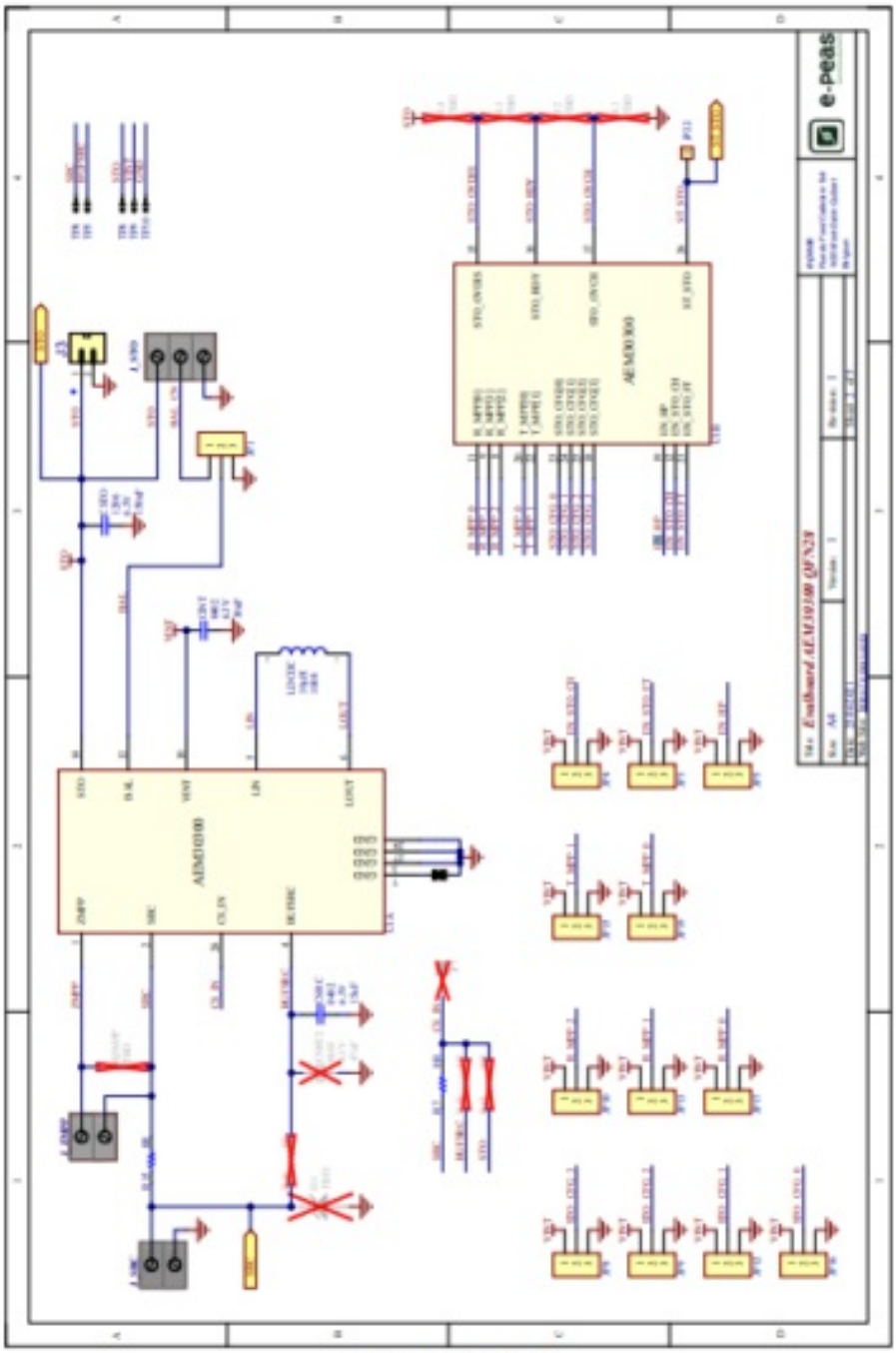


Figure 2: Schematic part 1

Documents / Resources

	e-peas AEM10330 Evaluation Board Printed Circuit Board [pdf] User Guide AEM10330, Evaluation Board Printed Circuit Board