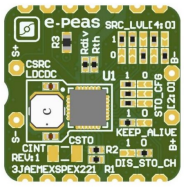

e-peas AEM00901 Stamp Module User Guide

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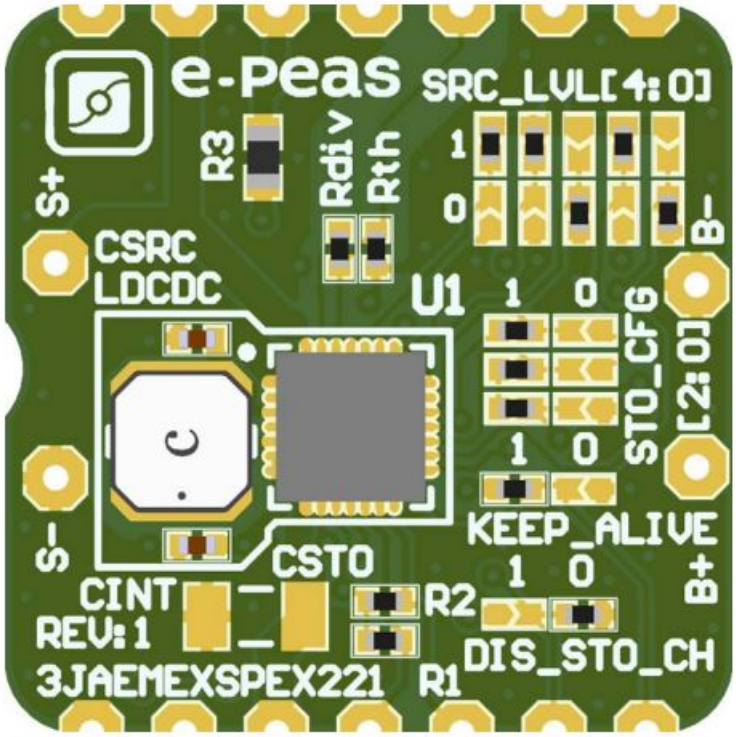
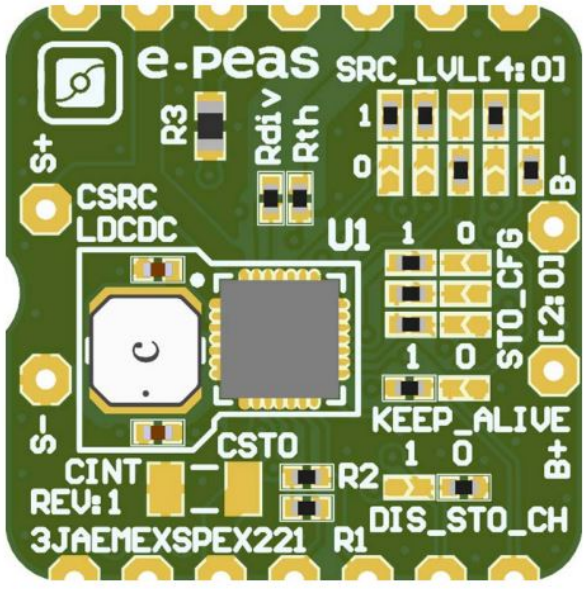


Description

The AEM00901 evaluation kit (EVK) is a printed circuit board (PCB) featuring all the required components to operate the AEM00901 integrated circuit (IC).
The AEM00901 evaluation board allows user to test the e-peas IC and analyse its performances in a laboratory-like setting or in product mock-ups.
It allows easy connections to an energy harvester (e.g. a single element PV cell) and a storage element. It also provides all the configuration access to set the device in any of the modes described in the datasheet at the exception of SRC_LVL_CFG[5], which has been tied to ground. The control and status signals are available on pads or through an I²C bus communication, allowing user to over-ride preconfigured board settings through host MCU and evaluate the IC performances.
The AEM00901 EVK is a plug and play, intuitive and efficient tool to optimize the AEM00901 configuration, allowing user to design a highly efficient subsystem for the desired target application. Component replacement and operating mode switching is convenient and easy.
More detailed information about AEM00901 features can be found in the datasheet.

Appearance



Features

Key features

- Very high efficiency conversion from single element PV
- Very low BOM
- Very small footprint
- Ready to use without MCU interaction
- Optional configuration through I²C
- Thermal monitoring

Breakout solder pads

- Connection to DC source of energy (PV)
- Connection to storage element
- AEM Internal voltage
- Temperature monitoring
- Reset
- I²C slave (address 0x41)
- Configuration

Additional two solder pads

- Connection to DC source of energy (PV)
- Connection to storage element

20 solder bridges and one resistor

- ZMPP configuration
- Constant source voltage (SRC_LVL_CFG) configuration
- Energy storage element threshold configuration
- Mode configuration

Applications

- **Wearable Electronics** Keyboards
- **Remote Control Units** Electronic Shelf Labels
- **Smart Buildings** Indoor Sensors

Device Information

Part Number	Dimensions
3JAEMEXSPEX221 REV:1	20 mm x 20 mm

Connections Diagram

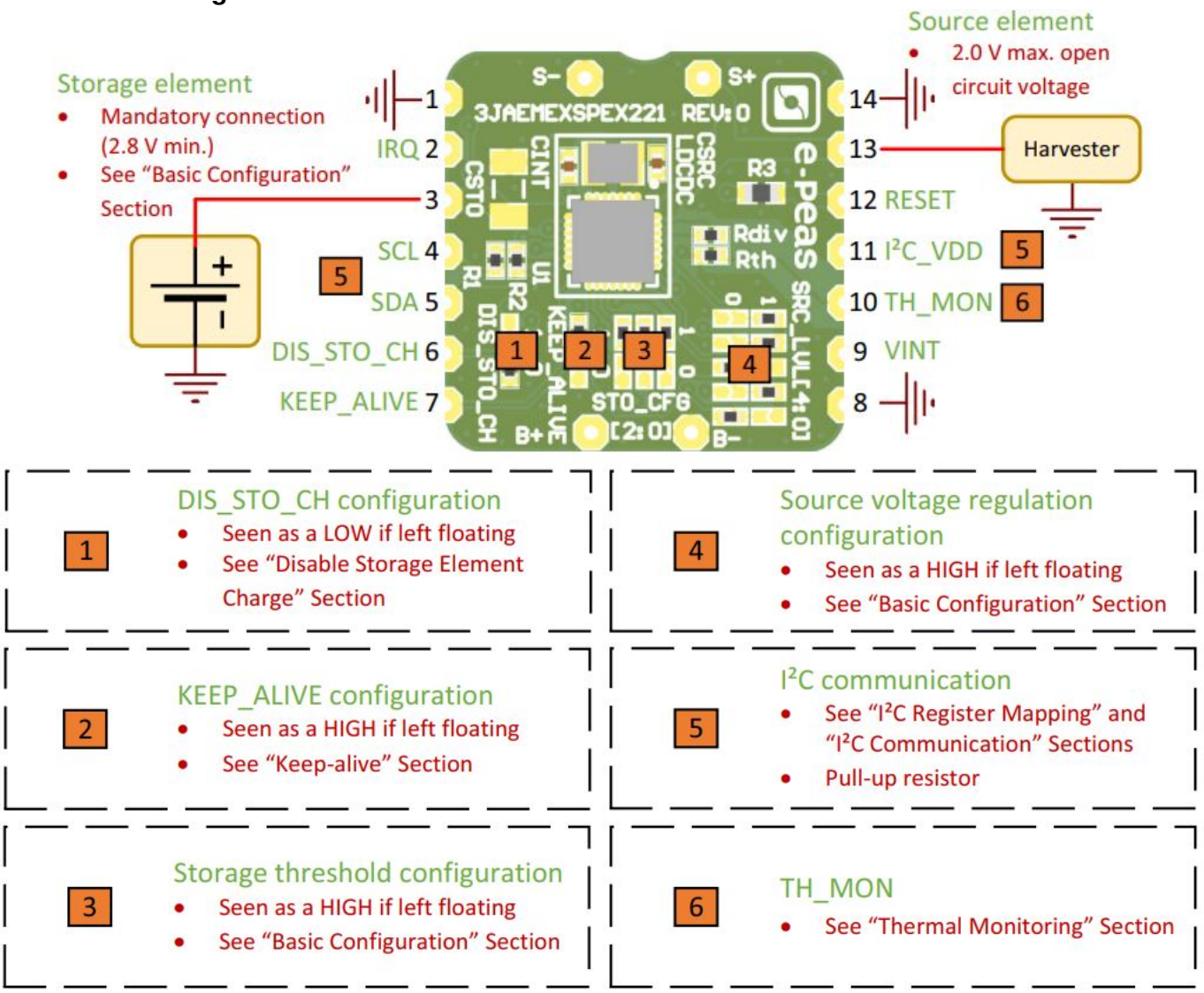


Figure 1: Connection diagram

Signals Description

NAME	FUNCTION	CONNECTION	
		If used	**If not used**
Power signals			
SRC	Connection to the harvested energy source.	Connect the source element.	Can be left floating.
STO	Connection to the energy sto rage element.	Cannot be left floating, voltage must always be above 2.8 V.	
I²C _VDD	Connection to I²C voltage su pply	Connect to I²C supply.	Connect to GND.
VINT	AEM Internal voltage supply.		
BUFSRC	AEM connection to a capacit or buffering the boost convert er input (no connector on EV K).		
Configuration signals			
SRC_LVL_CFG[5:0]	Used for the configuration of the source voltage level.	Connect solder bridge.	Read as high if left floating.
STO_CFG[2:0]	Configuration of the threshol d voltages for the energy stor age element.	Connect solder bridge.	Read as high if left floating.
TH_MON	Configuration of the thermal monitoring	Connect a thermistor.	Connect to VINT.
Control signals			
DIS_STO_CH	Disabling pin for the storage charging	Connect solder bridge.	Read as low if left floating.
KEEP_ALIVE	Enabling pin to supply intern al circuitry from the storage e lement if no power on SRC	Connect solder bridge.	Read as high if left floating.
I²C signals			
SDA	Bidirectional data line	Connect to host I²C bus.	Connect to I²C _VDD to GND (SDA and SCL will be pulled down by R1 and R2).
SCL	Unidirectional serial clock		
IRQ	Interrupt request	Connect to host GPIO.	Leave floating.

General Considerations

Safety Information

Always connect the elements in the following order:

1. Reset the board: do the following in this particular order:

- Disconnect the harvester from SRC.
- Short BUFSRC to GND.
- Short VINT to GND.

2. Completely configure the PCB (jumpers/resistors):
    - Battery configuration.
    - Mode configuration.
    - Thermal monitoring configuration.
3. Connect I2C_VDD:
    - To GND if I²C is not used (SDA and SCL will also be connected to GND through their pull up resistors).
    - To a power supply if I²C is used (1.5 V to 2.2 V).
4. Connect the storage elements on STO with a voltage higher than 2.8V.
5. Connect the source to the SRC connector (open circuit voltage lower than 2.0 V).

Basic Configurations
On the Stamp Module, the MSB of the SRC_LVL_CFG[5:0] pins has been tied to ground.

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0]						VSRC,REG
0	0	0	1	1	0	0.12 V
0	0	0	1	1	1	0.13 V
0	0	1	0	0	0	0.15 V
0	0	1	0	0	1	0.16 V
0	0	1	0	1	0	0.18 V
0	0	1	0	1	1	0.19 V
0	0	1	1	0	0	0.21 V
0	0	1	1	0	1	0.22 V
0	0	1	1	1	0	0.24 V
0	0	1	1	1	1	0.25 V
0	1	0	0	0	0	0.27 V
0	1	0	0	0	1	0.28V
0	1	0	0	1	0	0.30 V
0	1	0	0	1	1	0.33 V
0	1	0	1	0	0	0.36 V
0	1	0	1	0	1	0.39 V
0	1	0	1	1	0	0.42 V
0	1	0	1	1	1	0.45 V
0	1	1	0	0	0	0.48 V
0	1	1	0	0	1	0.51 V
0	1	1	0	1	0	0.54 V
0	1	1	0	1	1	0.57 V
0	1	1	1	0	0	0.60 V
0	1	1	1	0	1	0.63 V
0	1	1	1	1	0	0.66 V
0	1	1	1	1	1	0.69 V

Table 2: Configuration of SRC_LVL_CFG[5:0]

Configuration	Availability Through Pins		Storage element threshold voltage	
CFG[2:0]	I²C Interface	Configuration pins	Vovch	Vovdis
000	yes	yes	4.50 V	3.30 V
001	yes	yes	4.00 V	2.80 V
010	yes	yes	3.63 V	2.80 V
011	yes	yes	3.90 V	2.80 V
100	yes	yes	3.90 V	3.50 V
101	yes	yes	3.90 V	3.01 V
110	yes	yes	4.35 V	3.01 V
111	yes	yes	4.12 V	3.01 V

Table 3: Usage of CFG[2:0]

I²C Register Map

Address	Name	Bit	Field Name	Access	RESET	Description
0x00	VERSION	[3:0]	MINOR	R	–	Chip ID
		[7:4]	MAJOR	R	–	
0x01	SRCREGU	[6:0]	VALUE	R/W	0x77 (1.47 V)	Source voltage regulation
0x02	VOVDIS	[5:0]	THRESH	R/W	0x2D (3.05 V)	Overdischarge level of the storage element
0x03	VOVCH	[5:0]	THRESH	R/W	0x33 (4.1V)	Overcharge level of the storage element
0x04	TEMPCOLD	[7:0]	THRESH	R/W	0x8F (0°C)	Cold temperature level
0x05	TEMPHOT	[7:0]	THRESH	R/W	0x2F (45°C)	Hot temperature level
0x06	PWR	[0:0]	KEEPALEN	R/W	0x01	Keepalive enable
		[1:1]	HPEN	R/W	0x01	AEM00900: High power mode enable AEM00901: Reserved
		[2:2]	TMONEN	R/W	0x01	Temperature monitoring enable
		[3:3]	STOCHDIS	R/W	0x00	Battery charging disable

0x07	SLEEP	[0:0]	EN	R/W	0x01	Sleep mode enable
0x08	STOMON	[2:0]	RATE	R/W	0x00	ADC rate
0x09	APM	[0:0]	EN	R/W	0x00	APM enable
		[1:1]	MODE	R/W	0x00	APM mode
		[3:2]	WINDOW	R/W	0x00	APM computation window
0x0A	IRQEN	[0:0]	I2CRDY	R/W	0x01	IRQ serial interface ready enable
		[1:1]	VOVDIS	R/W	0x00	IRQ STO OVDIS enable
		[2:2]	VOVCH	R/W	0x00	IRQ STO OVCH enable
		[3:3]	SLPTHRESH	R/W	0x00	IRQ SRC LOW enable
		[4:4]	TEMP	R/W	0x00	IRQ temperature enable
		[5:5]	APMDONE	R/W	0x00	IRQ APM done enable
0x0B	CTRL	[0:0]	UPDATE	R/W	0x00	Load I²C registers configuration
		[2:2]	SYNCBUSY	R	0x00	Synchronization busy flag
0x0C	IRQFLG	[0:0]	I2CRDY	R	0x00	IRQ serial interface ready flag
		[1:1]	VOVDIS	R	0x00	IRQ STOR OVDIS flag
		[2:2]	VOVCH	R	0x00	IRQ STOR OVCH flag
		[3:3]	SLPTHRESH	R	0x00	IRQ SRC LOW flag
		[4:4]	TEMP	R	0x00	IRQ temperature flag
		[5:5]	APMDONE	R	0x00	IRQ APM done flag
0x0D	STATUS	[1:1]	VOVDIS	R	0x00	Status STO OVDIS
		[2:2]	VOVCH	R	0x00	Status STO OVCH
		[3:3]	SLPTHRESH	R	0x00	Status SRC LOW
		[4:4]	TEMP	R	0x00	Status temperature
		[6:6]	CHARGE	R	0x00	Status STO CH
0x0E	APM0	[7:0]	DATA	R	0x00	APM data 0
0x0F	APM1	[7:0]	DATA	R	0x00	APM data 1
0x10	APM2	[7:0]	DATA	R	0x00	APM data 2
0x11	TEMP	[7:0]	DATA	R	0x00	Temperature data
0x12	STO	[7:0]	DATA	R	0x00	Battery voltage
0x13	SRC	[7:0]	DATA	R	0x00	SRC ADC value

Table 4: Register summary

I²C Communication

The device address on the I²C bus is 0x41. All information about the I²C communication is available in the AEM00901 datasheet in the “System configuration” Section.
I2C_VDD must be connected to an external power supply which voltage is within the 1.5 V to 2.2 V range. On the Stamp Module, 1 kΩ pull-up on SDA and SCL (R1 and R2) to I2C_VDD are provided.
In case the configurations are set by I²C communication, the configuration pins will not be taken into account anymore.

Advanced Configurations
A complete description of the system constraints and configurations is available in Section “System configuration” of the AEM00901 datasheet.

Mode Configuration
DIS_STO_CH
Enabling/disabling battery charging can be done by setting a solder bridge on the corresponding pad.

- Use a solder bridge to connect the DIS_STO_CH to STO to disable the charge of the storage element
- Use a solder bridge to connect the DIS_STO_CH to GND to enable the charge of the storage element

KEEP_ALIVE
The KEEP_ALIVE feature allows to supply the internal circuitry from the storage element when no power is available on the source terminal.

- Use a solder bridge to connect the KEEP_ALIVE to H to enable the feature
- Use a solder bridge to connect the KEEP_ALIVE to L to disable the feature

Thermal monitoring
The thermal monitoring feature protects the battery by disabling the battery charging when ambient temperature is outside a specified range. The higher and lower thresholds are configurable using the I²C communication (see datasheet).

- Thermal monitoring is enabled by default on the Stamp Module. To disable it, user must connect “TH_MON” (pin 10, see Figure 1) to VINT (pin 9) externally.

Functional Tests

NOTE: Out of the box testing below can be done without any modification of the Stamp Module.
This section presents a few simple tests that allow user to understand the functional behaviour of the AEM00901. To avoid damaging the board, follow the procedure found in Section 2.1 “Safety Information”. If a test has to be restarted, make sure to properly reset the system to obtain reproducible results.
The measurements use the following equipment:

- Two Source Measurement Units (SMU, fourquadrant power supply)
- One 2-channel oscilloscope

The following functional tests were made using the following setup:

- Default configuration of the Stamp Module:
- SRC_LVL_CFG[5:0] = (L)HHLHL (0.54 V).
- STO_CFG[2:0] = HHH (3.01 V – 4.12 V).
- DIS_STO_CH = L.

- KEEP_ALIVE = H.
- Thermal Monitoring is enabled by default.
- Place a solder bridge to connect I²C _VDD and GND if the I²C communication is not used.

User can adapt the setup to match the use case system as long as the input limitations are respected, as well as the minimum storage voltage and cold-start constraints (see “Introduction” Section of AEM00901 datasheet).

Start-up
The following example allows the user to observe the start-up behaviour of the AEM00901.

Setup

- Place oscilloscope probes on VINT and STO.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”.
- STO: SMU set as a 3.0 V voltage source with 1 mA current compliance.
- SRC: SMU set as a 1 mA or 100 µA current source with 0.8 V voltage compliance.

Observations and measurements

- VINT: voltage rises to 2.2 V
- STO: observe the current absorbed by the SMU as power is transferred from SRC to STO.

Shutdown
This test allows user to observe the behaviour of the AEM00901 when the system is running out of energy. This test is to be done when the AEM00901 already started, as at the end of the test described in Section 3.1.

Setup

- Disable the KEEP_ALIVE feature (KEEP_ALIVE = L).
- Place the oscilloscope probe on VINT.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1).
- Disconnect the SMU from SRC.

Observations and measurements

- **VINT:** voltage falls to GND
- **STO:** no leakage from STO (probe impedance considered)

Cold start
The following test allows user to observe the minimum voltage required to coldstart the AEM00901. To prevent current leakage caused by the probe impedance, user should avoid probing any unnecessary node. Make sure to properly reset the board to observe the cold-start behaviour.

Setup

- Place oscilloscope probe on SRC.
- Referring Figure 1, follow steps 1 to 3 explained in Section 2.1.
- SRC: SMU set as 20 µA current source with 0.3 V voltage compliance.
- STO: SMU as 3.0 V voltage source with 100 µA current compliance.

Observations and measurements

- SRC voltage clamped at the cold-start voltage during the cold-start phase and then regulated at the selected source voltage when cold start is over. The duration of the cold-start phase decreases as the input power increases. Select the input power accordingly to be able to observe the cold-start phase.
- STO: SMU starts absorbing current sourced by the STO pin once the cold-start phase is completed.

Thermal monitoring
The following test allows user to observe the thermal monitoring functionality.

Setup

- Place a 10 kΩ NTC thermistor with β = 3380 on Rth.
- Place a 22 kΩ pullup resistor on RDIV.
- Place the jumper to connect TH_MON with THERM.
- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 as explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1).

Observations and measurements

- If the temperature is lower than 0°C, the charge of the storage element is disabled.
- If the temperature is higher than 45°C, the charge of the storage element is disabled.
- If the temperature is between 0°C and 45°C, the charge of the storage element is enabled.

Keep-alive
The KEEP_ALIVE feature sets the behaviour of the AEM00901 when no power is available on SRC.

Setup

- Place the oscilloscope probe on VINT.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1).
- Enable the KEEP_ALIVE feature (connect KEEP_ALIVE to H).
- Disconnect the SMU from the SRC pin.

Observations and measurements

- **VINT:** the internal circuitry is supplied by the storage element (VVINT does not drop).

Disable Storage Element Charge
To disable battery charging, the 3-pin header is available.

- Use a solder bridge to connect DIS_STO_CH to L to enable the charge of the storage element
- Use a solder bridge to connect DIS_STO_CH to H to disable the charge of the storage element

I²C Communication
This test allows user to change a configuration through the I²C communication.

Setup

- Place the oscilloscope probe on SRC.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1).
- Connect I²C _VDD to the I²C supply (between 1.8 V and 2.2 V).
- Write ‘0010 0011’ (0x23) on the SRCREGU register (0x01), so that constant source voltage is set to 0.285 V)
- Write ‘1’ to the CTRL register (0x0B) to load the I²C register configuration (at startup the AEM00901 load its configuration from the pins settings).

Observations and measurements

- **SRC:** observe that the voltage regulation switches from 0.54 V to 0.285 V, when the register value is loaded.

Efficiency
This test allows user to reproduce the efficiency graphs of the boost converter (see “DCDC Conversion Efficiency” Section if the AEM00901 datasheet).

Setup

- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1).
- **STO:** connect SMU configured as a 4.7 V voltage source with a 100 mA current compliance.
- **SRC:** connect SMU configured as a source current with a voltage compliance of 1.0 V to ensure the AEM00901 coldstarts.

Manipulations

- **STO:** set the SMU to the desired voltage, between VOVDIS and VOVCH. Make sure the SMU integration time is as long as possible.
- **SRC:** sweep the source level voltage by either changing the SRC_LVL_CFG[5:0] pins connections (solder bridge) or by writing the SRCREGU register by I²C communication.

Observations and measurements

- For each data point of the SRC voltage sweep, note the SRC SMU voltage and current, as well as the STO SMU voltage and current. Repeat the measurement for each data point a copious number of times to ensure

capturing current peaks.

- The efficiency η in percent is computed by applying the following formula:

$$\eta = 100 \cdot \frac{V_{STO} \cdot I_{STO}}{V_{SRC} \cdot I_{SRC}}$$

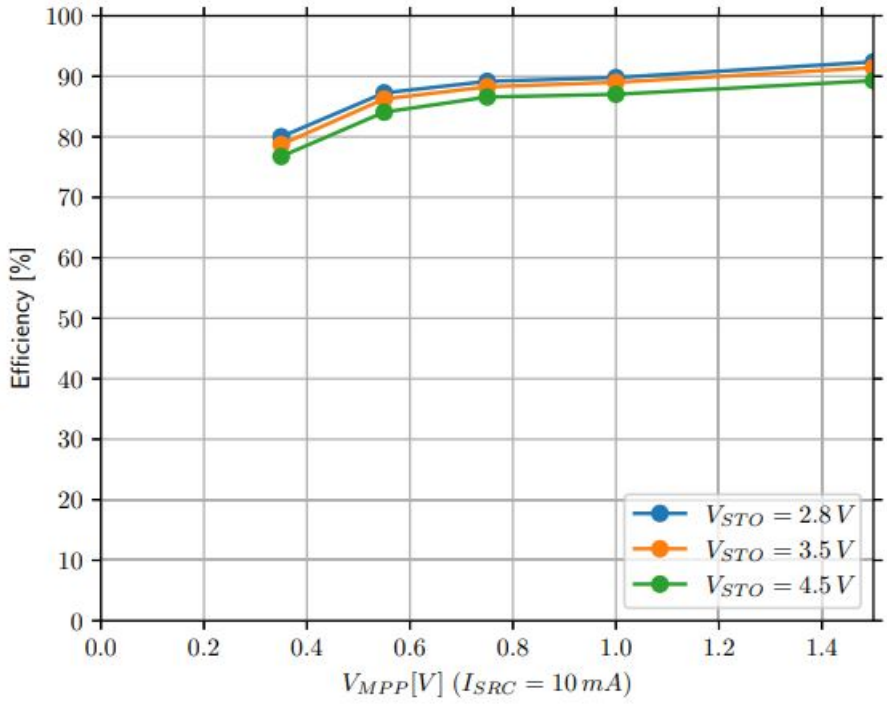


Figure 2: AEM00901 efficiency (preliminary measurements)

Schematics

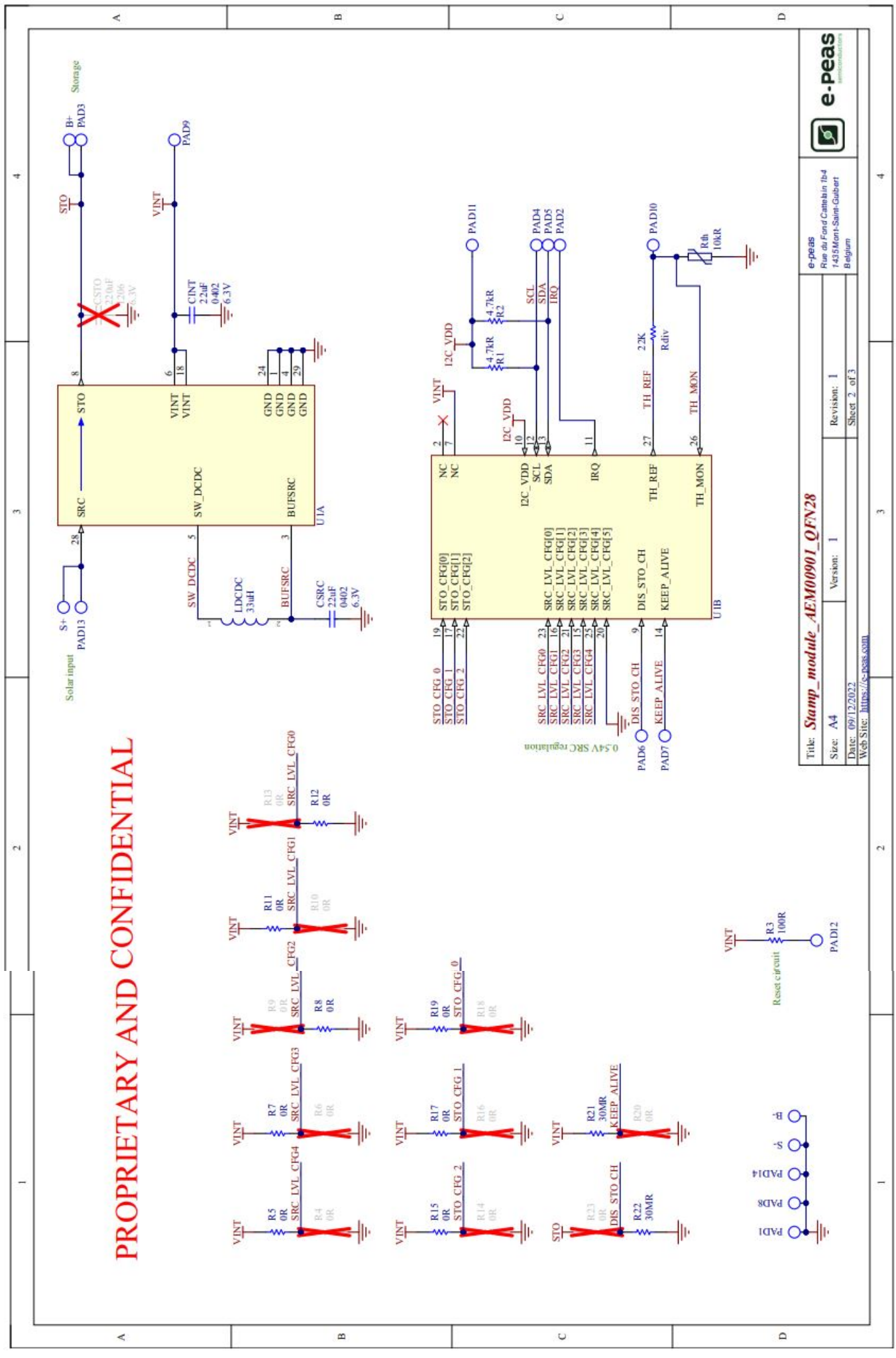

PROPRIETARY AND CONFIDENTIAL
Title: Stamp_module_AEM00901_QFN28
Size: A4
Version: 1
Revision: 1
Date: 09/12/2022
Sheet 2 of 3
Web Site: https://e-peas.com
e-peas
Rue du Fond Cattelain 1b4
1435 Mont-Saint-Guibert
Belgium
Storage
Solar input
0.54V SRC regulation
Reset circuit
U1A
U1B
LDCDC 33uH
CSRC 22uF 0402 6.3V
CINT 2.2uF 0402 6.3V
CSTO 220uF 2066 6.3V
I2C_VDD
4.7kR
2.2K
Rdiv
Rth 10kR
SRC_LVL_CFG0
SRC_LVL_CFG1
SRC_LVL_CFG2
SRC_LVL_CFG3
SRC_LVL_CFG4
STO_CFG_0
STO_CFG_1
STO_CFG_2
DIS_STO_CH
KEEP_ALIVE
30MR
100R

Figure 3: Schematic

Documents / Resources

	e-peas AEM00901 Stamp Module [pdf] User Guide 3JAEMEXSPEX221 REV 1, AEM00901 Stamp Module, AEM00901, AEM00901 Module, Stamp Module, Module