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dialog SEMICONDUCTOR DA14AVDDECT SF01 Wireless Module

General Description

The DA14AVDDECT from Dialog Semiconductor is a member of the wireless module family that operates in the interference-free DECT frequency band (1.9 GHz) and can be used in hosted or embedded Audio, Voice, and Data applications. The module includes all the required radio components, antenna, a low-power audio CODEC (DA7218), and a 32 Mb FLASH memory. The module is intended for users who are familiar with application-level software programming but does not require detailed understanding of the DECT protocol to facilitate rapid design-in cycles. The module can be operated as a stand-alone device or from a host through an API interface.
The module is based on Dialog's DA14495 chip that supports DQPSK and D8PSK besides the traditional GFSK. This increases the raw air data rate by up to three times.
The module is available with 1.5 mm pitch BGA solder balls for an excellent solderability and sufficient connectivity. The dimensions for the module are 17.0 mm × 26.65 mm.
This document describes the hardware of the DA14AVDDECT module. A separate document details the software and APIs.

Key Features

- All RF components are integrated, thus no customer tuning is required
- Supported bands include EU-DECT, DECT 6.0 for North America, and Japan DECT (JDECT)
- On-PCB antenna, the module also supports an optional second external antenna)
- Integrated RF shield
- Low power operations
- Audio bandwidth from 20 Hz to 20 kHz
- 32 Mbit FLASH, so program memory available for custom software

- Integrated audio ADC/DAC (external audio ADC/DAC supported through GPIO mapping)
- Limited modular approval for EN301-406 (EU-DECT), FCC Part 15 (DECT 6.0), and TELEC (J-DECT)
- Supports NiMH, alkaline, and Li-Ion batteries
- A Voice Data Stack or an Audio Data Stack are available to be downloaded

Applications (Defined by SW)

- Public Address solution with four microphones
- Tour Guide Systems for up to 1024 listeners
- Conferencing Systems with eight participants
- Wireless Intercom Systems supporting HD Voice
- Wireless Stereo Headphones and Headsets
- Wireless Low Latency Microphones

System Diagram

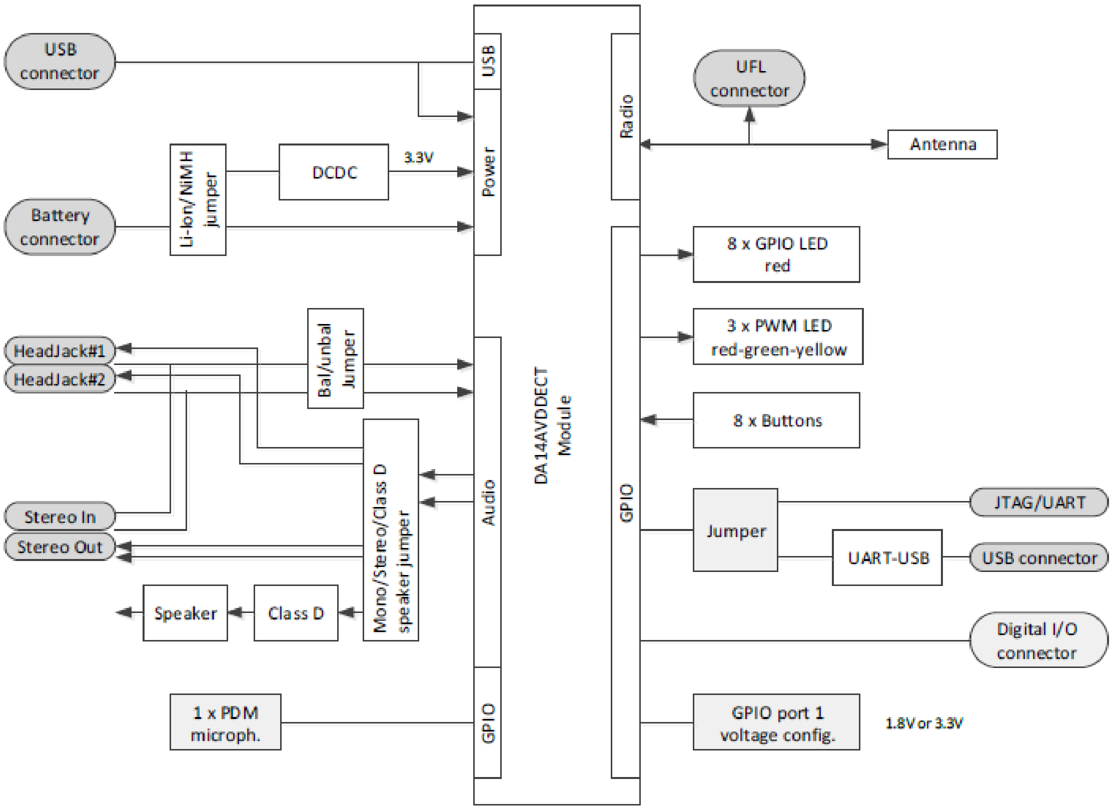


Figure 1: System Diagram

Block Diagram

The DA14AVDDECT module is built around Dialog's DA14495 DECT chip. The module integrates the RF components (that is, baluns, switches, RFPA, and crystal) with an integrated antenna. It also allows an additional external antenna to be connected in order to support antenna diversity.

A low-power audio CODEC from Dialog (DA7218) is integrated to support analog audio applications. A 32-Mb FLASH is integrated for custom software.

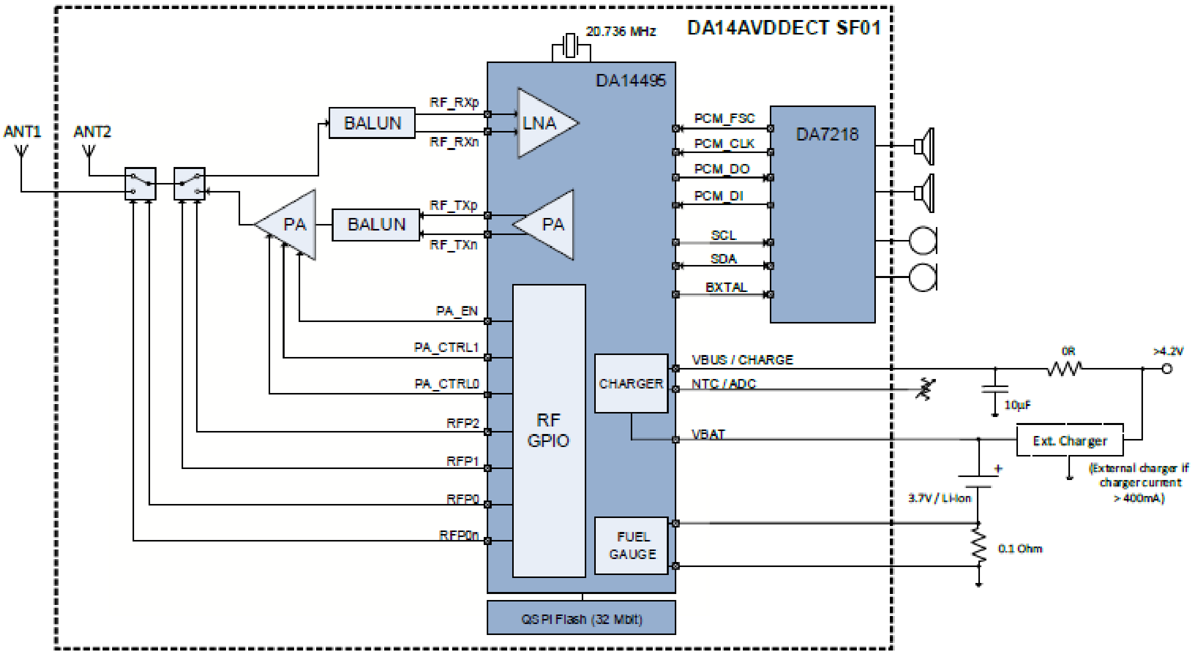
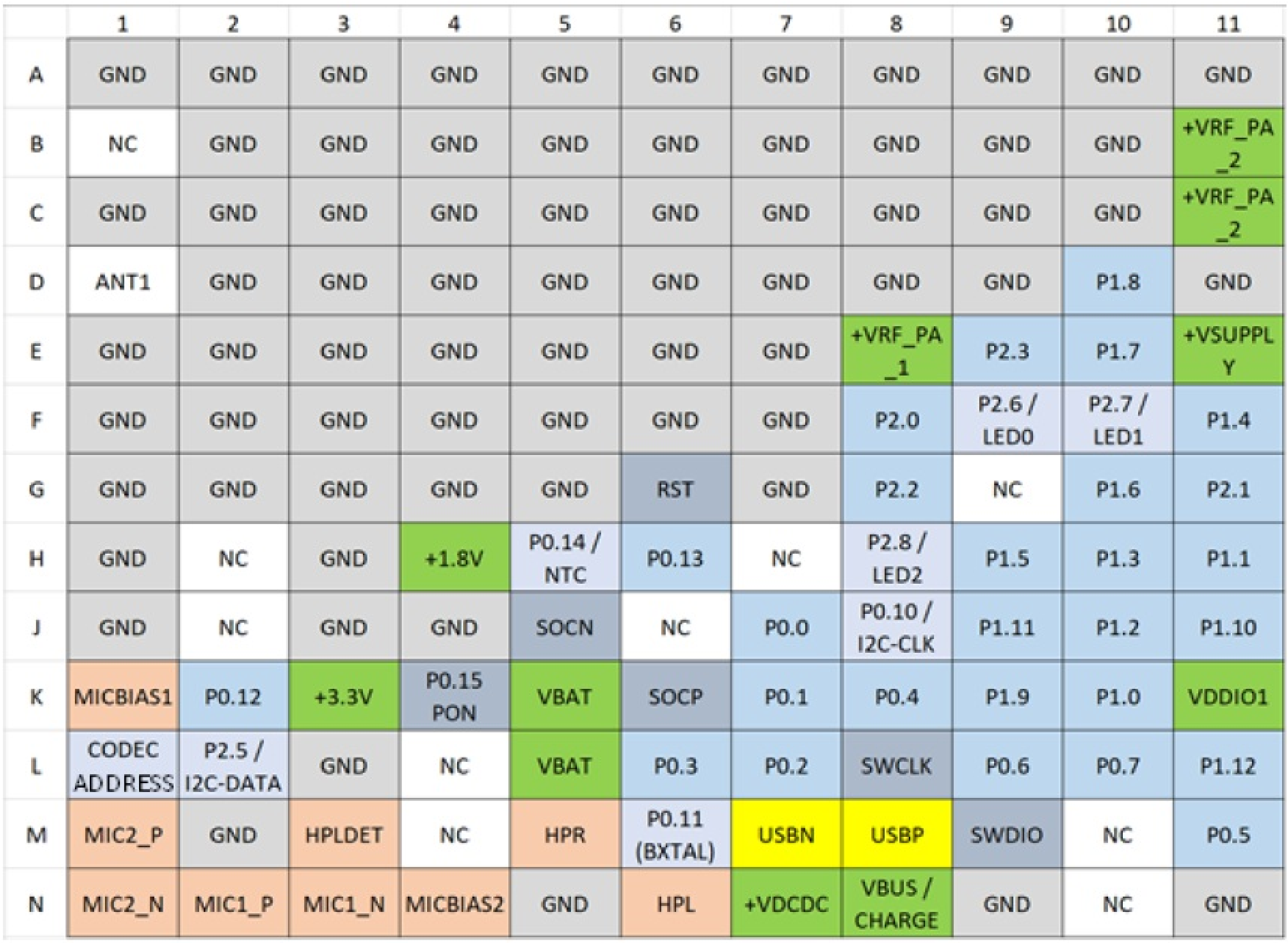


Figure 2: Block Diagram

Note that the block diagram shown in Figure 2 demonstrates the stereo audio capability. The hardware of the DA14AVDDECT supports these connections, but the current software implementations only supports mono audio.

Pinout

With Figure 3 the pin functions can easily be identified. Please refer to chapter 3 for an accurate mechanical representation.



	1	2	3	4	5	6	7	8	9	10	11
A	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
B	NC	GND	GND	GND	GND	GND	GND	GND	GND	GND	+VRF_PA_2
C	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	+VRF_PA_2
D	ANT1	GND	GND	GND	GND	GND	GND	GND	GND	P1.8	GND
E	GND	GND	GND	GND	GND	GND	GND	+VRF_PA_1	P2.3	P1.7	+VSUPPLY
F	GND	GND	GND	GND	GND	GND	GND	P2.0	P2.6 / LED0	P2.7 / LED1	P1.4
G	GND	GND	GND	GND	GND	RST	GND	P2.2	NC	P1.6	P2.1
H	GND	NC	GND	+1.8V	P0.14 / NTC	P0.13	NC	P2.8 / LED2	P1.5	P1.3	P1.1
J	GND	NC	GND	GND	SOCN	NC	P0.0	P0.10 / I2C-CLK	P1.11	P1.2	P1.10
K	MICBIAS1	P0.12	+3.3V	P0.15 PON	VBAT	SOCP	P0.1	P0.4	P1.9	P1.0	VDDIO1
L	CODEC ADDRESS	P2.5 / I2C-DATA	GND	NC	VBAT	P0.3	P0.2	SWCLK	P0.6	P0.7	P1.12
M	MIC2_P	GND	HPLDET	NC	HPR	P0.11 (BXTAL)	USBN	USBP	SWDIO	NC	P0.5
N	MIC2_N	MIC1_P	MIC1_N	MICBIAS2	GND	HPL	+VDCDC	VBUS / CHARGE	GND	NC	GND

Figure 3: DA14AVDDECT BGA Pinout Diagram (Top View)

NOTE

On the bottom (ball) side of the module, at the end of the printed antenna pattern, there is a ball ‘T1’ (see the lower left corner of Figure 4). This is for Dialog’s production test purposes only and serves no customer application use. The customer application shall not have a solder connection to T1.

Table 1: Pin Description

Pin No.	Pin Name	Type (Table 2)	Drive (mA)	Reset State	Description
RF					

D1	ANT1	AIO			RF connection ANT1 This pin is used together with the integrated printed antenna to connect an external antenna to support antenna diversity.
T1	ANT_TEST	AIO			The PCB of a customer application shall not have a solder connection to T1.
Power					
E8	+VRF_PA_1	PWR			Input supply voltage of RFPA bias stage
B11, C11	+VRF_PA_2	PWR			Input supply voltage of RFPA power stage
H4	+1.8V	PWR			Output supply voltage 1.8 V It can be used to configure the GPIO voltage of bank 1 (VDDIO1), for example.
K3	+3.3V	PWR			Output supply voltage 3.3 V It can be used to configure the GPIO voltage of bank 1 (VDDIO1), for example.
K5, L5	VBAT	PWR			Main input supply voltage
K11	VDDIO	PWR			Input supply voltage of GPIO bank 1

N7	+VDCDC	PWR			Output supply voltage of internal DCDC converter It can be used as an input when the internal DCDC is disabled.
N8	VBUS/CHARGE	PWR			Input supply voltage of the battery charger and/or the USB
E11	VSUPPLY	PWR			Output voltage of DA14495
Audio					
K1	MICBIAS1	AO			Microphone bias output 1 (requires 1 µF decoupling)
N2	MIC1_P	AI DO			Differential analog microphone 1 input (Pos) Digital microphone 1 clock output
N3	MIC1_N	AI DI			Differential analog microphone 1 input (Neg) Digital microphone 1 data input
N4	MICBIAS2	AO			Microphone bias output 2 (requires 1 µF decoupling)

M1	MIC2_P	AI DO			Differential analog microphone 2 input (Pos) Digital microphone 2 clock output
N1	MIC2_N	AI DI			Differential analog microphone 2 input (Neg) Digital microphone 2 data input

Pin No.	Pin Name	Type (Table 2)	Drive (mA)	Reset State	Description
M3	HPLDET	AI			Current source for headphone detection
M5	HPR	AO			Single-ended headphone output (Right)
N6	HPL	AO			Single-ended headphone output (Left)
L1	CODEC ADDRESS	DI			Connecting this pin to GND selects the I2C slave address 0x1A; Connecting this pin to pin H4 selects the I2C slave address 0x1B.
USB					
M7	USBN	A11		Hi-Z	INPUT/OUTPUT. USB-. Typical HSoutput impedance is 45 Ω.

M8	USBP	A11		Hi-Z	INPUT/OUTPUT. USB+. Typical HSoutput impedance is 45 Ω.
JTAG					
L8	SWCLK	DI-BP		I_PD	INPUT. ARM debug interface clock.
M9	SWDIO	DIO-BP	4/8	I_PU	INPUT/OUTPUT. ARM debug interface data input/output.
Special Functions					
G6	RSTn	A5		25 kΩpull-up resistor connect ed to VDD1V 2	INPUT/OPEN DRAIN OUTPUT withinternal pull-up.Reset signal (active LOW). No external capacitor required.If the internal VDD1V2 drops below 1.06 V, this pin is pulled low. An external device may not drive this pin higher than VDD1V2 (1.2V).
J5	SOCN	A1		I	INPUT. Battery fuel gauge reference ground. Connect as star point.If it is not used, connect it to GND to prevent a false power-on trigger (NEW_BAT) due to a floating pin.
K6	SOCP	A1			INPUT. Battery fuel gauge positive input.If it is not used, connect it to VSS to prevent a false power-on trigger (NEW_BAT) due to a floating pin.

K4	P0.15/PON	DI	4/8	I_PD	INPUT with a selectable pull up/down resistor.Note that P0.15 cannot be used as output.INPUT. Device Power-on.It can be directly connected to VBAT (max 5 V).If PON has a fixed connection to VBAT, the PD resistor can be disabled to save power.
F9	P2.6/LED0	DIO-BP DO-BP	4/8/16	I_PU	INPUT/OUTPUT with a selectable pull up/down resistor.OUTPUT: Back drive protected pad for LED0 up to VSUPPLY. A series of resistors is required for LED operation.

Pin No.	Pin Name	Type (Table 2)	Drive (mA)	Reset State	Description
F10	P2.7/LED1	DIO-BP DO-BP	4/8/16	I_PU	INPUT/OUTPUT with a selectable pull up/down resistor.OUTPUT: Back drive protected pad for LED1 up to VSUPPLY. A series of resistors is required for LED operation.
H8	P2.8/LED2	DIO-BP DO-BP	4/8/16	I_PU	INPUT/OUTPUT with a selectable pull up/down resistor.OUTPUT: Back drive protected pad for LED2 up to VSUPPLY. A series of resistors is required for LED operation.

H5	P0.14/NTC	DIO-BP AIAI	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.ANALOG INPUT: Analog to Digital Converter (ADC) input 0.ANALOG INPUT: Li-Ion/Li_Po NTCprotection which is used to automatically switch off the charger circuit if this input goes beyond the specified voltage ranges.Note: Only GPIO port (I/O), digital input, and the analog function are available; no peripheral outputs are available.
L2	P2.5/I2C_DATA	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
J8	P0.10/I2C_CLK	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
M6	P0.11/BXTAL	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.OUTPUT: PLL Codec output (12.288 MHz/24.567 MHz).Supplied from VDDIO_BXTAL.
General Purpose IO					
J7	P0.0	DIO	4/8	I_PU	INPUT/OUTPUT with a selectable pull up/down resistor.If ‘0’ is on the rising edge of the RSTn pin, boot the module from UART. Assign the module as UTX if the module is booted from UART

K7	P0.1	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor. Assign the module as URX if the module is booted from UART.
L7	P0.2	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.If ‘1’ is on the rising edge of the RSTn pin, the Booter will wait in an endless loop for debugging purposes.
L6	P0.3	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
K8	P0.4	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
M11	P0.5	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.

Pin No.	**Pin Name**	**Type (Table 2)**	**Drive (mA)**	**Reset State**	**Description**
L9	P0.6	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
L10	P0.7	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
K2	P0.12	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
H6	P0.13	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.

K10	P1.0	DIO	4/8/12/16	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
H11	P1.1	DIO	4/8/12/16	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
J10	P1.2	DIO	4/8/12/16	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
H10	P1.3	DIO	4/8/12/16	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
F11	P1.4	DIO	4/8/12/16	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
H9	P1.5	DIO	4/8/12/16	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
G10	P1.6	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
E10	P1.7	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.

D10	P1.8	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
K9	P1.9	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
J11	P1.10	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
J9	P1.11	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
L11	P1.12	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
F8	P2.0	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
G11	P2.1	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
G8	P2.2	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
E9	P2.3	DIO	4/8	I_PD	INPUT/OUTPUT with a selectable pull up/down resistor.
Ground and No Connects					

Pin No.	**Pin Name**	**Type (Table 2)**	**Drive (mA)**	**Reset State**	**Description**
A1, A2, A3, A4, A5, A					

6, A7, A8, A9, A10, A11, B2, B3, B4, B5, B6, B7, B8, B9, B10, C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, D2, D3, D4, D5, D6, D7, D8, D9, D11, E1, E2, E3, E4, E5, E6, E7, F1, F2, F3, F4, F5, F6, F7, G1, G2,	GND	GND			Analog and digital ground. They are connected together on a solid ground plane.

G3, G4, G5, G7, H1, H3, J1, J3, J4, L3, M2, N5, N9, N11					
G9, H7, J6, M4, M10, N10	NC	NC			Not connected. No package ball/pin available on the package.
H2, J2, L4	Keep out	NC			Not connected, but package balls/pins are available: implement keep-out on application PCBs to ensure balls/pins are not connected to anything or close to any noise signals.

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
DIOD	Digital input/output open drain	BP	Back drive protection

PU	Pull-up resistor (fixed)	SPU	Switchable pull-up resistor
PD	Pull-down resistor (fixed)	SPD	Switchable pull-down resistor
PWR	Power	GND	Ground

Characteristics

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied.

Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	**Description**	**Conditions**	**Min**	**Max**	**Unit**
VESD	Maximum ESD voltage	HBM		2	kV
VBAT	Battery voltage			4.6	V
VBUS	BUS voltage			6.5	V

Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**

VBAT	Battery supply voltage	Limited by the supply voltage requirements of the SKY77762 power amplifier module from SYKWORKS	1.9		4.2	V
VBUS	USB voltage		4.2		5.75	V
+VRF_PA_1	Bias supply SKY77762	< 10 mA current draw	3.0		4.2	V
+VRF_PA_2	Power supply SKY77762	Up to ~350 mA current draw	1.9	3.3	3.6	V
TA	Ambient operating temperature range		-20		+60	°C
VSUPPLY	Output voltage of DA14495		1.9	3.45	3.6	V
VDCDC	Output voltage of the DA14495 DCDC converter. When the DCDC is disabled, the same pin can be connected to an external supply, overriding the internal DCDC converter		.4		1.89	V

Electrical Characteristics

Table 5: Digital I/O Characteristics

Parameter	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
VDDIO	Supply voltage of IO band		1.6		3.45	V
VPIN_NEG	Negative voltage on IO pin		GND – 0.3			V
VPIN_POS	Positive voltage on IO pin				VDDIO + 0.2	V
VPIN_PON	Voltage on pin P0.15/PON				5	V
VPIN_USB	Voltage on pins USBp and USBn				3.6	V
VIH	High level input voltage		0.7 × VDDIO			V
VIL	Low level input voltage				0.3 × VDDIO	V
VDDIO0_2	IO voltage bank0/2			1.8		V
VDDIO1	IO voltage bank 1	User programmable by connecting the 3V3 (pin K3) or 1V8 (pin H4) from the module to VDDIO1		1.8 3.3		V

Table 6: Radio Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Foperating	Frequency bands supported	EU-DECT, US-DECT, and J-DECT (K-DECT is not supported)				
RXsense	Receiver sensitivity	GFSK, EU-DECT ch5		-93		dBm
Po	Transmitted output power	GFSK, EU-DECT ch5		+22		dBm
Pspur	Spurious emissions	ETSI/FCC compliant				
TXACPR1	Transmitter adjacent channel power ratio M = 1	Po = +16dBm, π/4 DQPSK			-33	dBc
TXACPR3	Transmitter adjacent channel power ratio M = 3	Po = +16dBm, π/4 DQPSK			-66	dBc
TXEVM	Transmitter error vector magnitude	Po = +16dBm, π/4 DQPSK			6	%

Table 7: Supply Currents (Tour Guide mode)

Parameter	Description	Conditions (Note 1)	Min	Typ	Max	Unit
Iavg_TG_stby	Standby supply current (Tour Guide mode)	FP (TX); HPM		23		mA
		FP (TX); HPM/U		20		mA
		PP (RX); HPM		8		mA

Iavg_TG_talk	Talk mode supply current	FP (TX); LPM		53		mA

Parameter	Description	Conditions (Note 1)	Min	Typ	Max	Unit
	(Tour Guide mode)	FP (TX); HPM		71		mA
		FP (TX); HPM; Question call		91		mA
		FP (TX); HPM/U		61		mA
		FP (TX); HPM/U; Question call		76		mA
		PP (RX); LPM; RX only		31		mA
		PP (RX); LPM; Return channel		38		mA
		PP (RX); HPM; RX only		42		mA
		PP (RX); HPM; Return channel		49		mA
		PP (RX); HPM/U; RX only		37		mA
		PP (RX); HPM/U; Return channel		46		mA

Note 1 VBAT, +VRF_PA_1 and +VRF_PA_2 pins connected to +3.3V supply; Iavg: current drawn from the +3.3V supply.

SW configuration by default example appplication. Standby mode: no PP locked to FP.

Table 8: Supply Currents (Public Address mode)

Parameter	**Description**	**Conditions (Note 1)**	**Min**	**Typ**	**Max**	**Unit**
Iavg_PA_stby	Standby supply current (Public Address mode)	FP (RX); HPM		26		mA
		FP (RX); HPM/U		20		mA
		PP (TX); HPM		8		mA
Iavg_PA_talk	Talk mode supply current (Public Address mode)	FP (RX); LPM; 1PP (TX)		35		mA
		FP (RX); LPM; 2PPs (TX)		42		mA
		FP (RX); LPM; 3PPs (TX)		50		mA
		FP (RX); LPM; 4PPs (TX)		56		mA
		FP (RX); HPM; 1PP (TX)		38		mA
		FP (RX); HPM; 2PPs (TX)		48		mA
		FP (RX); HPM; 3PPs (TX)		56		mA
		FP (RX); HPM; 4PPs (TX)		63		mA
		FP (RX); HPM/U; 1PP (TX)		34		mA
		FP (RX); HPM/U; 2PPs (TX)		43		mA

		FP (RX); HPM/U; 3PPs (TX)		51		mA
		FP (RX); HPM/U; 4PPs (TX)		60		mA
		PP (TX); LPM		32		mA
		PP (TX); HPM		44		mA
		PP (TX); HPM/U		38		mA

Table 9: Supply Currents (Voice Conference mode)

Parameter	**Description**	**Conditions (Note 1)**	**Min**	**Typ**	**Max**	**Unit**
Iavg_CVM_stby	Standby supply current (Voice Conference mode)	FP; HPM		16		mA
		PP; HPM		8		mA

Parameter	**Description**	**Conditions (Note 1)**	**Min**	**Typ**	**Max**	**Unit**
		FP; HPM; 1PP		39		mA
		FP; HPM; 2PPs		47		mA
		FP; HPM; 3PPs		58		mA
		FP; HPM; 4PPs		68		mA
		FP; HPM; 5PPs		76		mA
		FP; HPM; 6PPs		86		mA

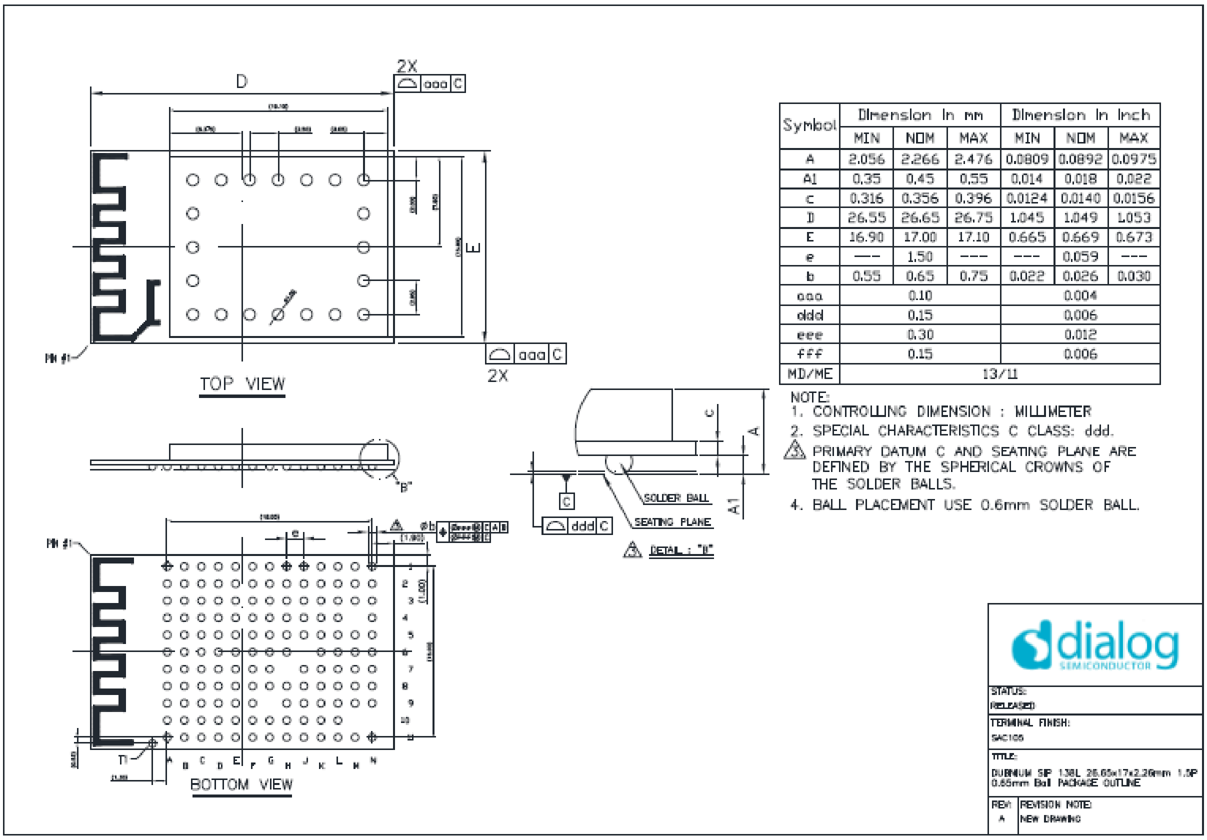
Iavg_CVM_talk	Talk mode supply current (Voice Conference mode)	FP; HPM; 7PPs		95		mA
		FP; HPM; 8PPs		104		mA
		FP; HPM/U; 1PP		37		mA
		FP; HPM/U; 2PPs		45		mA
		FP; HPM/U; 3PPs		54		mA
		FP; HPM/U; 4PPs		62		mA
		FP; HPM/U; 5PPs		69		mA
		FP; HPM/U; 6PPs		77		mA
		FP; HPM/U; 7PPs		85		mA
		FP; HPM/U; 8PPs		91		mA
		PP; HPM		31		mA

Functional Description

The DA14AVDDECT module is a hardware platform capable of serving multiple functions. The functions fall into two categories, Cordless Voice Module (CVM) and Wireless Audio Module (WAM), and they are defined in the software. These two functions of the DA14AVDDECT are described in their separate CVM and WAM software documents. Please consult with your Dialog representative for further details.
Please also note that the module is supplied without any software pre-loaded in FLASH. Please refer to [3] for programming and configuring the module.

Package Information

Package Outline Drawing



Symbol	Dimension In mm			Dimension In Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.056	2.266	2.476	0.0809	0.0892	0.0975
A1	0.35	0.45	0.55	0.014	0.018	0.022
c	0.316	0.356	0.396	0.0124	0.0140	0.0156
D	26.55	26.65	26.75	1.045	1.049	1.053
E	16.90	17.00	17.10	0.665	0.669	0.673
e	---	1.50	---	---	0.059	---
b	0.55	0.65	0.75	0.022	0.026	0.030
aaa	0.10			0.004		
ddd	0.15			0.006		
eee	0.30			0.012		
fff	0.15			0.006		
MD/ME	13/11					

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. SPECIAL CHARACTERISTICS C CLASS: ddd.
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. BALL PLACEMENT USE 0.6mm SOLDER BALL.

STATUS:
RELEASED
TERMINAL FINISH:
SAC105
TITLE:
DUBNIUM SIP 138L 26.65x17x2.26mm 1.5P 0.65mm Ball PACKAGE OUTLINE
REV: A
REVISION NOTE: NEW DRAWING

Figure 4: DA14AVDDECT BGA Package Outline Drawing

Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 10.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org

The DA14AVDDECT is qualified for MSL 3.

Table 10: MSL Classification

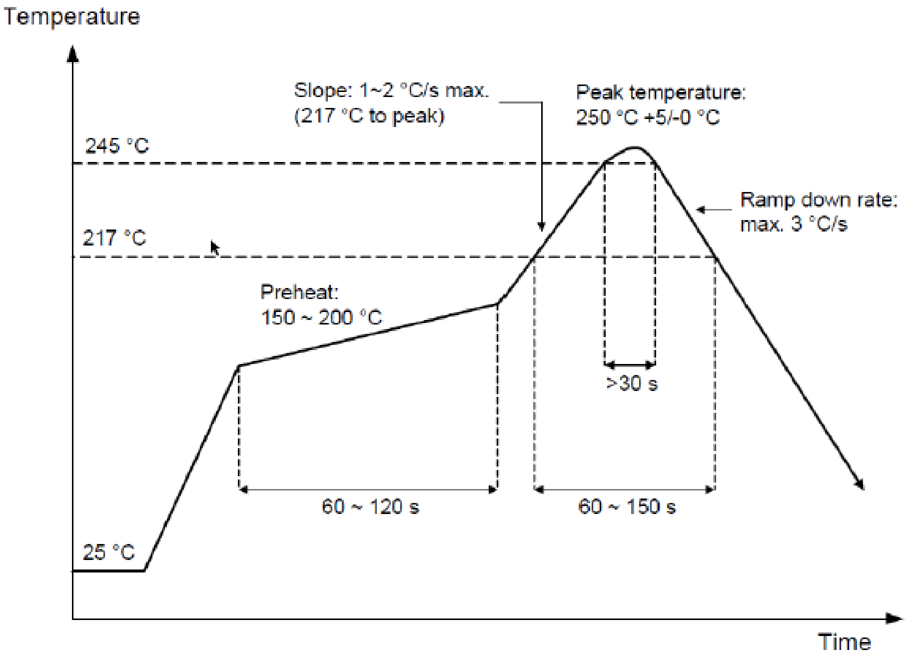
MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH

MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

Soldering Information

The DA14AVDDECT should be soldered using a lead-free reflow soldering profile as shown in Figure 5. Adjustments to the profile may be necessary, depending on process requirements.

The recommended solder paste for lead-free soldering is Sn 96.5%, Ag 3.0%, and Cu 0.5%.



Packaging

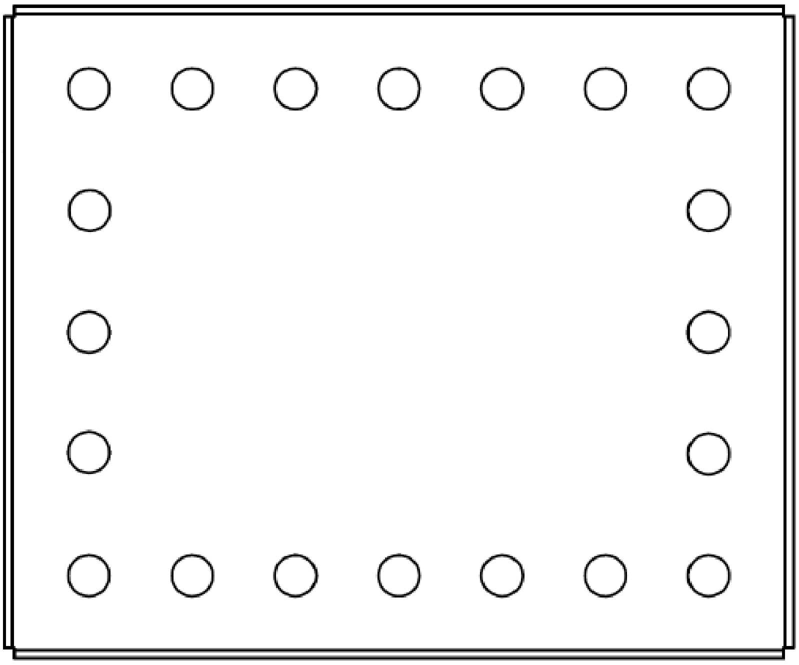


Figure 6: DA14AVDDECT Package Marking

Figure 6: DA14AVDDECT Package Marking

Table 11: DA14AVDDECT Package Marking Table

Row/Column	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
1.					Manufacturer Part Number															
2.	Dialog Logo				Date Code					TELEC License Number										
3.					Assembly Lot Number											TELEC mark				
4.	CE mark																			
5.					Qualification Code															
6.	RF License (FCC)																			
7.	RF License (Industry Canada)																			
8.	Pin1 Orientation																			

Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's customer support portal or your Dialog Semiconductor local sales representative.
Table 12: Ordering Information

Part Number	Package	Size Module(mm)	Shipment Form
DA14AVDDECT SF01	PCB Module	17.0 mm × 26.65 mm	Tray

Application Information

As mentioned in chapter 2, the DA14AVDDECT functionality is defined in software and the software specifics are detailed in separate documents. The DA14AVDDECT can be operated stand-alone or controlled from a host application through the API interface. The on-board FLASH memory can be used to store the custom code.
The following points highlight some hardware-specific aspects of application implementation:

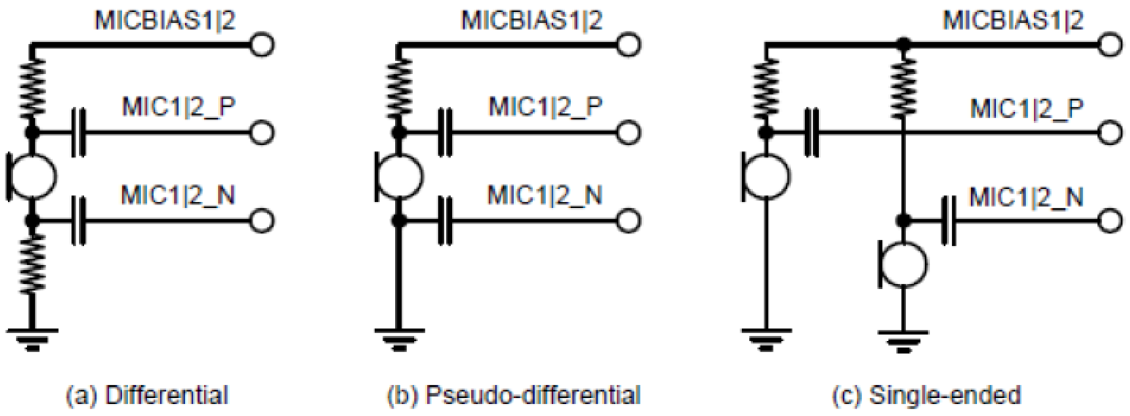
- Antennas:
    - The module includes an integrated printed antenna (ANT1)
    - Optionally, an additional external antenna (ANT2) can be connected to support antenna diversity
    - For an optimal wireless performance, it is recommended to always use two antennas, that is, the internal antenna combined with an external antenna
    - A special build option may be ordered with a special ordering code that disconnects ANT1 from the internal printed antenna and allows two external antennas to be used
- Supply voltage of RFPA:
    - +VRF_PA_1 and +VRF_PA_2 need to be connected to external supply voltages
    - In order to be able to leverage the Limited Modular Approval certification (for more information please refer to [4]), the supply circuit should be copied from the reference application used for certification. If it is desired to deviate from the reference application, please note the following, and it may not be possible to

leverage the Limited Modular Approval any more:

  - +VRF_PA_1 requires a minimum input voltage of 3.0 V (current draw 10 mA), so an external DCDC boost converter will be required if two AA applications are targeted
  - Typically, +VRF_PA_2 is connected to an external 3.3 V supply voltage (up to 350 mA current draw depending on the RF TX output power levels). An optimal battery efficiency is obtained if +VRF_PA_2 is sourced from a DCDC power supply adjusted within 0.5 V to 3.5 V based on the target output power levels
- The DA14AVDDECT module includes an integrated battery charger and the associated power dissipation increases the module's temperature. Please make sure that the chip temperature does not exceed its operational temperature range, especially when other functions are also enabled. Since the module includes an on-board temperature sensor to facilitate chip temperature detection, how to protect the chip from overheating needs to be implemented in software and is not described in further detail in this document
- The DA14AVDDECT module includes an integrated audio CODEC. To support an external audio CODEC, please map the GPIOs accordingly. It is implemented in software and is not described in further detail in this document
- An external protection IC may be required to protect VBUS from supply circuits with possible high overshoot

Audio Connections

Analog microphones can be connected as shown in Figure 7.



(a) Differential

(b) Pseudo-differential

(c) Single-ended

Figure 7: Connection of Analog Microphones

The bias resistor value shall be selected depending on the microphone requirements and MICBIAS1/2 must be decoupled with 1 µF capacitors.

Alternatively, up to four digital microphones can be supported by reusing the MIC1_P and MIC2_P pins as clock outputs and the MIC1_N and MIC2_N pins as digital data inputs. The IO voltage level of DMIC1 is set by the voltage present on MICBIAS1 and the IO voltage level of DMIC2 is set by the voltage present on MICBIAS2. The voltage present on MICBIAS1/MICBIAS2 can be either an output of the MICBIAS LDO or the IO voltage of the DMIC that is connected as an input on the appropriate MICBIAS pin for a minimum power consumption. The configuration of MICBIAS is through software and thus is not detailed further in this document.

The DA14AVDDECT module can support headphone detection. Document UM-D-012 [7] explains how to control this feature in the software. Please contact your Dialog representative for further details.

Layout Guidelines

The module pinout of DA14AVDDECT has been specifically designed to accommodate easy integration with the PCBs of customer applications without having to adding expensive PCB components to increase the cost due to, for example, blind vias or small line/space dimensions.

All standard practice layout rules and guidelines apply. Additional special care may be paid to the antenna and USB areas:

- The application PCB may not extend underneath the antenna area (see Figure 8)
- Signals from the application PCB containing high harmonic content (for example, clock signals or memory buses) must be kept away from the antenna
- No metal objects should be placed in the vicinity of the antenna (see Figure 8)
- The USB data lines should be routed with 90 Ω differential impedance lines and the line lengths must match
- Appropriate trace width and number of vias should be used for all power supply paths
- A common ground plane should be used to allow proper electrical and thermal performances
- Noise-sensitive analog signals, such as feedback lines or clock connections, should be kept away from the traces carrying pulsed analog or digital signals. This can be achieved by separation (distance) or by shielding the sensitive signals with quiet signals or ground traces

- Decoupling capacitors should be X5R ceramics and should be placed as near to the module as possible

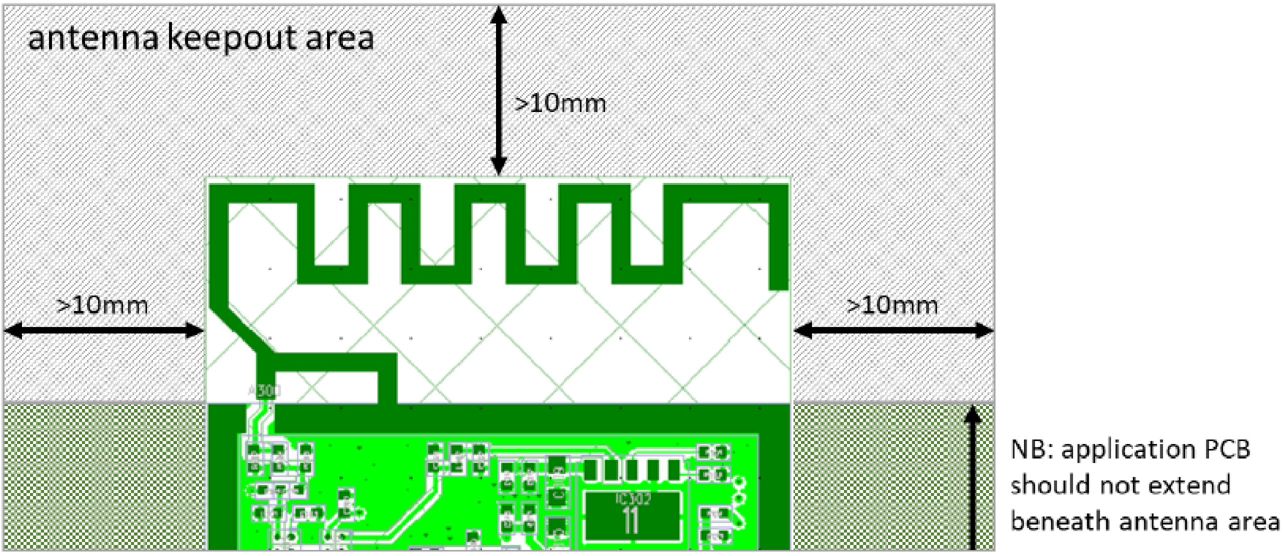


Figure 8: Keep-out Areas

It is also advised to use the HW layout of the DA14AVDDECT evaluation kit as a guideline for customer products. This HW was used during the certification process and should be regarded as a reference.

Please see reference document [4] for more information on the Limited Modular Approval certification and how it can be used, so that no new radio certification needs to be obtained for the end customer products.

Revision History

Revision	Date	Description
2.1	02-Jun-2020	Added supply current tables
2.0	14-May-2020	Preliminary datasheet
1.9	18-Sep-2019	Added ‘P2.5’ to I2C-DATA pin name

1.8	9-Sep-2019	Added reflow profile Changed pin name I2C-DATA Revised H2/J2 in figure 3 to correspond with table 1 Updated figure 9 to the latest EVK schematic snapshot
1.7	13-Aug-2019	Added text at LMA section Corrected pin L4 in the pin diagram (1.6 was erroneously reverted to GND), also corrected some pin naming typos Added wording about SW supporting only mono where as the HW supports stereo
1.6	8-Aug-2019	Updated pin diagram and table (E11 = Vsupply and others) Corrected B1 and D1 pin descriptions
1.5	6-Jun-2019	Changed pin L4 to NC, added comment about pin T1
1.4	19-Mar-2019	Updated POD
1.3	7-Mar-2019	Added keepout area drawing in ch9, changed pins H2, J2 to NC
1.2	20-Feb-2019	Updated package outline drawing; minor cosmetic edits
1.1	26-Nov-2018	Added package outline drawing
1.0	31-Oct-2018	First version of target datasheet

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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Contacting Dialog Semiconductor

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Germany

Dialog Semiconductor Gmb

FCC Statement

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. his device must accept any interference received, including interference that may cause undesired operation.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.
The device has been evaluated to meet general RF exposure requirement. The device can be used in portable exposure condition without restriction.
If the FCC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following:

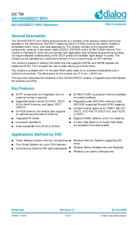
“Contains Transmitter Module FCC ID: NTMGXTM Or Contains FCC ID: NTMGXTM”
When the module is installed inside another device, the user manual of the host must contain below warning statements;

The devices must be installed and used in strict accordance with the manufacturer's instructions as described in the user documentation that comes with the product.
Any company of the host device which install this modular with Single modular approval should perform the test of radiated emissionand spurious emission according to FCC part 15C : 15.247 and 15.209 requirement,Only if the test result comply with FCC part 15C : 15.247 and 15.209 requirement, then the host can be sold legally.

FCC RF Exposure Information and Statement
The SAR limit of USA (FCC) is 1.6 W/kg averaged over one gram of tissue. Device types: Transmitter Module (FCC ID:NTMGXTM) has also been tested against this SAR limit. The highest SAR value reported under this standard during product certification for use properly worn on the body is 0.382W/kg. This device was tested for typical body-worn operations with the back of the handset kept 0mm from the body. To maintain compliance with FCC RF exposure requirements, use accessories that maintain a 0mm separation distance between the user's body and the back of the handset. The use of belt clips, holsters and similar accessories should not contain metallic components in its assembly. The use of accessories that do not satisfy these requirements may not comply with FCC RF exposure requirements, and should be avoided.

Body-worn Operation
This device was tested for typical body-worn operations. To comply with RF exposure requirements, a minimum separation distance of 0mm must be maintained between the user's body and the handset, including the antenna. Third-party belt-clips, holsters, and similar accessories used by this device should not contain any metallic components. Body-worn accessories that do not meet these requirements may not comply with RF exposure requirements and should be avoided. Use only the supplied or an approved antenna.

Documents / Resources

	dialog SEMICONDUCTOR DA14AVDDECT SF01 Wireless Module [pdf] Owner's Manual DA14AVDDECT SF01, DA14AVDDECT SF01 Wireless Module, Wireless Module, Module

References

- User Manual

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DA14AVDDECT SF01, DA14AVDDECT SF01 Wireless Module, dialog SEMICONDUCTOR, Module, Wireless Module

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