AzureWave AW-XH323 PUR Wi-Fi Plus Bluetooth 5.2 Combo SIP Module Owner's Manual

AzureWave Technologies, Inc.

AW-XH323
AW-XH325
AW-XH327
IEEE 802.11 a/b/g/n/ac/ax Wi-Fi
+ Bluetooth 5.3 Combo SIP Module
Datasheet
Rev.C DF
(For Standard)
FORM NO.: FR2-015_A
Responsible Department: WBU

Contents

Features

WiFi

- 802.11a/b/g/n/ac/ax dual-band capable (2.4/5/6 GHz)

- 5/6 GHz: 20/40/80-MHz channels, 1024-QAM, 2×2 MIMO providing up to 1.2 Gbps PHY data rate
- 2.4 GHz: 20/40-MHz channels, 1024-QAM, 2×2 MIMO providing up to 574 Mbps PHY date rate
- 802.11ax STA mode and Soft AP mode with 11ax scheduled access
- Supports 802.11d, h, k, r, v, w, ai
- Zero-wait dynamic frequency selection (DFS): Background channel availability check (CAC) scan for immediate switch to candidate DFS channel compliant,
- On-chip power amplifiers and low-noise amplifiers
- Supports 2 and 3-antenna configurations
- Supports multipoint external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE
- Fast VSDB (Virtual Simultaneous Dual Band)
- Worldwide regulatory support: Global products supported with worldwide homologated design
- Integrated Arm® Cortex® R4 processor with tightly coupled memory for complete WLAN subsystem functionality. This architecture offloads the host processor completely from WLAN functionality.
- Transmission and reception of HE-SU and HE- ER-SU PPDU.
- Reception of HE-MU PPDU -OFDMA/MU- MIMO Frame.
- Transmission of HE-TB PPDU (Uplink MU OFDMA).

Bluetooth

- Qualified for Bluetooth® Core specification 5.3 (Basic Rate+ Enhanced Data Rate+ Bluetooth® Low Energy)
- All Bluetooth 5.0/5.1/5.2 optional features supported including LE-Audio.
- Dedicated Bluetooth RF path for best WLAN-BT coexistence performance.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a high-speed UART interface and PCM/12S for audio data.
- Supports multiple simultaneous Advanced Audio Distribution.
- Profiles (A2DP) for stereo sound.
- On-chip memory includes 512 KB SRAM and 2 MB ROM.

Revision History

Document NO: R2-1323-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2022/11/23	DCN028186	Initial Version	Barry Tsai	N.C. Chen
B	2023/02/03	DCN028626	Power table update	Barry Tsai	N.C. Chen
C	2023/05/31	DCN029248	Pin table update Storage Temperature update	Barry Tsai	N.C. Chen

Introduction

1.1 Product Overview

The AW-XH323 device provides the highest level of integration for Commercial and Consumer IoT wireless systems with integrated dual-band 2×2 MIMO IEEE 802.11ax WLAN MAC/baseband/radio, Bluetooth 5.3 MAC/baseband/radio, and integrated Power Management Unit. WLAN and Bluetooth radios also include on-chip power amplifiers and low-noise amplifiers to further reduce the need for external components.

WLAN interfaces to host processor through a PCIe v3.0 Gen2 and SDIO 3.0 interface while Bluetooth host interface is provided through high-speed 4-wire UART interface. Additionally, the Bluetooth section supports PCM interfaces for audio applications.

AW-XH323 is qualified to operate across Industrial (-40 °C to +85 °C) temperature range.

1.2 Block Diagram

TBD

1.3 Specifications Table

1.3.1 General

Features	**Description**
Product Description	IEEE 802.11 a/b/g/n/ac/ax Wi-Fi + Bluetooth 5.3 Combo SIP Module
Major Chipset	Infineon CYW5557X (486-ball WLCSP)
Host Interface	WiFi + BT PCIe + UART/SDIO+UART **Note:** Please refer to G10 pin of 2.3 Host configuration interface table for your interface choice
Dimension	10mm x 10mm x 1.26mm
Form factor	Sip module,117 pins
Antenna	2T2R, external ANT1(Main) WiFi/Bluetooth → TX/RX ANT2(Aux) WiFi → TX/RX
Weight	TBD

1.3.2 WLAN

Features	**Description**

WLAN Standard	IEEE 802.11 a/b/g/n/ac/ax
WLAN VID/PID	N/A
WLAN SVID/SPID	N/A
Frequency Rage	WLAN: 2.4 / 5 / 6 GHz Band
Modulation	DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9), 1024-QAM(MCS10~11)
Number of Channels	2.4GHz USA, Canada and Taiwan – 1 ~ 11 China, Most European Countries – 1 ~ 13 Japan, 1 ~ 13 5GHz USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165 6GHz CH1~CH233 5GHz USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165 6GHz CH1~CH233

Output Power[1]
(Board Level Limit)*

2.4G

	Min	Typ	Max	Unit
11b(11Mbps) @EVM<8°/0	18	20.	21	dBm
11g (54Mbps) @EVW≦-25 dB	17.	18	20.	dBm
IIn (HT20 MCS7) ©EVW≦-27 dB	15.		18.	dBm
11 ax (HE20 MCS11) @EVM ≦-35 dB 13.5 15			17.	dBm

5G

	Min	Typ	Max	Unit
11 a (54Mbps) @EVM<-25 dB	15.	17.	19.	dBm
IIn (HT20 MCS7) @EVM ≦-27 dB	14.	16.	18.	dBm
IIn (HT40 MCS7) @EVM ≦-27 dB	14.	16.	18.	dBm
11 ac (VHT20 MCS8) @EVM ≦-30 dB	12	14	16	dBm
11 ac (VHT40 MCS9) @EVM ≦-32 dB	11.	13.	15.	dBm
11 ac (VHT80 MCS9) @EVM ≦-32 dB	10.	12.	14.	dBm
11 ax (HE20 MCS11) @EVM ≦-35 dB	11	13	15	dBm
1 lax (HE40 MCS11) @EVM ≦-35 dB	11	13	15	dBm
11 ax (HE80 MCS11) @EVM ≦-35 dB	10	12	14	dBm

[1]Unless otherwise stated, limit values apply for an ambient temperature of +25 °C.

6G

	Min	Typ	Max	Unit
11 ax (HE20 MCS11) @EVM ≦-35 dB	8	10	12	dBm
11ax (HE40 MCS11) @EVM dB ≦-35	8	10	12	dBm
11ax (HE80 MCS11) @EVM ≦-35 dB	8	10	12	dBm

Receiver Sensitivity**

2.4G

	Min	Typ	Max	Unit
11b (11Mbps)		-89	-86	dBm
11g (54Mbps)		-77	-74	dBm
11n (HT20 MCS7)		-75	-72	dBm
11 ax (HE20 MCS11)		-64	-61	dBm

5G(n/ac packets with LDPC)

	Min	Typ	Max	Unit
11a (54Mbps)		-74	-71	dBm
11n (HT20 MCS7)		-72	-69	dBm
11n (HT40 MCS7)		-69	-66	dBm
11 ac (VHT20 MCS8)		-67	-64	dBm
11 ac (VHT40 MCS9)		-63	-60	dBm
11 ac (VHT80 MCS9)		-60	-57	dBm
11 ax (HE20 MCS11)		-61	-58	dBm
11 ax (HE40 MCS11)		-56	-53	dBm
11 ax (HE80 MCS11)		-55	-52	dBm

6G

	Min	Typ	Max	Unit
11 ax (HE20 MCS11)		-54	-51	dBm
11 ax (H E40 MCS11)		-53	-50	dBm
11 ax (HE80 MCS11)		-52	-49	dBm

Data Rate	802.11b: 1, 2, 5.5, 11Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n: MCS0~7 HT20/HT40 802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11ac: MCS0~8 VHT20 802.11ac: MCS0~9 VHT40/VHT80 802.11ax: MCS10~11 HE20/HE40/HE80
Security	WPA, WAPI STA, WPA2 (Enterprise) and WPA3 (Enterprise) support for powerful encryption and authentication AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibi lity Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)

* If you have any certification questions about output power please contact FAE directly
** Project is in engineering stage, RF performance is still being verified.

1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth 5.3</td></tr>
<tr><td>Bluetooth VID/PID</td><td>N/A</td></tr>
<tr><td>Frequency Rage</td><td>2400~2483.5MHz</td></tr>
<tr><td>Modulation</td><td>GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)</td></tr>
<tr><td>Output Power*</td><td><table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td>4</td><td>7</td><td>10</td><td>dBm</td></tr>
<tr><td>Low Energy (2MHz)</td><td>4</td><td>7</td><td>10</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Receiver Sensitivity**</td><td><table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td></td><td>-90</td><td>-87</td><td>dBm</td></tr>
<tr><td>EDR</td><td></td><td>-86</td><td>-83</td><td>dBm</td></tr>
<tr><td>Low Energy (2MHz)</td><td></td><td>-92</td><td>-89</td><td>dBm</td></tr>
</table></td></tr>
</table>

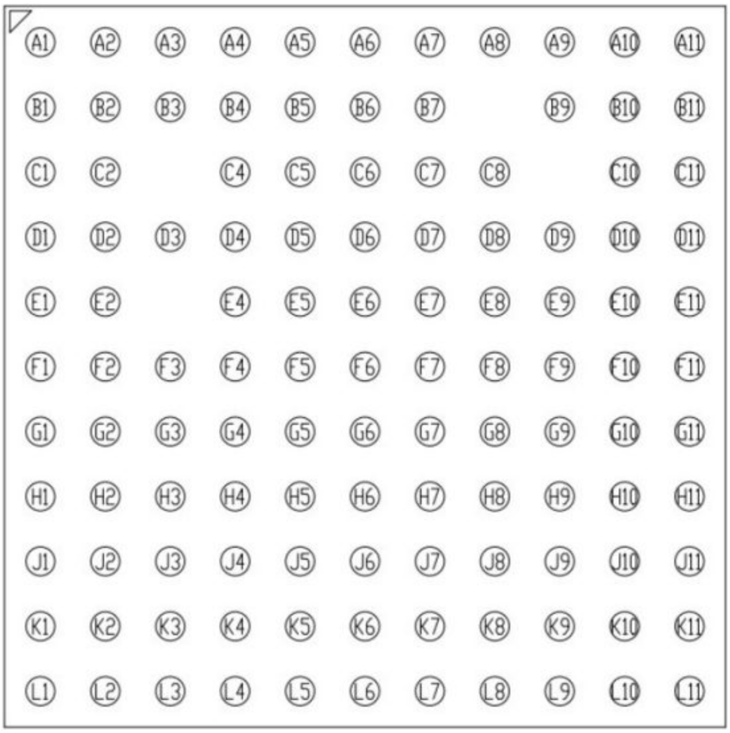
* If you have any certification questions about output power please contact FAE directly
** Project is in engineering stage, RF performance is still being verified.

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V
Operating Temperature	-40℃ to 85℃
Operating Humidity	less than 85% R.H.
Storage Temperature	-40℃ to 85℃
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	TBD
Changed Device Model	TBD

Pin Definition

2.1 Pin Map



AW-XH323 Pin Map (Top View)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
A1	GND	Ground.	–	GND
A2	PCIE_RDN	PCIE Receiver Differential Pair Negative Input		I
A3	PCIE_RDP	PCIE Receiver Differential Pair Positive Input		I
A4	PCIE_TDN	PCIE Transmitter Differential Pair Negative Output		O
A5	PCIE_TDP	PCIE Transmitter Differential Pair Positive Output		O
A6	PCIE_REFCLKN	PCI Express differential clock input-Negative		I
A7	PCIE_REFCLKP	PCI Express differential clock input-Positive		I
A8	GND	Ground.	–	GND
A9	CSR_VLX	CSR Power Stage Output to Inductor	0.9V	O
A10	ASR_VLX	ASR Power Stage Output to Inductor	1.12V	O
A11	GND	Ground.	–	GND
B1	GND	Ground.	–	GND
B2	GND	Ground.	–	GND
B3	GND	Ground.	–	GND
B4	GND	Ground.	–	GND
B5	GND	Ground.	–	GND
B6	GND	Ground.	–	GND
B7	GND	Ground.	–	GND
B9	CSR_VLX	CSR Power Stage Output to Inductor	0.9V	O
B10	ASR_VLX	ASR Power Stage Output to Inductor	1.12V	O
B11	GND	Ground.	–	GND
C1	WL_REG_ON	Low asserting reset for WiFi core	3.3V	I
C2	BT_PCM_SYNC	PCM sync signal	1.8V	I/O
C4	PCIE_CLKREQ_L	PCIe clock request	1.8V	OD

C5	GND	Ground.	–	GND
C6	LHL_GPIO5	Miscellaneous General Purpose I/O	1.8V	I/O
C7	BT_REG_ON	Low asserting reset for Bluetooth core	3.3V	I
C8	GND	Ground.	–	GND
C10	VBAT	Main power voltage source input	3.3V	PWR
C11	VBAT	Main power voltage source input	3.3V	PWR
D1	PCIE_PERST_L	PCIe host indication to reset the device	1.8V	I
D2	BT_PCM_IN	PCM data input.	1.8V	I
D3	BT_PCM_OUT	PCM data output.	1.8V	O
D4	BT_PCM_CLK	PCM clock; can be master (output) or slave (input).	1.8V	I/O
D5	PCIE_PME_L	PCI power management event output	1.8V	OD
D6	LHL_GPIO3	Miscellaneous General Purpose I/O	1.8V	I/O
D7	LHL_GPIO2	Miscellaneous General Purpose I/O	1.8V	I/O
D8	GND	Ground.	–	GND
D9	CBUCK_0P9	Internal Buck 0.9V voltage generation pin.	0.9V	I
D10	CBUCK_0P9	Internal Buck 0.9V voltage generation pin.	0.9V	I
D11	ABUCK_1P12	Internal Buck 1.12V voltage generation pin.	1.12V	I
E1	GND	Ground.	–	GND
E2	GPIO_0_WL_HOST_WAKE	WL Host Wake.	1.8V	O
E4	BT_DEV_WAKE	Bluetooth DEVICE WAKE	1.8V	I/O
E5	GND	Ground.	–	GND
E6	LHL_GPIO4	Miscellaneous General Purpose I/O	1.8V	I/O
E7	GPIO_11_WL_UART_TX	Debug UART Serial Output.	1.8V	O
E8	GND	Ground.	–	GND
E9	GPIO_10_WL_UART_RX	Debug UART Serial Input.	1.8V	I

E10	GND	Ground.	–	GND
E11	ABUCK_1P12	Internal Buck 1.12V voltage generation pin.	1.12V	I
F1	BT_UART_RTS_N	Bluetooth UART request to send	1.8V	O
F2	BT_UART_CTS_N	Bluetooth UART clear to send	1.8V	I
F3	BT_HOST_WAKE	Bluetooth HOST_WAKE.	1.8V	I/O
F4	BT_CLK_REQ	A Bluetooth clock request.	1.8V	I/O
F5	GND	Ground.	–	GND
F6	LHL_GPIO0	Miscellaneous General Purpose I/O	1.8V	I/O
F7	LPO_IN	External Sleep Clock Input (32.768 kHz)	1.8V	I
F8	GND	Ground.	–	GND
F9	GND	Ground.	–	GND
F10	GND	Ground.	–	GND
F11	VDDIO	1.8 V IO Supply for WLAN GPIOs	1.8V	PWR
G1	BT_UART_TXD	Bluetooth UART serial data output	1.8V	O
G2	BT_UART_RXD	Bluetooth UART serial data input	1.8V	I
G3	GND	Ground.	–	GND
G4	GND	Ground.	–	GND
G5	GND	Ground.	–	GND
G6	GND	Ground.	–	GND
G7	GND	Ground.	–	GND
G8	GND	Ground.	–	GND
G9	GND	Ground.	–	GND
G10	GPIO_1	Strap option	1.8V	I/O
G11	GND	Ground.		GND
H1	SDIO_CMD	SDIO Command Line	1.8V	I/O
H2	SDIO_DATA_0	SDIO Data Line 0	1.8V	I/O

H3	SDIO_DATA_3	SDIO Data Line 3	1.8V	I/O
H4	SDIO_DATA_2	SDIO Data Line 2	1.8V	I/O
H5	GND	Ground.	–	GND
H6	WL_DEV_WAKE	WL DEV_WAKE.	1.8V	I/O
H7	GND	Ground.	–	GND
H8	GND	Ground.	–	GND
H9	RESERVED	Please don’t connect to this pin.	–	–
H10	RESERVED	Please don’t connect to this pin.	–	–
H11	RESERVED	Please don’t connect to this pin.	–	–
J1	SDIO_CLK	SDIO Clock Input	1.8V	I
J2	SDIO_DATA_1	SDIO Data Line 1	1.8V	I/O
J3	GND	Ground.	–	GND
J4	GND	Ground.	–	GND
J5	GND	Ground.	–	GND
J6	GND	Ground.	–	GND
J7	GND	Ground.	–	GND
J8	GND	Ground.	–	GND
J9	RESERVED	Please don’t connect to this pin.	–	–
J10	RESERVED	Please don’t connect to this pin.	–	–
J11	RESERVED	Please don’t connect to this pin.	–	–
K1	GND	Ground.	–	GND
K2	GND	Ground.	–	GND
K3	GND	Ground.	–	GND
K4	GND	Ground.	–	GND
K5	GND	Ground.	–	GND
K6	BT_GPIO_11	BT General Purpose I/O	1.8V	I/O

K7	GND	Ground.	–	GND
K8	GND	Ground.	–	GND
K9	GND	Ground.	–	GND
K10	GND	Ground.	–	GND
K11	GND	Ground.	–	GND
L1	GND	Ground.	–	GND
L2	RESERVED	Please don’t connect to this pin.	–	–
L3	GND	Ground.	–	GND
L4	GND	Ground.	–	GND
L5	C0_ANT	WLAN/BT Main RF TX/RX path.		RF
L6	GND	Ground.	–	GND
L7	GND	Ground.	–	GND
L8	GND	Ground.	–	GND
L9	GND	Ground.	–	GND
L10	C1_ANT	WLAN Aux RF TX/RX path.		RF
L11	GND	Ground.	–	GND

2.3 Host Configuration Interface Table

Pin No	**Definition**	**Interface**	**Strap**
G10	GPIO_1	PCIE	1
		SDIO	0

Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Unit**
VBAT	DC supply for the VBAT and PA driver supply	-0.5	–	6.0	V
VDDIO	DC supply voltage for dig ital I/O	-0.5	–	2.2	V
Tj	Maximum junction tempe rature	–	–	125	°C

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulator	3.135	3.3	3.465	V
VDDIO	DC supply voltage for digi tal I/O	1.71	1.8	1.89	V

3.3 Digital 10 Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Digital I/O pins, VDDIO=1.8V					
VIH	Input high voltage	0.65 × VDDIO	–	–	V
VIL	Input low voltage	–	–	0.35 × VDDIO	V
VOH	Output high voltage	VDDIO – 0.45	–	–	V
VOL	Output Low Voltage	–	–	0.45	V

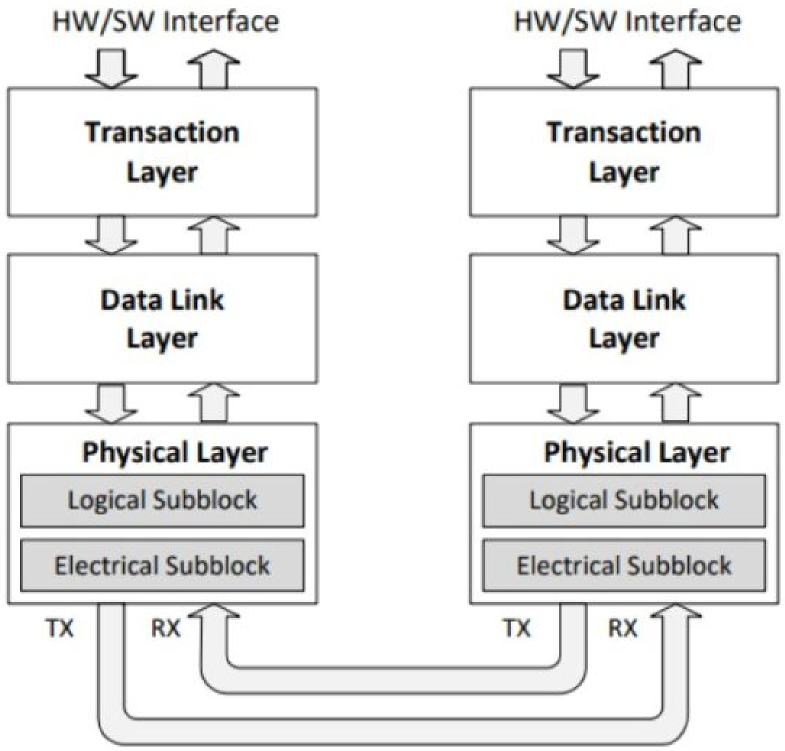
3.4 Host Interface

3.4.1 PCIe Interface

The PCI Express (PCIe) core in AW-XH323 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen2 speeds. This core contains all the necessary blocks, including logical and electrical functional sub blocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

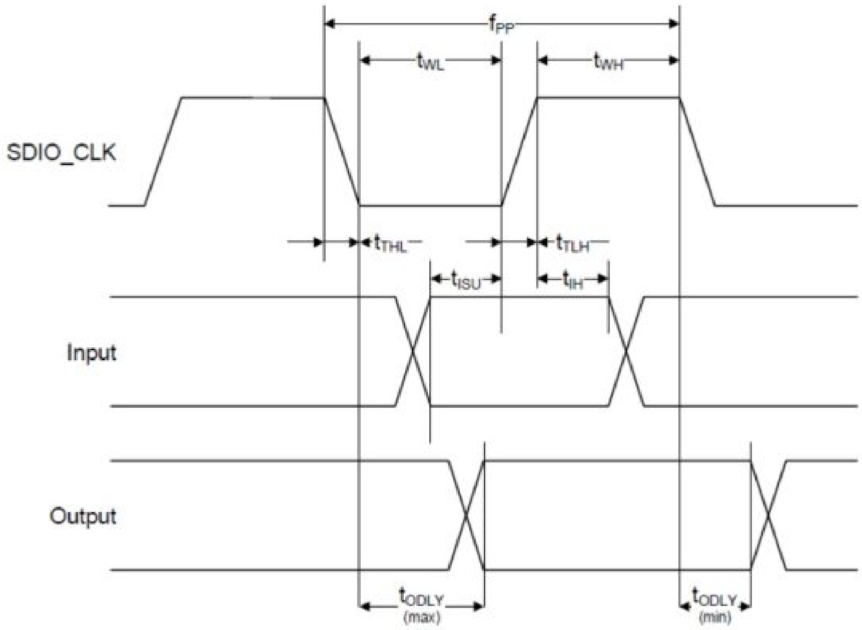
Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in Figure 20. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and AW-XH323 device. The transmit side processes outbound packets whereas the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.



3.4.2 SDIO Interface

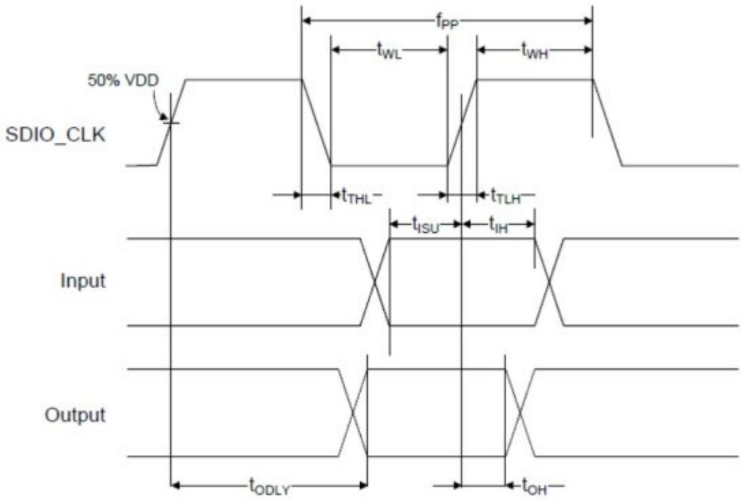
SDIO Bus Timing (Default Mode)



SDIO Bus Timing Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL)					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

SDIO Bus Timing (High-Speed Mode)



SDIO Bus Timing Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL [b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

3.4.3 UART Interface

The AW-XH323 UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The baud rate may be selected through a vendor-specific UART HCI command.

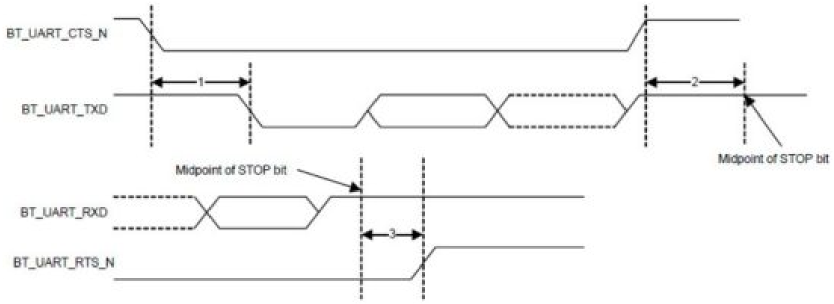
UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth 5.0 UART HCI specification. The default baud rate is 115.2 Kbaud.

The AW-XH323 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-XH323 UARTSs operate correctly with the host UART as long as the combined baud rate error of the two devices is within +2%.

UART Interface Signals

PIN No.	Name	Description	Type
F1	BT_UART_RTS_N	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.	O
F2	BT_UART_CTS_N	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	I
G1	BT_UART_TXD	UART Serial Output. Serial data output for the HCI UART interfac e.	O
G2	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.	I



UART Timing

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high b efore midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT _UART_RTS_N high	–	–	0.5	Bit periods

3.5 Power up Timing Sequence

AW-XH323 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states.

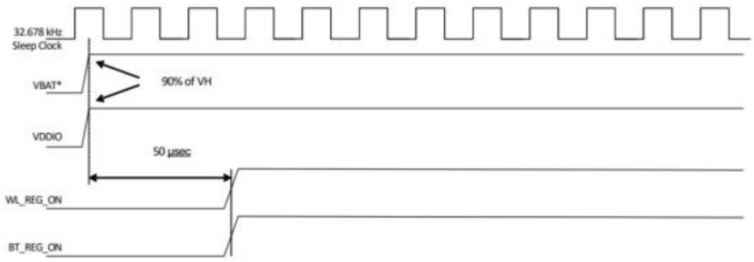
The timing values indicated are minimum required values; longer delays are also acceptable. Description of Control Signals

- WL_REG_ON: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal AW-XH323 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
  If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- BT_REG_ON: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal AW-XH323 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note

- AW-XH323 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating PCIe accesses.
- VBAT and VDDIO should not rise 10%—90% faster than 40 microseconds.

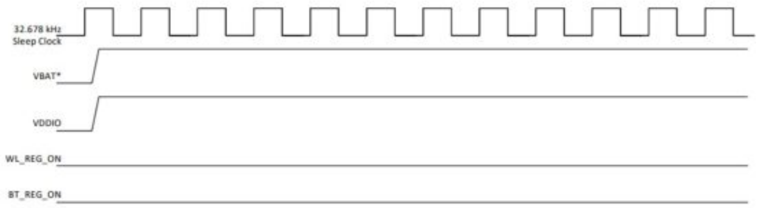
WLAN = ON, Bluetooth = ON



***Notes :**

1. VBAT and VDDIO should not rise 10%-90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

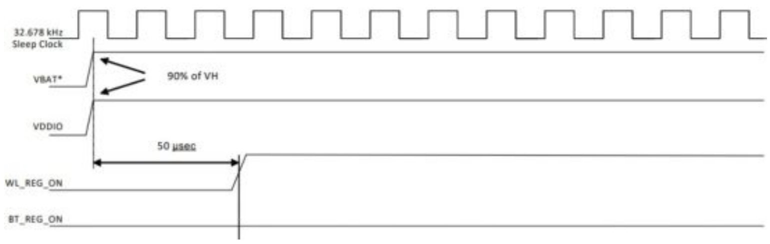
WLAN = OFF, Bluetooth = OFF



***Notes:**

1. VBAT and VDDIO should not rise 10%-90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

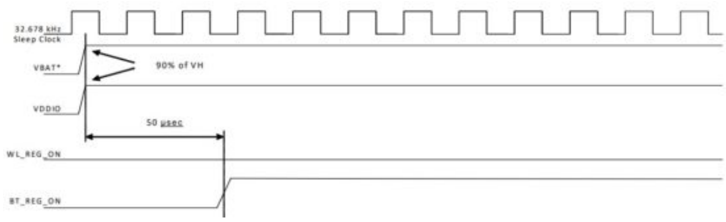
WLAN = ON, Bluetooth = OFF



***Notes:**

1. VBAT and VDDIO should not rise 10%-90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is hi

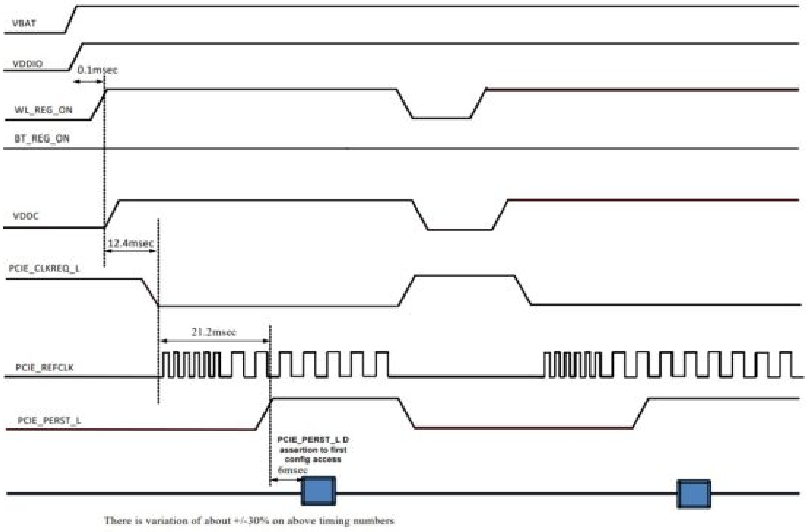
WLAN = OFF, Bluetooth = ON



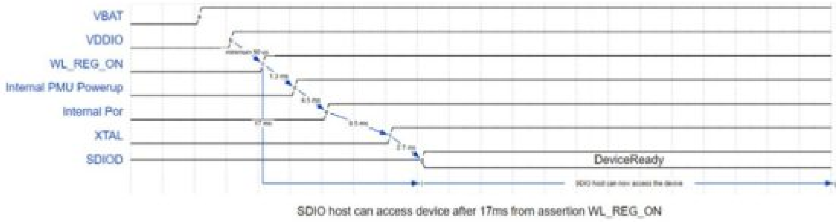
***Notes:**

1. VBAT and VDDIO should not rise 10%-90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN Power-Up Sequence for PCIe Host



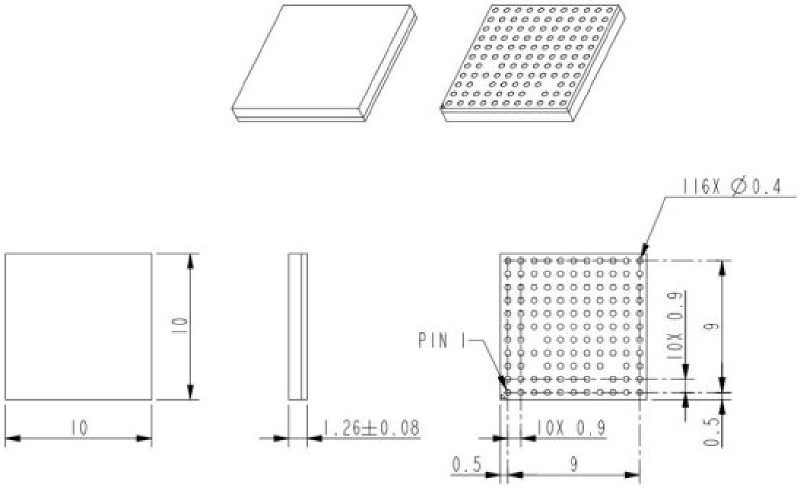
WLAN Boot-Up Sequence for SDIO Host



3.6 Power Consumption'
3.6.1 WLAN
TBD
* The power consumption is based on Azurewave test environment, these data for reference only.
3.6.2 Bluetooth
TBD
* The power consumption is based on Azurewave test environment, these data for reference only.

Mechanical Information

4.1 Mechanical Drawing



Packaging Information

TBD

FCC:

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.
However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Operation of transmitters in the 5.925-7.125 GHz band is prohibited for control of or Communications with unmanned aircraft systems.
Additional testing and certification is necessary when the lowest gain in WLAN operation 6GHz of antennas which may be used in the future that is less than the lowest gain of the original certified for Contention Based Protocol (CBP).

IMPORTANT NOTE:

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

IMPORTANT NOTE:

This module is intended for OEM integrator. This module is only FCC authorized for the specific rule parts listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.
Additional testing and certification may be necessary when multiple modules are used.
OEM integrators that they must use the equivalent antennas or C2PC will be required.
The host manufacturer should reference KDB Publication 996369 D04 Module Integration Guide.

USERS MANUAL OF THE END PRODUCT:
In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied.
The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.
This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.
Operation of transmitters in the 5.925-7.125 GHz band is prohibited for control of or Communications with unmanned aircraft systems.
LABEL OF THE END PRODUCT:
The final end product must be labeled in a visible area with the following " Contains TX FCC ID: TLZ-XH32X".
This equipment complies with FCC mobile radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body.
If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.
This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.
Ant list

Ant.	Brand	Model Name	Antenna Type	Connector	Gain (dBi)
1	ARISTOTLE	RFA-27-JP326MHF4C198	PIFA Antenna	I-PEX	Note1

Note1:

Ant.	Gain (dBi)	
	WLAN 2.4GHz/Bluetooth	**WLAN 5GHz/6GHz**
1	3.5	5

Revision History

Version	Revision Date	Description	Initials	Approved
01	**2023/02/06**	**Initial Version**	**Barry Tsai**	**N.C. Chen**
02	**2024/04/08**	**Update 5.RF trace layout guide**	**Barry Tsai**	**N.C. Chen**

INTRODUCTION
This document provides key guidelines and recommendations to be followed when creating AW-XH323/AW-XH325/AW-XH327 layout. It is strongly recommended that layouts be reviewed by the AzureWave engineering team before being released for fabrication.
The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

- GENERAL RF GUIDELINES
- Ground Layout

- Power Layout
- Digital Interface
- RF Trace
- Antenna
- Antenna Matching
- GENERAL LAYOUT GUIDELINES
- THE OTHER LAYOUT GUIDE INFORMATION

1. GENERAL RF GUIDELINES
Follow these steps for optimal WLAN performance.
A.Control WLAN 50 ohm RF traces by doing the following:

- Route traces on the top layer as much as possible and use a continuous reference ground plane underneath them.
- Verify trace distance from ground flooding. At a minimum, there should be a gap equal to the width of one trace between the trace and ground flooding. Also keep RF signal lines away from metal shields.
- This will ensure that the shield does not detune the signals or allow for spurious signals to be coupled in.
- Keep all trace routing inside the ground plane area by at least the width of a trace.
- Check for RF trace stubs, particularly when bypassing a circuit.

B. Keep RF traces properly isolated by doing the following:

- Do not route any digital or analog signal traces between the RF traces and the reference ground.
- Keep the balls and traces associated with RF inputs away from RF outputs. If two RF traces are close each other, then make sure there is enough room between them to provide isolation with ground fill.
- Verify that there are plenty of ground vias in the shield attachment area. Also verify that there are no non-ground vias in the shield attachment area. Avoid traces crossing into the shield area on the shield layer.

C. Consider the following RF design practices:

- Confirm antenna ground keep-outs.
- Verify that the RF path is short, smooth, and neat. Use curved traces or microwave corners for all turns; never use 90-degree turns. Avoid width discontinuities over pads. If trace widths differ significantly from component pad widths, then the width change should be mitered. Verify there are no stubs.
- Do not use thermals on RF traces because of their high loss.
- The RF traces between AW-XH323/AW-XH325/AW-XH327 CO_ANT pin and C1_ANT pin and antenna must be made using 50Q controlled-impedance transmission line.

2. Ground Layout
Please follow general ground layout guidelines. Here are some general rules for customers' reference.

- The layer 2 of PCB should be a complete ground plane. The rule has to be obeyed strictly in the RF section while RF traces are on the top layer.
- Each ground pad of components on top layer should have via drilled to PCB layer 2 and via should be as close to pad as possible. A bulk decoupling capacitor needs two or more.

- Don’t place ground plane and route signal trace below printed antenna or chip antenna to avoid destroying its electromagnetic field, and there is no organic coating on printed antenna. Check antenna chip vendor for the layout guideline and clearance.
- Move GND vias close to the pads.

3. Power Layout
Please follow general power layout guidelines. Here are some general rules for customers’ reference.

- A 4.7uF capacitor is used to decouple high frequency noise at digital and RF power terminals. This capacitor should be placed as close to power terminals as possible.
- In order to reduce PCB’s parasitic effects, placing more via on ground plane is better.

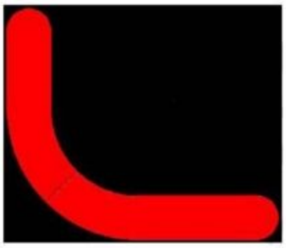
4. Digital Interface
Please follow power and ground layout guidelines. Here are some general rules for customers’ reference.

- The digital interface to the module must be routed using good engineering practices to minimize coupling to power planes and other digital signals.
- The digital interface must be isolated from RF trace.

5. RF Trace
The RF trace is the critical to route. Here are some general rules for customers’ reference.

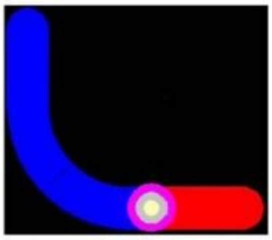
- The RF trace impedance should be 50Q between ANT port and antenna matching network.
- The length of the RF trace should be minimized.
- Toreduce the signal loss, RF trace should laid on the top of PCB and avoid any via on it.
- The CPW (coplanar waveguide) design and the microstrip line are both recommended; the customers can choose either one depending on the PCB stack of their products.
- The RF trace must be isolated with aground beneath it. Other signal traces should be isolated from the RF trace either by ground plane or ground vias to avoid coupling.
- To minimize the parasitic capacitance related to the corner of the RF trace, the right angle corner is not recommended.

If the customers have any problem in calculation of trace impedance, please contact AzureWave



Correct RF trace

Right-angled corner



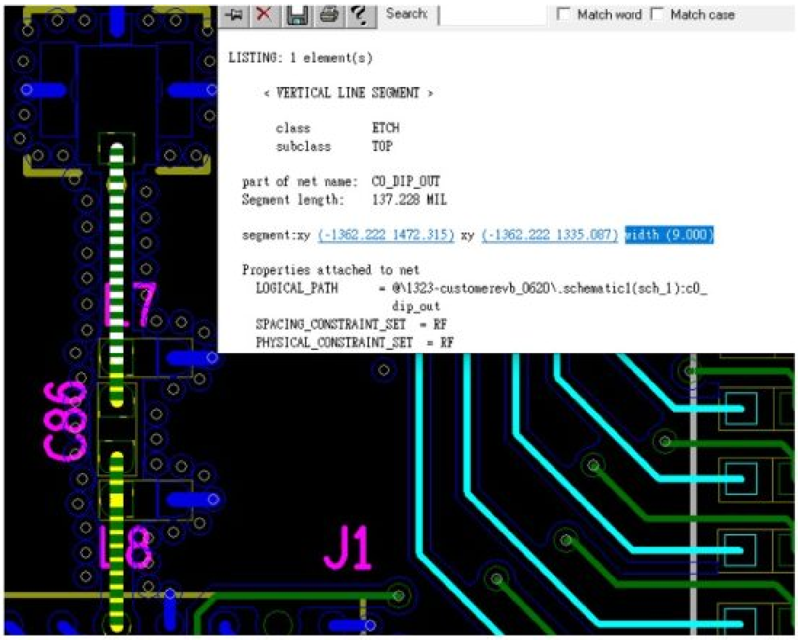
Via on RF trace

Incorrect RF trace

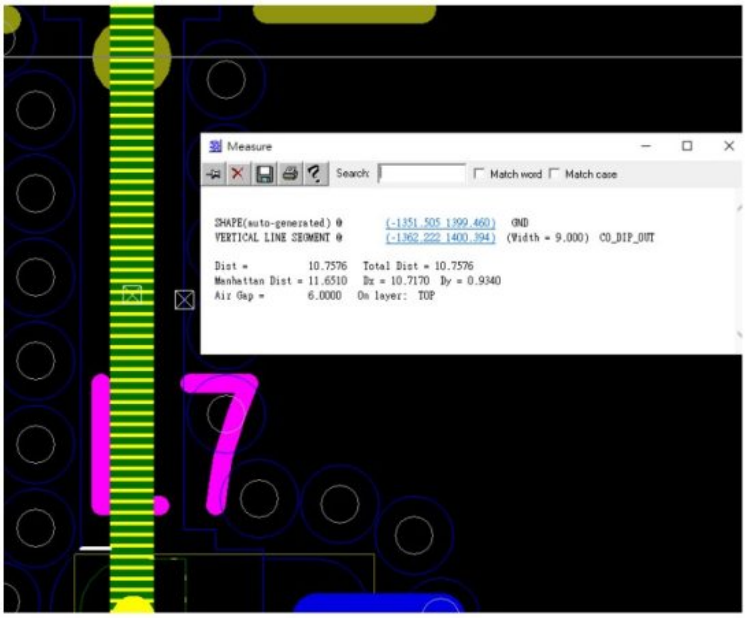
RF Trace Layout Reference:
AW-XH323/AW-XH325/AW-XH327 RF trace should be follow the rules as below

- Line length of Antenna trace about 165.8mi and 110.3 mil

- Line width of Antenna trace about 9 mil



- Air gap between RF trace and ground about 6 mil

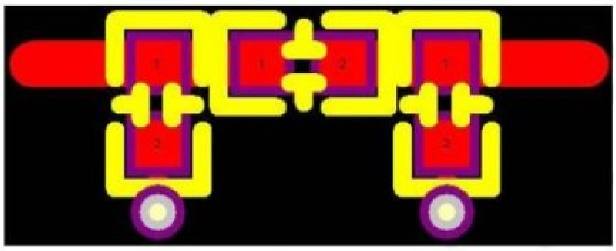


Antenna

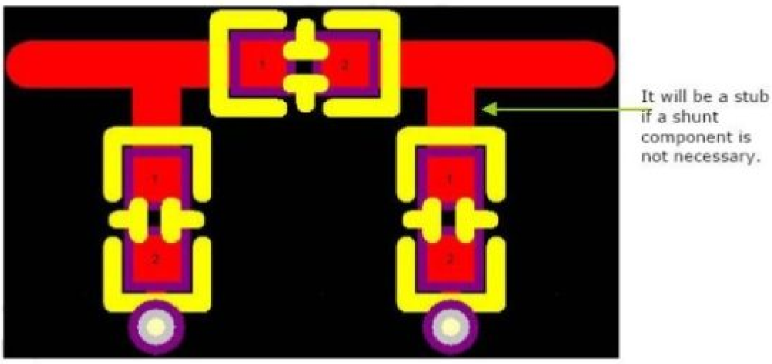
All the high-speed traces should be moved far away from the antenna. For the best radiation performance, check antenna chip vendor for the layout guideline and clearance.

Antenna Matching

PCB designer should reserve an antenna matching network for post tuning to ensure the antenna



Correct layout for antenna matching



Incorrent layut for antenna matching

8. SHIELDING CASE

Magnetic shielding, ferrite drum shielding, or magnetic-resin coated shielding is highly recommended to prevent EMI issues.

9. GENERAL LAYOUT GUIDELINES

Follow these guidelines to obtain good signal integrity and avoid EMI:

A. Place components and route signals using the following design practices:

- Keep analog and digital circuits in separate areas.
- Identify all high-bandwidth signals and their return paths. Treat all critical signals as current performance in different environments. Matching components should be close to each other.
  Stubs should also be avoided to reduce parasitic while no shunt component is necessary after tuning.loops.

Check each critical loop area before the board is built. A small loop area is more important than short trace lengths.

- Orient adjacent-layer traces so that they are perpendicular to one another to reduce crosstalk.
- Keep critical traces on internal layers, where possible, to reduce emissions and improve immunity to external noise.
- However, RF traces should be routed on outside layers to avoid the use of vias on these traces.
- Keep all trace lengths to a practical minimum. Keep traces, especially RF traces, straight wherever possible. Where turns are necessary, use curved traces or two 45-degree turns.
  Never use 90-degree turns.

B. Consider the following with respect to ground and power supply planes:

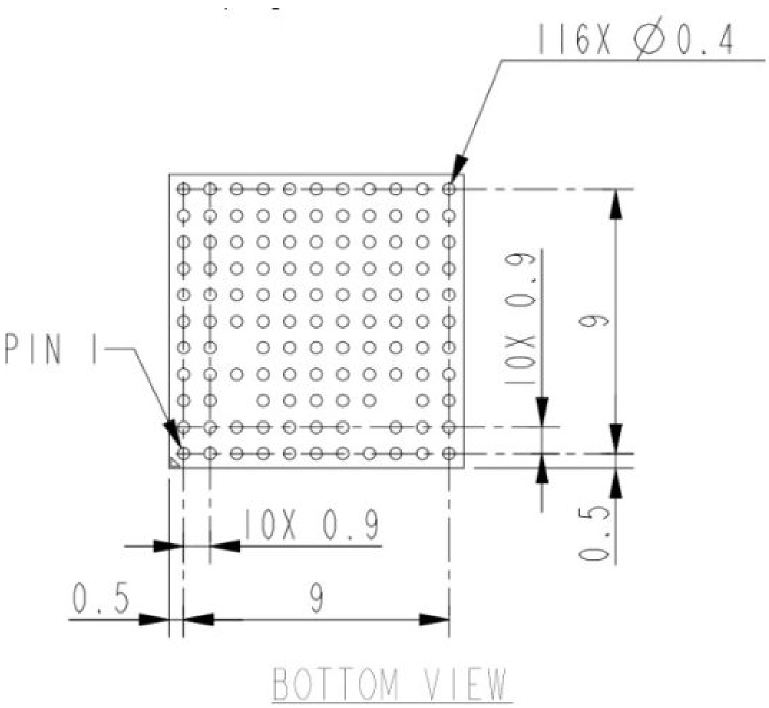
- Route all supply voltages to minimize capacitive coupling to other supplies. Capacitive coupling can occur if supply traces on adjacent layers overlap. Supplies should be separated from each other in the stack-up by a ground plane, or they should be coplanar (routed on different areas of the same layer).
- Provide an effective ground plane. Keep ground impedance as low as possible. Provide as much ground plane as possible and avoid discontinuities. Use as many ground vias as possible to connect all ground layers together.
- Maximize the width of power traces. Verify that they are wide enough to support target currents, and that they can do so with margin. Verify that there are enough vias if the traces need to change layers.

C. Consider these power supply decoupling practices:

- Place decoupling capacitors near target power pins. If possible, keep them on the same side as the IC they decouple to avoid vias that add inductance. If a filter component cannot be directly connected to a given power pin with a very short and fat etch, do not connect it by a copper trace. Instead, make the connection directly to the associated planes using vias.
- Use appropriate capacitance values for the target circuit, and consider each capacitor's self-resonant frequency.

10. Stamp Module stencil and Pad opening Suggestion

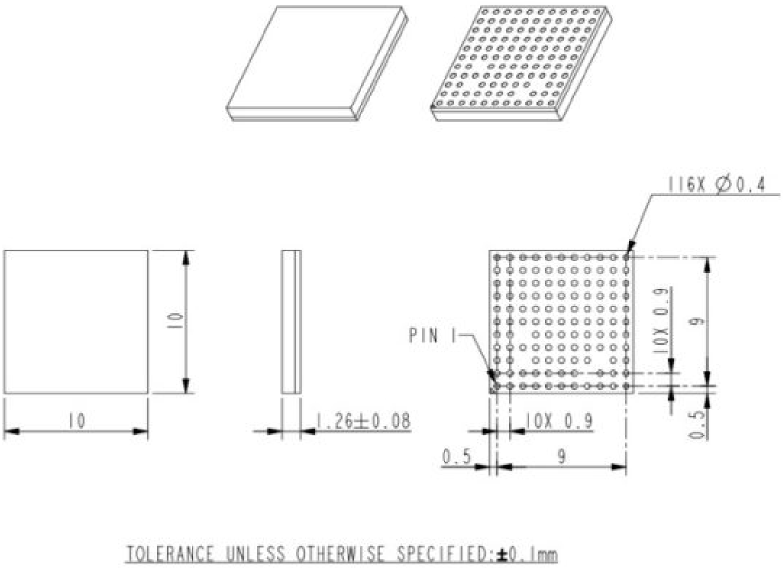
- Stencil thickness : 0.12~0.15mm
- Function Pad opening size suggestion: Max. 1:1
  PS: This opening suggestion just for customer reference, please discuss with AzureWave's Engineer before you start SMT.
- 10x10mm Solder Printer Opening Reference:



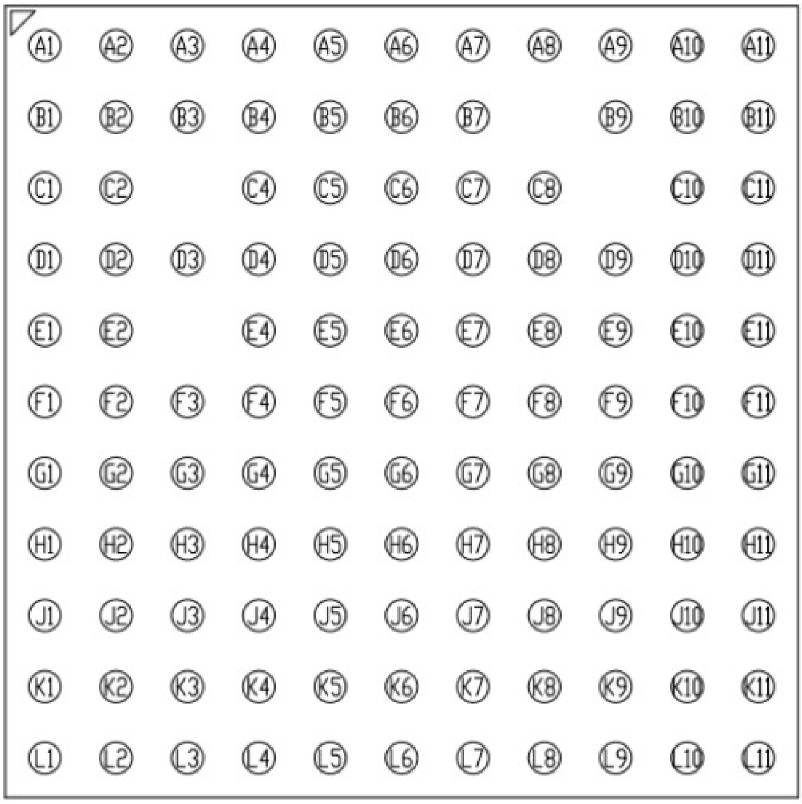
11. The other layout guide Information

- Make sure every power traces have good return path (ground path).
- Connect the input pins of unused internal regulators to ground.
- Leave the output pins of unused internal regulators floating.
- High speed interface (i.e. UART/SDIO/HSIC) shall have equal electrical length. Keep them away from noise sensitive blocks.
- Good power integrity of VDDIO will improve the signal integrity of digital interfaces.
- Good return path and well shielded signal can reduce crosstalk, EMI emission and improve signal integrity.
- RF 10 is around 50 ohms, reserve Pi or T matching network to have better signal transition from port to port.
- Smooth RF trace help to reduce insertion loss. Do not use 90 degrees turn (use two 45 degrees turns or one miter bend instead).
- Well arranged ground plane near antenna and antenna itself will help to reduce near field coupling between other RF sources (e.g. GSM/CDMA … antennas).
- Discuss with AzureWave Engineer after you finish schematic and layout job.

12. Mechanical Drawing
Package Outline Drawing

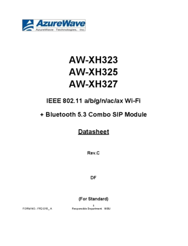


Bottom View of PCB Layout Foot Print



AzureWave
AzureWave Technologies, Inc.

Documents / Resources

 AW-XH323 AW-XH325 AW-XH327 IEEE 802.11 a/b/g/n/ac/ax Wi-Fi + Bluetooth 5.3 Combo SIP Module Datasheet Rev. C DF (For Standard)	AzureWave AW-XH323 PUR Wi-Fi Plus Bluetooth 5.2 Combo SIP Module [pdf] Owner's Manual AW-XH323 PUR Wi-Fi Plus Bluetooth 5.2 Combo SIP Module, AW-XH323, PUR Wi-Fi Plus Bluetooth 5.2 Combo SIP Module, Bluetooth 5.2 Combo SIP Module, 5.2 Combo SIP Module, SIP Module, Module

References

- User Manual