




AzureWave AW-CU484 IEEE 802.15.4 and Bluetooth LE 5.0 wireless microcontroller Stamp LGA Module User Guide

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AW-CU484 IEEE 802.15.4 and Bluetooth LE 5.0 wireless microcontroller Stamp LGA Module Layout Guide Rev. A

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Revision History

Version	Revision Date	Description	Initials	Approved
A	2020/9/7	• Initial Version	Chihuahua Huang	N.C. Chen

INTRODUCTION

This document provides key guidelines and recommendations to be followed when creating the AWC484 layout. It is strongly recommended that the layout be reviewed by the AzureWave engineering team before being released for fabrication. The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

- Ground Layout
- Power Layout
- Digital Interface
- RF Trace
- The other layout guide Information
- Module stencil and Pad opening Suggestions

Ground Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

1. The top layer of the customer platform should keep the complete ground plane as much as possible as you can, in order to be connected to all ground pins of AW-CU484 module.
2. The area under our module forbade any trace and via on the top layer of the customer platform.

Power Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

1. Power traces shall surround the ground to get stable and make sure all power traces have a good return path to the ground.
2. Do not get close to digital traces (SDIO.USB) or continuous data traces, there could be coupling noise affecting power traces and IC.

Digital Interface

Please follow power and ground layout guidelines. Here are some general rules for customers' reference.

1. The digital interface to the module must be well routed to minimize coupling to power planes and other digital signals.
2. SDIO and UART Traces need GND surrounded.
3. SDIO pin can add pull high resistor on traces close WIFI module.(reserved solution)

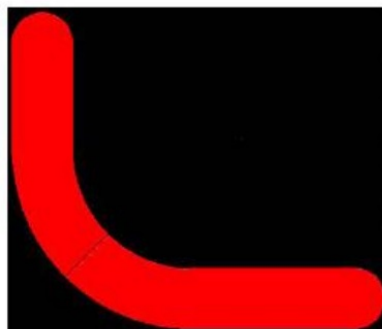
4. SDIO and UART traces between host and module are shot as possible.
5. SDIO Traces length between host and module is equal as possible.
6. SDIO & UART traces as possible away from the CLOCK signal

RF Trace

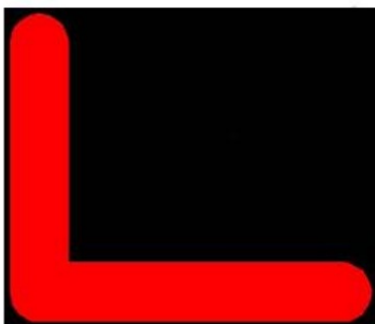
The RF trace is critical to the route. Here are some general rules for customers' reference.

1. The RF trace impedance should be 50Ω between the ANT port and the antenna matching network.
2. The length of the RF trace should be minimized.
3. To reduce the signal loss, RF trace should be laid on the top of PCB and avoid any via on it.
4. The CPW (coplanar waveguide) design and the microstrip line are both recommended; the customers can choose either one depending on the PCB stack of their products.
5. The RF trace must be isolated with a ground beneath it. Other signal traces should be isolated from the RF trace either by ground plane or ground vias to avoid coupling.
6. To minimize the parasitic capacitance related to the corner of the RF trace, the right angle corner is not recommended.

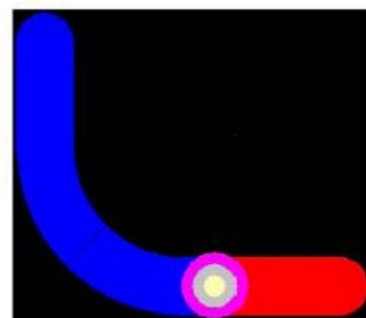
If the customers have any problems in the calculation of trace impedance, please contact Azurewave.



Correct RF trace



Right-angled corner



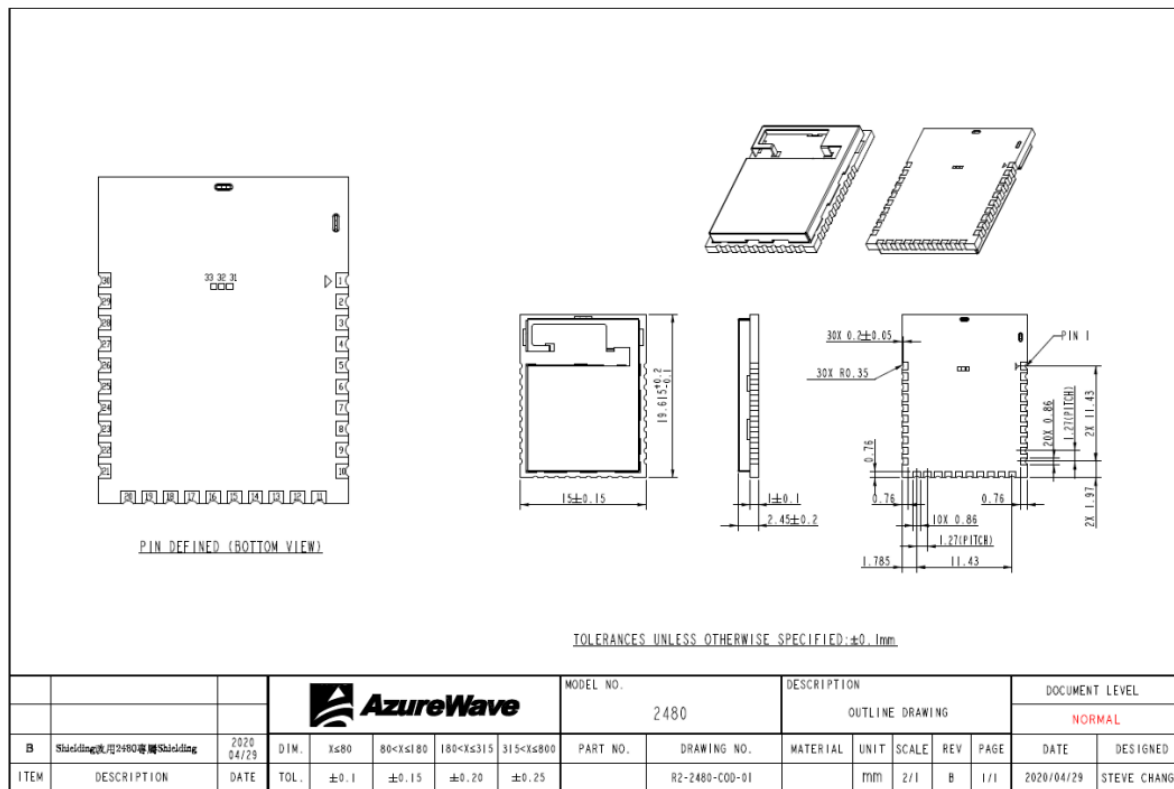
Via on RF trace

Incorrect RF trace

The other layout guide Information


- Keep the module's unused function pins floating.
- High-speed interface (i.e. UART/SDIO/HSIC) shall have equal electrical length. Keep them away from noise-sensitive blocks.

Mechanical Drawing



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Documents / Resources

 <p>AW-CU484</p> <p>IEEE 802.15.4 and Bluetooth LE 5.0 wireless microcontroller Stamp LGA Module</p> <p>Layout Guide</p> <p>Rev. A</p>	<p>AzureWave AW-CU484 IEEE 802.15.4 and Bluetooth LE 5.0 wireless microcontroller Stamp LGA Module [pdf] User Guide</p> <p>AW-CU484, IEEE 802.15.4 and Bluetooth LE 5.0 wireless microcontroller Stamp LGA Module</p>
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