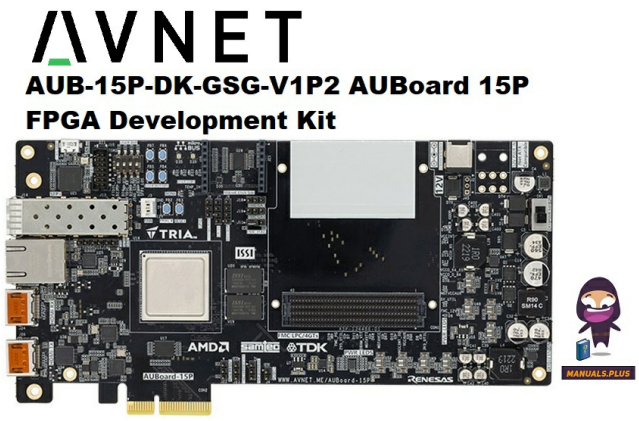

Avnet AUB-15P-DK-GSG-V1P2 AUBoard 15P FPGA Development Kit User Guide

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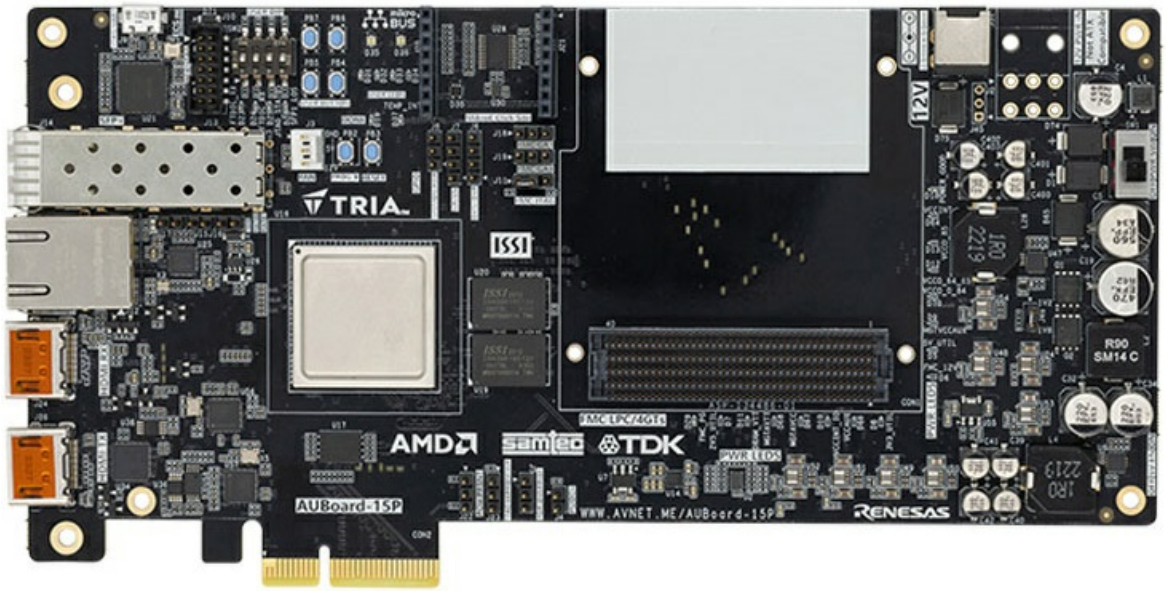

Specifications

- Product Name: AUBoard-15P Development Kit
- Version: 1.2
- LIT#: AUB-15P-DK-GSG-V1P2
- Expansion Connectors: FMC (FPGA Mezzanine Card)
- Processor: Artix UltraScale+ FPGA
- Interface: PCIe Gen4 x4

Product Usage Instructions

What's In The Box

The AUBoard-15P Development Kit includes the AUBoard-15P PCIe Gen4 x4 board. In the box, you will find:

- AUBoard-15P Development Kit board
- Micro-B USB cable
- Ethernet cable
- SFP+ cable
- HDMI cables

Note: Customers may need to acquire additional cables and modules based on their specific application requirements.

Getting Started Guide

The Getting Started Guide will help you set up the hardware for the AUBoard-15P Development Kit and run the Out-of-Box FreeRTOS application. Follow these steps:

1. Connect the necessary cables (USB, Ethernet, SFP+, HDMI) to the appropriate ports on the board.
2. Power on the board using the provided power source.
3. The Out-of-Box image is pre-programmed into the QSPI at the factory. This allows you to quickly bring up the

board with a network connection.
4. Run an application built using FreeRTOS to test the functionality of the board.

Online Resources

For additional documentation, tutorials, and reference designs, visit the following websites:

- element14
- Hackster.io

Document Control

- Document Version: 1.2
- Document Date: 5 February 2025.

Version History

Version	Date	Comment
1.0	10/28/2024	Initial Release
1.1	01/14/2025	Updated with production photos
1.2	02/05/2025	Updated Website Links

Pertinent Info

- The AUBoard-15P Development Kit is a solution that incorporates an Artix UltraScale+ on a PCIe Gen4 x4 board targeted for broad use in many applications:
- Offers an AMD based Development Kit in Commercial (0ºC to 70ºC) temperature grade for engineers to adopt in development, proof-of-concept, and production projects.
- Combines programmable logic designs with a MicroBlaze soft microprocessor core in a convenient and expandable board.
- Allows expansion to a variety of sensors and peripherals through the Mikroe Click Board™ and FMC (FPGA Mezzanine Card) expansion connectors.
- The following figure is a high-level block diagram of the AUBoard-15P Development Kit and the peripherals attached to the Artix UltraScale+ FPGA.

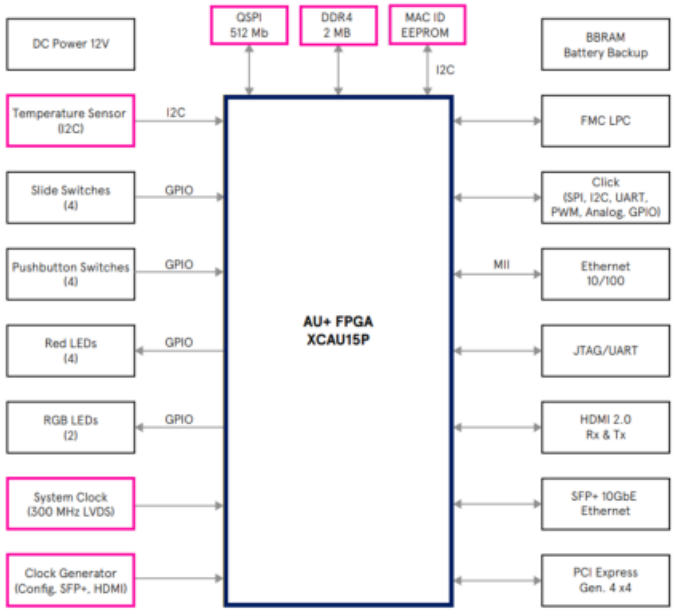

Figure 1 – Development Kit Block Diagram

- The following figure provides an overview of the physical connections, their designators, and relative position on the AUBoard-15P Development Kit. This image is of the production version of the AUBoard-15P Development Kit but the components depicted are still in there relevant locations

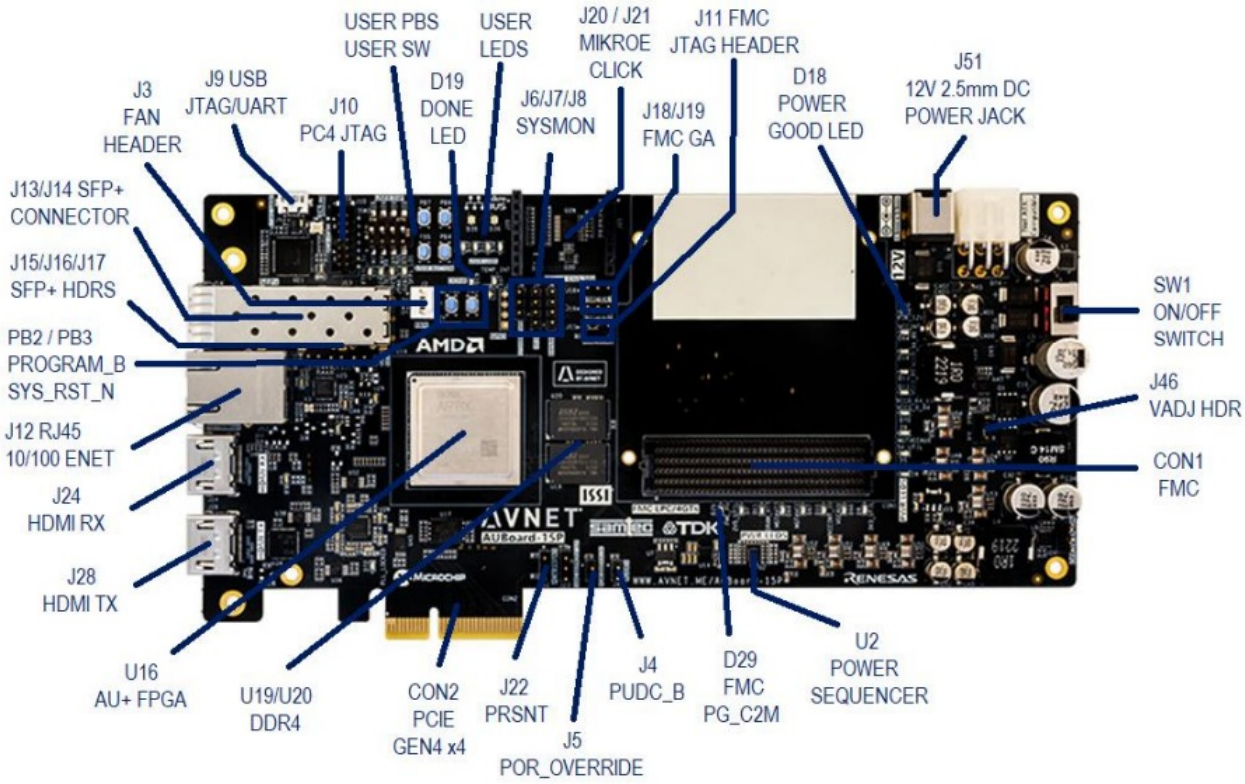

Figure 2 – Interfaces and Connectors

- The Getting Started Guide will outline the steps to setup the AUBoard-15P Development Kit hardware and documents the procedure to run the Out-of-Box FreeRTOS
- **What's In The Box**
- The AUBoard-15P Development Kit includes the AUBoard-15P PCIe Gen4 x4 board. The AUBoard-15P Development Kit includes the following in the box:

AUBoard-15P PCIe Gen4 x4 board

- Power Supply
- Quick Start Card
- PCIe Bracket

Customers may need to acquire a micro-B USB cable, Ethernet cable, SFP+ cable, and HDMI cables depending on their end application. Customers will also need to procure or produce appropriate modules that target the various expansion interfaces. Here are links to web pages that provide such products:

- MikroE Click Boards: **https://www.mikroe.com/click**
- FMC: **https://www.xilinx.com/products/boards-and-kits/fmc-cards.html**

This is not an exhaustive list of available off-the-shelf products targeting the expansion connectors, but should provide a userwith an idea of the available products that could be leveraged.

What's On The Web

- The AUBoard-15P Development Kit has documentation that is made available to users through the Avnet Board product page, element14, and Hackster.io community websites. Here are links to the various online content:
- **http://avnet.me/auboard-15p**
- **http://avnet.me/auboard-15p-forum**
- **http://avnet.me/board-support-site**

Available Documentation

- Getting Started Guide
- Hardware User Guide
- Board Definition Files
- Master User Constraint File
- Net Length Report
- Schematics
- Bill of Materials
- Mechanical Drawing
- 3D Model
- Source Databases

Denotes FAE involvement to gain access to these documents. Contact your local Avnet FAE.
Denotes FAE involvement and execution of Non-Disclosure Agreement (NDA). Contact your local Avnet FAE.

Tutorials and Reference Designs

- Any tutorials and reference designs that are available to targets this platform can be located at the links below.
- FreeRTOS Out-of-Box Design
- MicroBlaze RISC-V Petalinux Design
- HDMI Pass-Thru Example Design

- Avnet Boards Training and Courses
  - **http://avnet.me/tria-boards-training**

Trainings and Videos

- Any trainings and videos that may be available to target this platform can be located at the links below.
- Community based boards trainings and videos
  - **http://avnet.me/community-boards-training**
- **Getting Started**
- The functionality of the AUBoard-15P Development Kit is determined by the application configured from the non-volatile memory. In the case of the AUBoard-15P Development Kit the main configuration option is the on-board QSPI. For this Getting Started tutorial, the Out-of-Box image has been programmed into the QSPI at the factory. Having the QSPI pre-programmed allows the end user to quickly bring up the board with a network connection and run an application built using FreeRTOS.
- Reminder: In addition to the items included in the box, you will also need the following to complete the Getting Started tutorial.
- Micro-B USB Debug Cable for USB-UART Communications
- Open Ethernet Port on Network Router or Network Switch, Ethernet Cable

Out-of-Box Example Design

- The AUBoard-15P Development Kit has a FreeRTOS design that is utilized as its Out-of-Box experience. This FreeRTOS design is programmed to the on-board QSPI at the factory. Here is a link to the FreeRTOS Out-of-Box design that could alternatively be used when configuring the FPGA via JTAG.
- **http://avnet.me/auboard-15p-dk-oob**

Hardware Setup
There are a few tasks required to ensure the hardware is set up appropriately to run the Out-of-Box FreeRTOS design.

1. Check that the appropriate headers are shunted on the AUBoard-15P Development Kit.
   - The first header to review is the VCCO_66_86 voltage select header, J46, which determines if the voltage placed on VCCO Bank 66 and VCCO Bank 86. This voltage select header, J46, is used to select +1.8V or +1.2V for the +VCCO_66_86 rail on the AUBoard-15P Development Kit.
   - For +VCCO_66_86 to be set to +1.8V by shunting pin 1 to pin 2 on J46.
   - For +VCCO_66_86 to be set to +1.2V do not place a shunt on J46.
   - The second set of headers to review is the PUDC_B header, J4, and the POR_OVERRIDE header, J5. The PUDC_B header controls the state of the SelectIO from power-on until configuration completes on the Artix UltraScale+ device. The POR_OVERRIDE header controls the power-on reset delay before configuration begins for the Artix UltraScale+ device.
   - For PUDC_B header J4 not shunted pulls up this signal disabling internal pull-up resistors on SelectIO pins. SelectIO will be 3-stated after-power when PUDC is high.
   - For PUDC_B header J4 shunted pin 1 to pin 2 pulls down the PUDC_B signal enabling internal pull-up resistors on SelectIO pins.

- For POR_OVERRIDE header J5 shunted pin 1 to pin 2 pulls up this signal shortening the power-on-delay as specified in the Artix UltraScale+ data sheet. Note: Header J5 should be shunted.
- For POR_OVERRIDE header J5 shunted pin 3 to pin 2, pulls down this signal, elongating the power-on-delay. Note: Header J5 should be shunted.
- Note: POR_OVERRIDE J5 should be default shunted pin 3 to pin 2 connecting POR_OVERRIDE to GND unless the flash will always be ready as soon as the FPGA is powered up.
- The next header to review is the FMC JTAG header, J11, and the FMC General Address (GA0/GA1) headers, J18 and J19. The FMC header controls the inclusion of the FMC JTAG signals into the JTAG chain. The FMC General Address headers sets the I2C addresses on the FMC Mezzanine Card.
- For FMC JTAG header J1,1, shunted pin 1 to pin 2, the JTAG chain will only include the FPGA and cards plugged into the FMC header may not be visible to the JTAG chain.
- For FMC JTAG header J1,1 shunted pin 3 to pin 2, the JTAG chain will include both the FPGA and any devices on the JTAG chain that are included on the FMC card plugged into the FMC connector, CON1.
- Header J18 and J19 can be pulled high by shunting from pin 1 to pin 2 or can be pulled low by shunting from pin 3 to pin 2.
- The last header to review is the MAC ID EEPROM Write Protect header, J23. The MAC ID EEPROM Write Protect header when enabled prevents write accesses from corrupting the MAC ID EEPROM contents.
- For MAC ID EEPROM Write Protect header J23 shunted pin 1 to pin 2, pulls up the Write Protect function and it will be enabled on the MAC ID EEPROM.
- For MAC ID EEPROM Write Protect header J23 shunted pin 3 to pin 2 pulls down the Write Protect function, and writes to the MAC ID EEPROM can occur.
- **Note:** This list calls out important headers and may not document all available options. Please review the AUBoard-15P Development Kit User Guide for the full list of header documentation.

2. The appropriate cables should be attached to the AUBoard-15P Development Kit. The cables required to run the Out-Of-Box design are as follows:
    - Ethernet Cable should be attached from host PC ethernet interface to the AUBoard-15P Development Kit RJ45 connector, J12.
    - microUSB Cable should be attached from host PC USB interface to the AUBoard-15P USB JTAG/UART connector, J9.
    - Attach the provided barrel jack power supply (or connect board to a powered PCIe Card Edge) to the AUBoard-15P Development Kit Power Supply connector, J51

The following figure depicts the fully connected AUBoard-15P Development Kit ready to run the Out-of-Box Design. The image depicted here is a production version of the AUBoard-15P Development Kit.

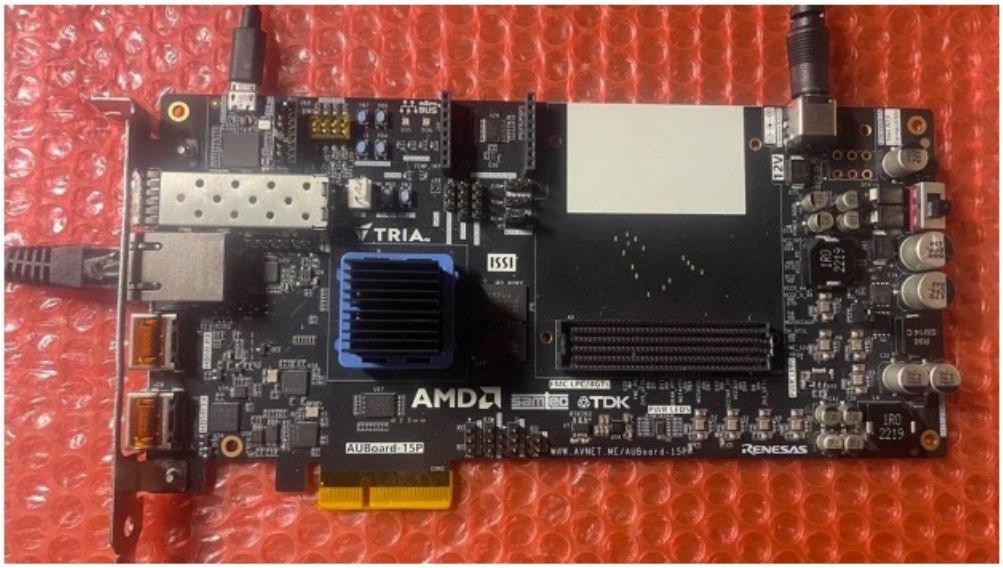

Figure 3 – Cable Locations on AUBoard-15P

Terminal Setup

1. A terminal program is required. Tera Term was used in this example which can be downloaded from the Tera Term project. Install Tera Term or another terminal program of your choice to a host Windows PC.
   - https://teratermproject.github.io/index-en.html
2. When a microUSB cable is connected to the AUBoard-15P Development Kits USB JTAG/UART port J9 from your host Windows PC with the board having been powered on by toggling switch SW1 to ON, the proper drivers, if installed, will give you confirmation of the available COM ports in the Device Manager of Windows as show in the following figure.

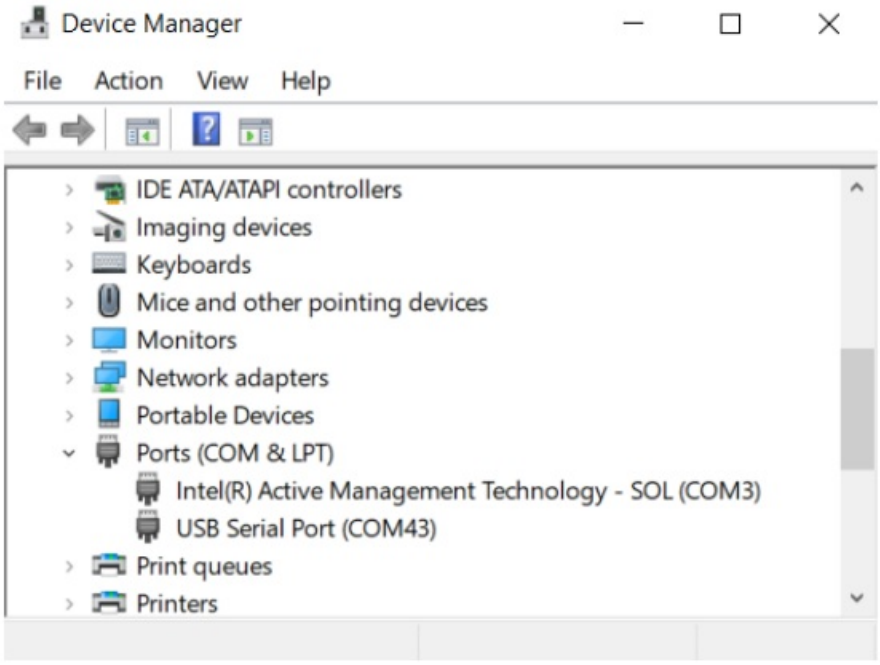

Figure 4 – USB-JTAG/UART COM Port Assignments

3. If the drivers are not installed, then you must manually install the driver for the FT2232H device. Visit the FTDI website and download the appropriate driver for your operating system.
   - http://www.ftdichip.com/Drivers/VCP.htm
4. Prior to installing drivers manually, you should power off the board by toggling switch SW1 to off and then

unplug the microUSB cable from the AUBoard-15P Development Kit. After the Kit is unplugged from the PC, you can unzip and install the FT2232H driver.

5. At this point you should reboot your PC and then proceed to plug in the microUSB cable for the USB JTAG/UART to J9.

Boot FreeRTOS

- Before booting the FreeRTOS Out-of-Box Example Design, we need to ensure that the network connection that we are using for this design is set up properly for ethernet communication to occur.
- For the Out-of-Box Design to function properly, we need to have the IP address of the AUBoard-15P Development Kit set by a DHCP server. The assignment of the IP address should automatically be accomplished on most networks using a Network Router or Network Switch.
- With the AUBoard-15P Development Kit setup and the IP address able to be assigned automatically by the DHCP server, it is now time to boot the FreeRTOS Out-of-Box Design on the AUBoard-15P Development Kit by toggling switch SW1 to ON. The board will start to boot and complete with the terminal appearing as follows

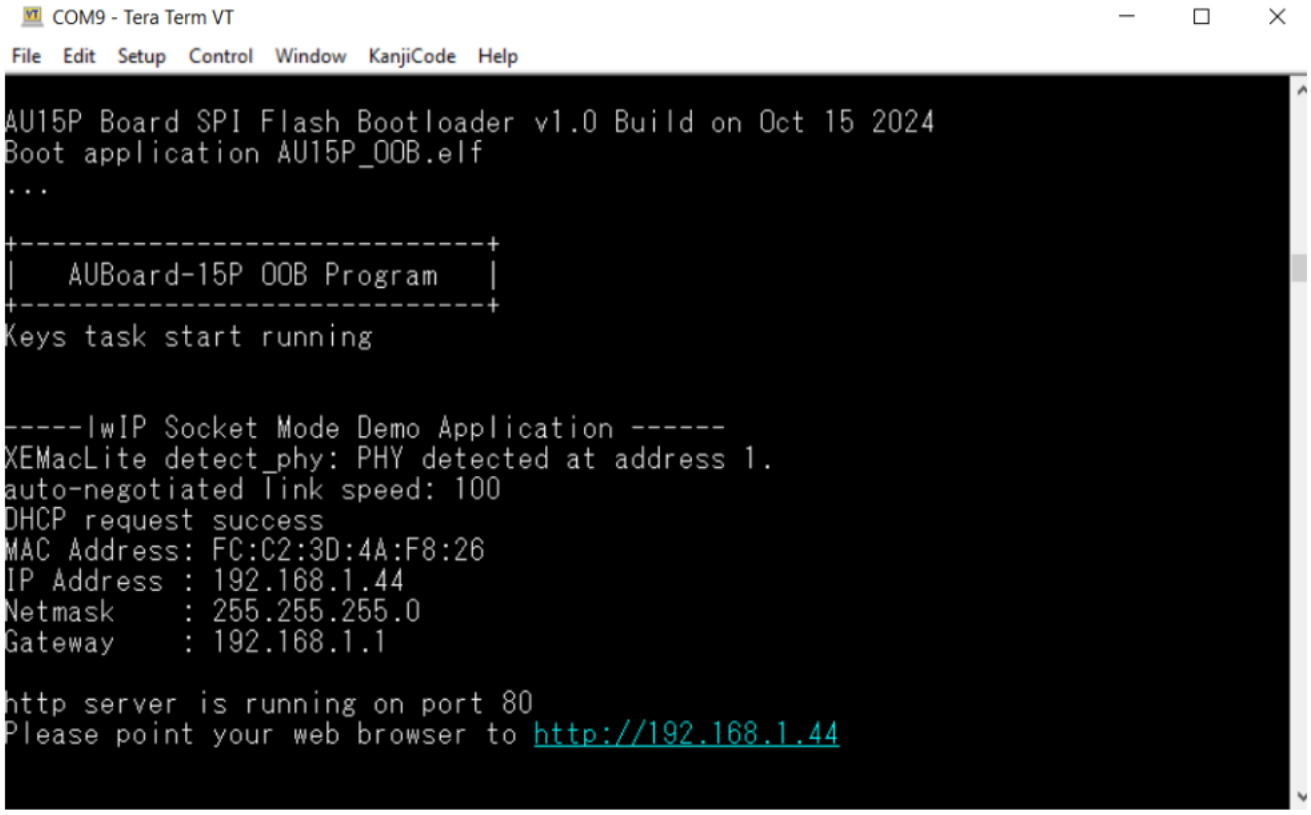

Figure 5 – Out-of-Box Design Boot

Using Out-of-Box Example Design

- At this point, it is time to utilize the Out-of-Box Example Design. Open your favourite web browser and point the browser to the assigned IP address displayed in the terminal window.
- If everything has been successful to this point, the user will see the following web page in the web browser:

Figure 6 – Out-of-Box Design Web Server Page

- In the webpage GUI, the user will be able to toggle the USER RGB LEDs (D35 and D36) of the AUBoard-15P Development Kit showing communication and control over ethernet of the board. The user will be able to set toggle the USER LEDs ON and OFF via buttons in the LED TAB of the webpage. The user will also be able to toggle the USER SWITCH SW2 values and read them back via the GUI

Figure 7 – Webserver Board Control Interfaces

On board, the user will be able to toggle the various User Push Buttons on the board (PB4, PB5, PB6, and PB7) which will in turn cause the User RED LEDs (D31, D32, D33, and D34) to toggle ON and OFF.

- Pressing PB7 – Toggle D34 RED LED.
- Pressing PB6 – Toggle D33 RED LED.
- Pressing PB5 – Toggle D32 RED LED.
- Pressing PB4 – Toggle D31 RED LED.
- Pressing PB2 – Will cause the FPGA to reconfigure (PROG_B control).

Getting Started Complete

- That completes this tutorial. The user may now power down the AUBoard-15P Development Kit by toggling power slide switch SW1 to the off position.

Getting Help and Support

- If additional support is required, TRIA Technologies has many avenues to search depending on your needs.
- For general questions regarding AUBoard-15P Development Kit, please visit our website at http://avnet.me/auboard-15p. Here you can find any available documentation, technical specifications, videos and tutorials, reference designs, and other support.

- Detailed questions regarding AUBoard-15P Development Kit hardware design, software application development, using AMD tools, training and other topics can be posted on the AUBoard-15P Development Kit.
- Support Forum at **http://avnet.me/auboard-15p-forum**. Avnet's technical support team monitors the forum during normal business hours in North America.
- Those interested in customer-specific options on AUBoard-15P Development Kit can send inquiries to **customize@avnet.com**.

FAQ

- **Q: What do I do if I need additional products for the expansion connectors?**
  - A: You can explore off-the-shelf products targeting the expansion connectors or contact your local Avnet FAE for assistance.
- **Q: How can I access tutorials and reference designs for this platform?**
  - A: Tutorials and reference designs can be found at**http://avnet.me/tria-boards-training.**

Documents / Resources

	**Avnet AUB-15P-DK-GSG-V1P2 AUBoard 15P FPGA Development Kit** [pdf] User Guide AUB-15P-DK-GSG-V1P2, AUB-15P-DK-GSG-V1P2 AU Board 15P FPGA Development Kit, AU B-15P-DK-GSG-V1P2, AU Board 15P FPGA Development Kit, Board 15P FPGA Development Kit, 15P FPGA Development Kit, FPGA Development Kit, Development Kit, Kit

References

- avnet.me/auboard-15p-dk-oob
- AUBoard 15P - element14 Community
- Hackster.io - The community dedicated to learning hardware.
- Avnet Boards Training - element14 Community
- Hackster.io - The community dedicated to learning hardware.
- Avnet Boards Training - element14 Community
- Tera Term Open Source Project
- User Manual