

Digilent Arty A7-100T

Digilent Arty A7-100T Artix-7 FPGA Development Board User Manual

Model: Arty A7-100T (410-319)

1. INTRODUCTION

The Digilent Arty A7-100T is a versatile Field Programmable Gate Array (FPGA) development board designed for makers and hobbyists. It features the Xilinx Artix-7 XC7A100TCSG324-1 FPGA, offering a powerful platform for digital circuit design, embedded systems development, and various custom hardware projects. This manual provides essential information for setting up, operating, and maintaining your Arty A7-100T board.

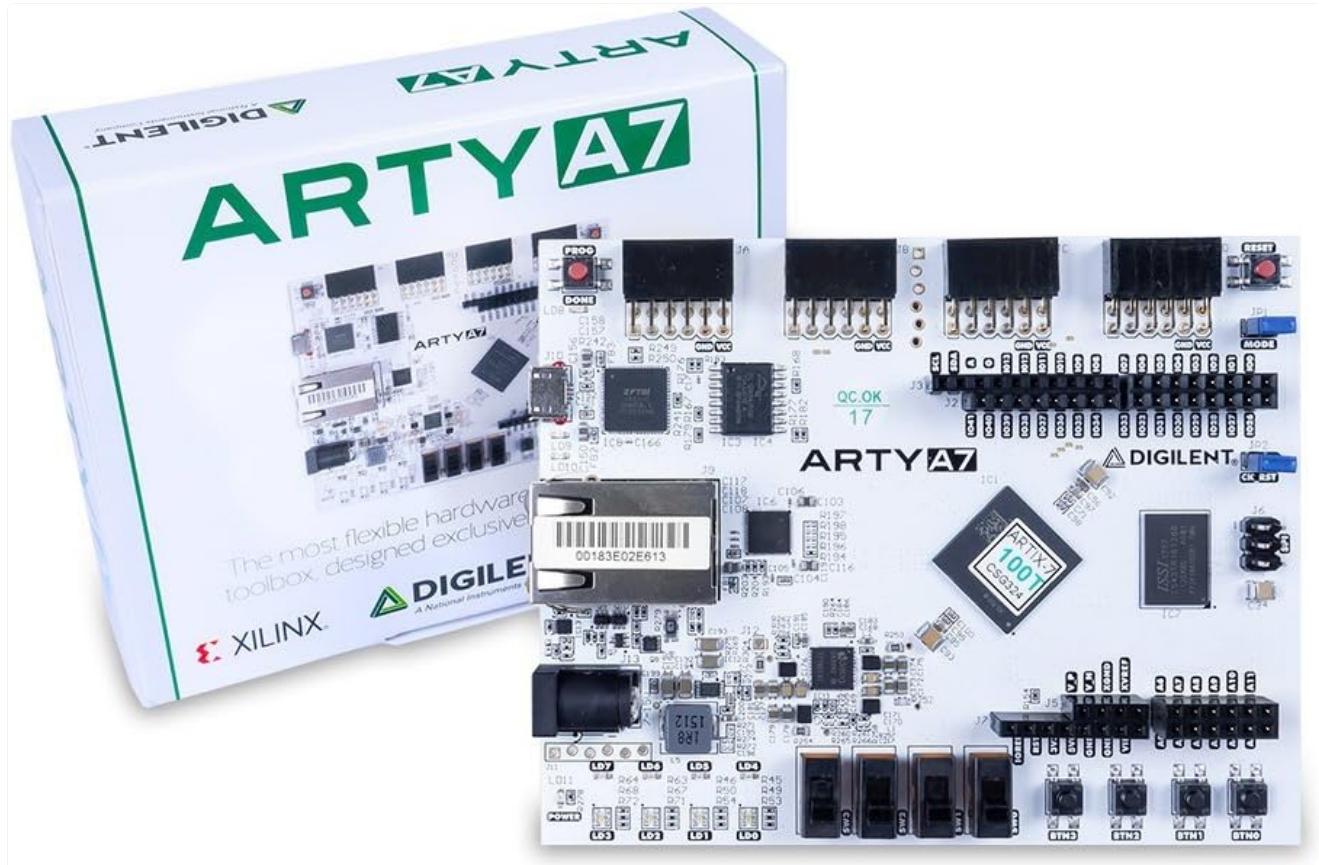


Figure 1: Digilent Arty A7-100T FPGA Development Board and its retail packaging.

2. KEY FEATURES

The Arty A7-100T board is equipped with a range of features to support diverse development needs:

- **FPGA:** Xilinx Artix-7 XC7A100TCSG324-1.
- **Clock Speed:** Internal clock speeds exceeding 450MHz.
- **Analog-to-Digital Converter:** On-chip XADC.
- **Programming:** Programmable over JTAG and Quad-SPI Flash.
- **Memory:** 256MB DDR3L with a 16-bit bus @ 667MHz, 16MB Quad-SPI Flash.
- **Connectivity:** 10/100 Mbps Ethernet, USB-UART Bridge.
- **Power:** Powered from USB or any 7V-15V source.
- **User Interfaces:** 4 Switches, 4 Buttons, 1 Reset Button, 4 LEDs, 4 RGB LEDs.
- **Expansion:** 4 Pmod connectors, shield connector.

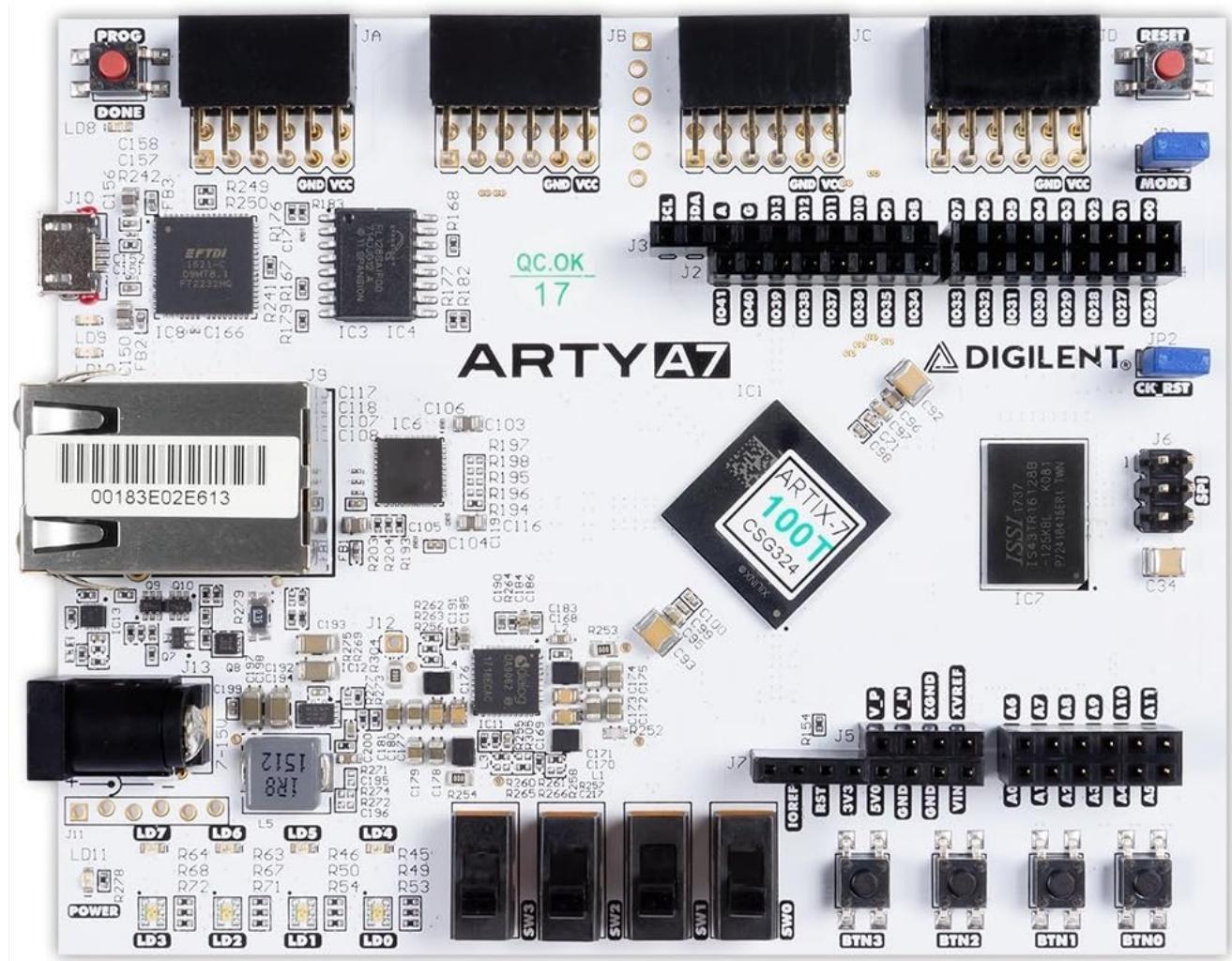


Figure 2: Top-down view of the Arty A7-100T board, highlighting the Artix-7 FPGA, Ethernet port, and various user I/O components.

3. SETUP GUIDE

Follow these steps to set up your Arty A7-100T development board:

1. Power Connection:

The Arty A7-100T can be powered via the USB port or an external 7V-15V DC power supply connected to the barrel jack. For initial setup and programming, connecting via USB is typically sufficient.

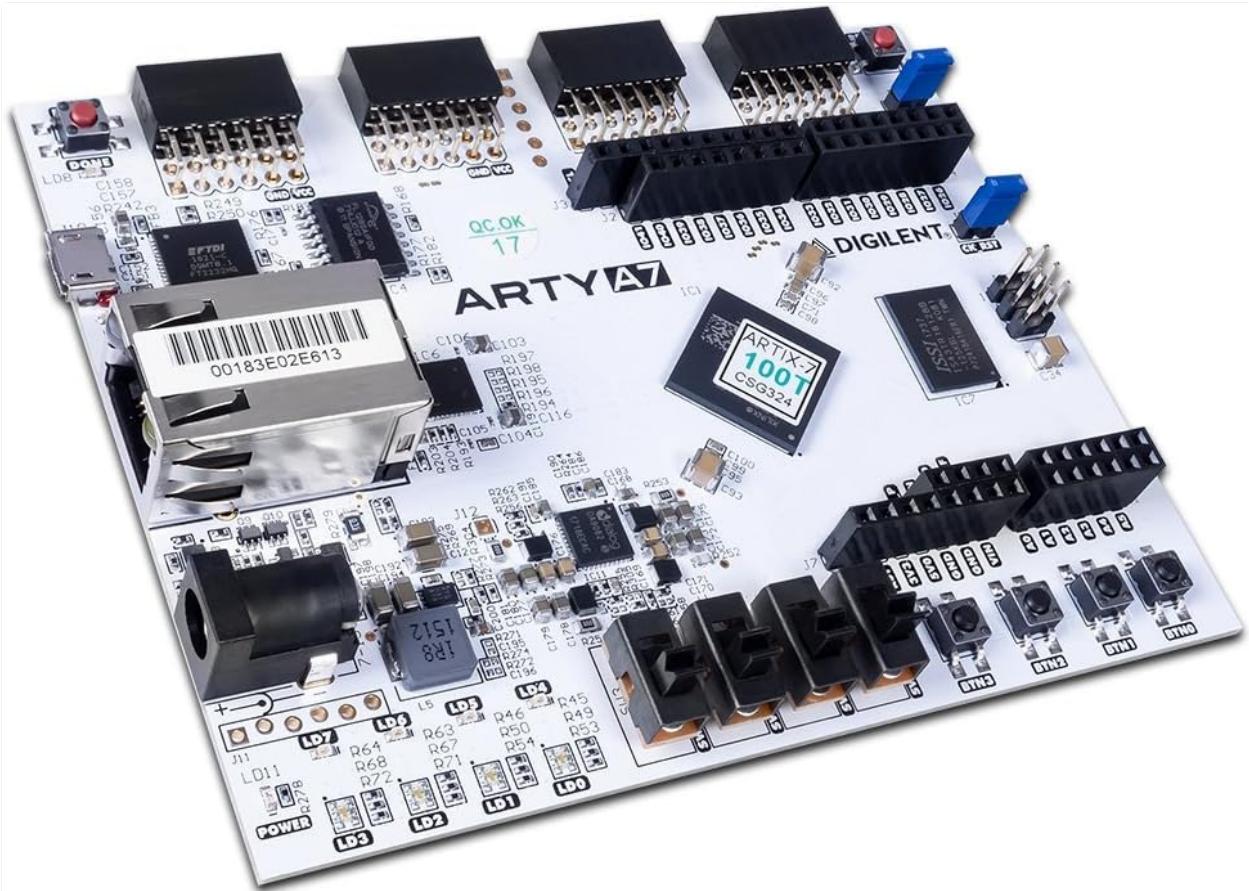


Figure 3: Angled view of the Arty A7-100T, showing the USB port and DC barrel jack for power input.

2. USB Connection:

Connect the Arty A7-100T to your computer using a USB cable. This connection provides power, enables USB-JTAG programming, and facilitates communication via the USB-UART bridge.

3. Software Installation:

Install the Xilinx Vivado Design Suite (WebPack edition is suitable for this board) on your computer. This software is required for developing, synthesizing, and programming your FPGA designs. Refer to the official Xilinx documentation for detailed installation instructions.

4. Driver Installation:

Ensure that the necessary USB drivers for the Digilent board are installed. These are typically included with the Vivado installation or can be downloaded from the Digilent website.

4. OPERATING INSTRUCTIONS

Operating the Arty A7-100T involves creating and deploying FPGA designs. Here's a general workflow:

1. Project Creation:

Start a new project in Xilinx Vivado. Select the correct FPGA part: **XC7A100TCSG324-1** (or **XC7A35TICSG324-1L** if you have the 35T variant).

2. Design Entry:

Write your hardware description language (HDL) code (VHDL or Verilog) for your desired functionality. This could involve implementing custom logic, a soft-core processor like MicroBlaze, or interfacing with peripherals.

3. Constraint Files (XDC):

Add Xilinx Design Constraint (XDC) files to map your design's I/O ports to the physical pins on the Arty A7-100T board. Digilent provides master XDC files for the Arty A7 on their website, which serve as a good starting point.

4. Synthesis and Implementation:

Run synthesis and implementation in Vivado. This process translates your HDL code into a netlist, maps it to the FPGA's resources, and generates the bitstream file.

5. Bitstream Generation:

After successful implementation, generate the bitstream (.bit) file. This file contains the configuration data for the FPGA.

6. Programming the FPGA:

Use the Vivado Hardware Manager to connect to your Arty A7-100T board via the USB-JTAG interface.

Program the FPGA with your generated bitstream. You can also program the Quad-SPI Flash for persistent storage of your design.

7. Testing and Debugging:

Test your design using the onboard switches, buttons, and LEDs, or by connecting external Pmod modules.

Utilize Vivado's debugging tools, such as the Integrated Logic Analyzer (ILA), for verifying internal signals.

5. MAINTENANCE

Proper care and maintenance will ensure the longevity and reliable operation of your Arty A7-100T board:

- **Handling:** Always handle the board by its edges to avoid touching sensitive components.
- **Static Discharge:** Take precautions against electrostatic discharge (ESD) when handling the board. Use an anti-static wrist strap and work on an ESD-safe surface.
- **Cleaning:** Keep the board clean and free from dust and debris. Use compressed air or a soft brush for cleaning. Avoid using liquids directly on the board.
- **Storage:** Store the board in an anti-static bag when not in use, in a dry environment away from extreme temperatures.
- **Power Supply:** Use only recommended power supplies (USB or 7V-15V DC). Incorrect voltage can damage the board.

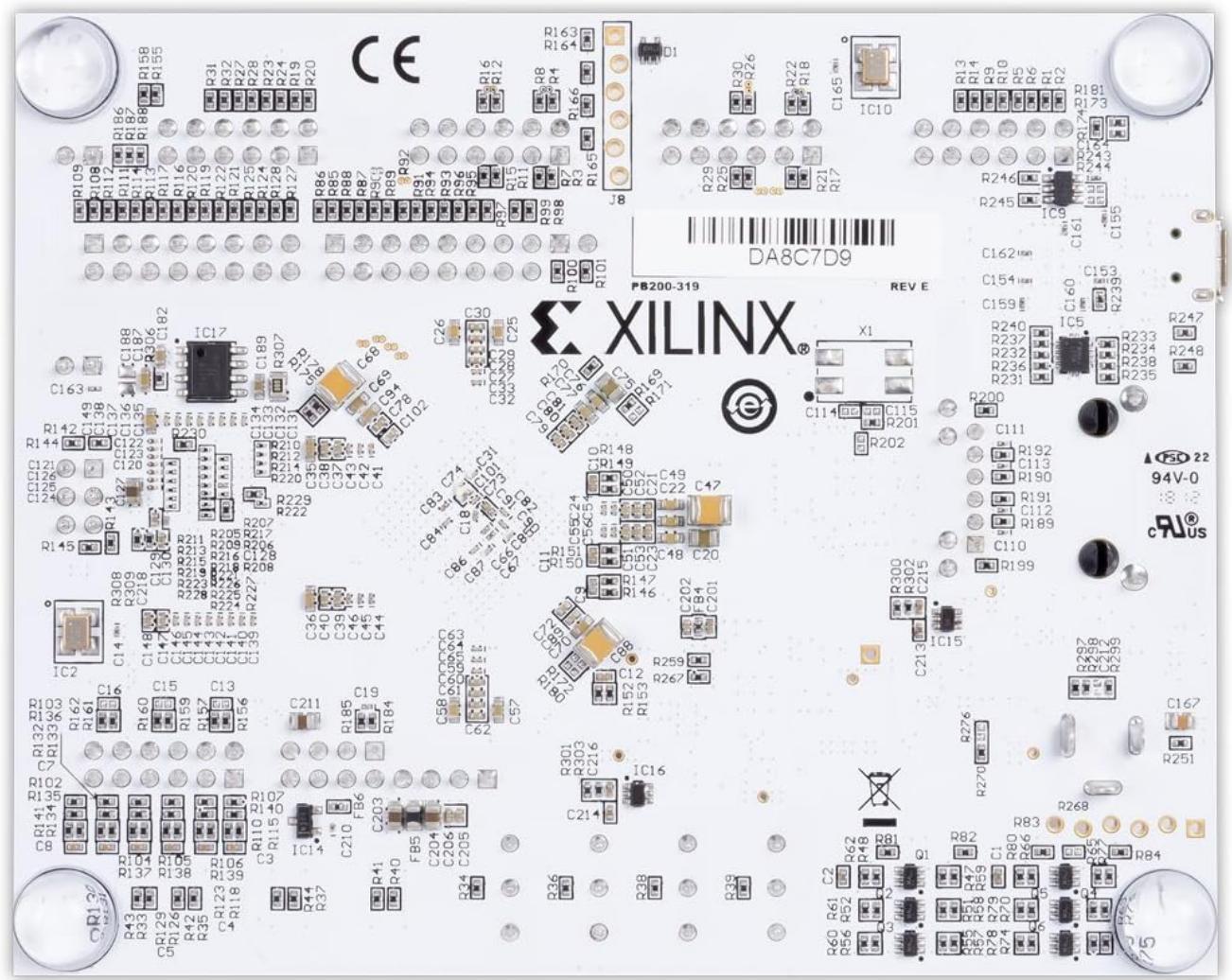


Figure 4: Bottom view of the Arty A7-100T board, showing solder points and regulatory markings.

6. TROUBLESHOOTING

If you encounter issues with your Arty A7-100T, consider the following troubleshooting steps:

- **Power Indicator:** Check if the power LED (LD1) is illuminated when the board is connected to power. If not, verify your power source and connections.
- **USB Connection Issues:** If your computer does not recognize the board, ensure USB drivers are correctly installed. Try a different USB port or cable.
- **Programming Errors:**
 - Verify that the correct FPGA part (XC7A100TCSG324-1) is selected in your Vivado project.
 - Ensure the JTAG chain is correctly detected in Vivado Hardware Manager.
 - Check for any error messages in the Vivado console.
- **Design Functionality:**
 - Double-check your HDL code for syntax or logical errors.
 - Review your XDC constraints to ensure correct pin assignments.
 - Use Vivado's simulation tools to verify your design logic before programming the FPGA.
 - Utilize the Integrated Logic Analyzer (ILA) for on-chip debugging of your running design.
- **External Peripherals:** If using Pmod connectors, ensure they are correctly connected and compatible with the Arty A7's voltage levels and pin assignments.

7. SPECIFICATIONS

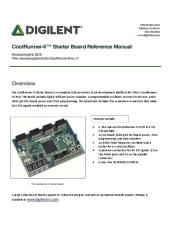
FPGA Model	Xilinx Artix-7 XC7A100TCSG324-1
RAM Memory Installed Size	256 MB DDR3L
Flash Memory	16 MB Quad-SPI Flash
CPU Speed (Internal Clock)	Exceeding 450 MHz
Ethernet	10/100 Mbps
Power Input	USB or 7V-15V DC
Package Dimensions	4.41 x 3.54 x 1.26 inches
Item Weight	11.3 ounces
Model Number	410-319
Manufacturer	Digilent

8. WARRANTY AND SUPPORT

The Digilent Arty A7-100T is manufactured by Digilent. For detailed warranty information, technical support, and additional resources such as schematics, reference manuals, and example projects, please visit the official Digilent website.

[Visit Digilent's Official Website](#)

Related Documents - Arty A7-100T

	<p>Digilent CoolRunner-II Starter Board Reference Manual</p> <p>A comprehensive reference manual for the Digilent CoolRunner-II Starter Board, a USB-powered development platform featuring a Xilinx CoolRunner-II CPLD, power supplies, oscillator, I/O devices, and expansion connectors.</p>
	<p>Digilent FX12 Board Errata and Modifications</p> <p>Official errata document from Digilent detailing modifications made to the FX12 development board, specifically addressing JTAG signal routing issues on Rev B boards.</p>

	<p>Digilent Pmod 8LD Reference Manual - High-Brightness LED Module</p> <p>Detailed reference manual for the Digilent Pmod 8LD, a compact module featuring eight high-brightness green LEDs controlled via GPIO pins and BJTs for low-power logic-level operation.</p>
	<p>Digilent PmodIOXP Input/Output Expansion Module Reference Manual</p> <p>This reference manual details the Digilent PmodIOXP, an Input/Output expansion module designed to provide up to 19 additional I/O pins. It highlights features such as I²C communication, a 16-element FIFO, built-in keypad decoding, and PWM generation, along with functional descriptions, interfacing details, pinout, and physical dimensions.</p>
	<p>Digilent PmodDHB1 Dual H-Bridge Motor Driver Reference Manual</p> <p>Reference manual for the Digilent PmodDHB1, a dual H-bridge motor driver capable of controlling two DC motors or a bipolar stepper motor, featuring over-current protection and quadrature encoder feedback.</p>
	<p>Digilent PmodRS485 Reference Manual</p> <p>This reference manual provides detailed information on the Digilent PmodRS485, a high-speed RS-485 communication module offering signal and power isolation for robust data transfer in noisy environments. It covers features, functional description, interfacing, pinouts, and physical dimensions.</p>

Documents - Digilent – Arty A7-100T

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Arty A7-100T™ Statement of Volatility
Revised April 27, 2023 Author: AB
This document lists the location, purpose, capacity, volatility, and reprogrammability of memory devices that may be included in the Arty A7-100T. The Arty A7-100T is a high-performance, high-density, and low-power FPGA. It is a device that is not intended for use in medical, safety, or other applications where failure of the device could result in personal injury or death. The Arty A7-100T is a device that is not intended for use in medical, safety, or other applications where failure of the device could result in personal injury or death. The Arty A7-100T is a device that is not intended for use in medical, safety, or other applications where failure of the device could result in personal injury or death. The Arty A7-100T is a device that is not intended for use in medical, safety, or other applications where failure of the device could result in personal injury or death.

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Volatile Memory

	Memory Region	User programmable	User removable	SRAM	Flash	Reset procedure
XC7A200T-2SGG324	DS91 Program/ User memory	Yes	No	256b	Retain power for 10 seconds	
XC7A200T-2SGG324	Configurable SRAM for interconnect	Yes	No	32,400,480 bits	Retain power for 10 seconds	
XC7A200T-2SGG324	Block RAM	Yes	No	4,096 bits	Retain power for 10 seconds	
XC7A200T-2SGG324	Configurable RAM	Yes	No	1,389,110 bits	Retain power for 10 seconds	

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Arty A7-100TTM Statement of Volatility Revised April 27, 2023 Author: AB
 This document applies to the Arty A7 rev. E.X 1300 Henley Court Pullman, WA 99163
 509.334.6306 www.digilent.com This document lists the location, purpose, capacity, volatility and re programmability of memory devices that ma...
 lang:en score:43 filesize: 160.44 K page_count: 2 document date: 2023-04-27

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Running a RISC-V Processor on the Arty A7
The Arty A7-100T contains a Xilinx XC7A100T FPGA which is the largest FPGA available for the Arty A7 and is ideal for deployment of softcore processors. These processors can be either proprietary or open source. One of the most popular open source processors is the RISC-V. This tutorial covers building a RISC-V processor, specifically the SiFive Freedom E310. This guide steps through the process of loading the Freedom E310 onto an Arty A7, and programming it using the Arduino IDE.

This tutorial covers building a RISC-V processor, specifically the SiFive Freedom E310 and steps through the process of loading the Freedom E310 onto an Arty A7, and programming it using the Arduino IDE.

- Getting Started
- Building the RISC-V
- Programming the Hardware
- Generating Software

What do you need for this project?

- Arty A7-100T
- Ubuntu 18.04 LTS 64bit
- SiFive RISC-V USB Programmer
- Ubuntu 20.04 LTS - Wikipedia Edition
- Arduino Dev Segment Environment
- SiFive RISC-V USB Programmer and the programmer and use of the Arty's Pmod connectors, which is connected to the JTAG Test Access Port of the processor.
- A Linux development or virtual machine is needed to compile the processor, generate the firmware and update metadata to the processor.

With the following tutorial at https://reference.digilentinc.com/reference/programmable_hardware/arty_a7_100t_risc_v/ to create the RISC-V based application

www.digilentinc.com

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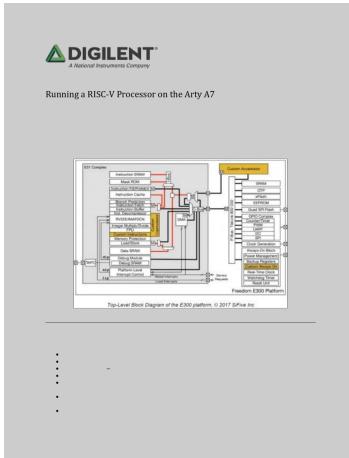
From a Custom 2 Series Core to Hello World in 30 Minutes

Drew Barbier - Sr. Product Marketing Manager Amy Lindburg - Director Product Management May, 2019

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Minutes From a Custom 2 Series Core to Hello World in 30 Manual functional description of the deliverable User Guide detailed including information on integration and testbench Arty FPGA describes how use info Metadata about design device tree retiming SiFive Insight tests sifive cdn prismic io 79079c42 21c9 4829 a7f9 eaa565673bf3

From a Custom 2 Series Core to Hello World in 30 Minutes Drew Barbier - Sr. Product Marketing Manager Amy Lindburg - Director Product Management May, 2019 About This Presentation This presentation will introduce SiFive Core Designer, our RISC-V Core IP deliverables, and software development method...
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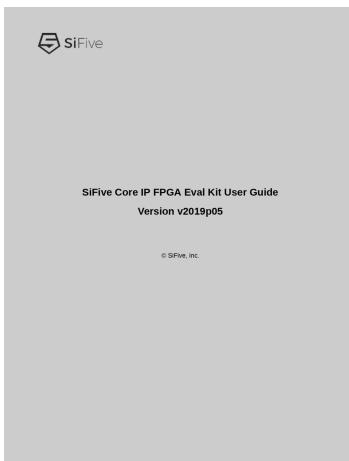


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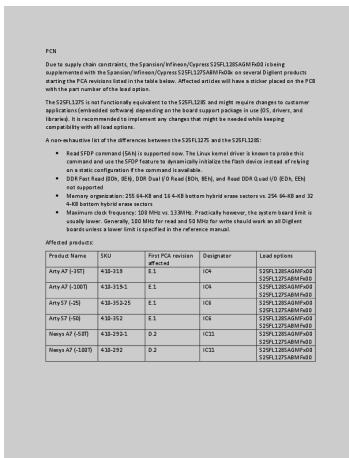


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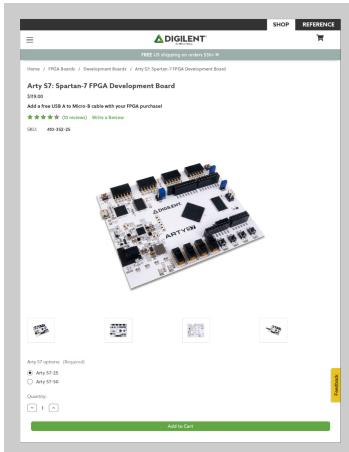
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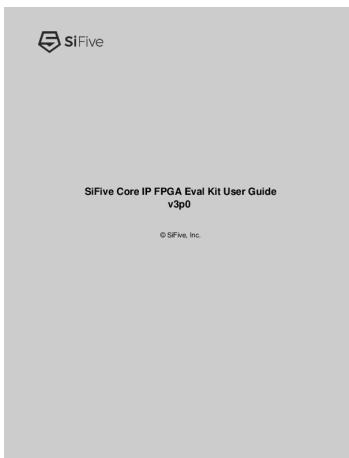
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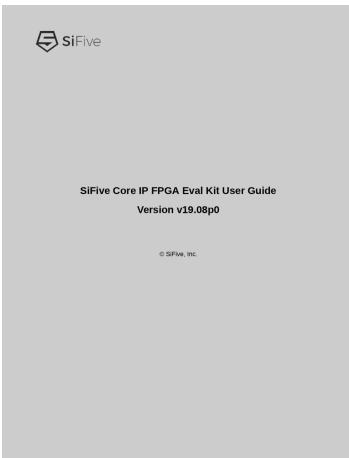


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