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APEX WAVES PXIe-5842 PXI Vector Signal Transceiver User Guide

Contents

APEX WAVES PXIe-5842 PXI Vector Signal Transceiver

Product Information

- Product Name: PXIe-5842
- Manufacturer: NI
- Board Assembly Part Numbers: 135077B-01L or later
- Volatile Memory:
  - Device Operation (x2): DRAM
  - Processor RAM Type: DRAM
  - FPGA SRAM: 2 MB Lattice LCMXO3LF9400 (x2), 2 MB Lattice
  - LCMXO3D4300 (x2)
  - FPGA / Processor DRAM Size: 1 GB Xilinx XCZU47DR
  - Battery Backup: No
  - User1 Accessible: Yes
  - System Accessible: Yes
- Non-Volatile Memory (incl. Media Storage):
  - Target Data: Flash EEPROM
  - Flash Size: 256 MB
  - Device configuration, Device information, FPGA bitstream
  - Calibration Storage, Calibration metadata, Calibration data, Boot
  - Flash (x2), Device Settings, Power Up Configuration
  - Battery Backup: No
  - User Accessible: No
  - System Accessible: Yes

Product Usage Instructions

1. To clear the calibration password in the Calibration Storage
   Flash, follow these steps:

   - Open an NI-RFSG session using the niRFSG Initialize VI.
   - To clear/reset the calibration password
   - Add the niRFSG Change External Calibration Password VI after the niRFSG Initialize VI
   - Specify the current password in the password input of the RFS Change External Calibration Password VI

- Wire an empty string (blank password) to the new password input of the niRFSG Change External Calibration Password VI.
- Close the NI-RFSG session using the niRFSG Close VI.

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Contact: 866-275-6964 | **support@ni.com**

Manufacturer: NI
Board Assembly Part Numbers (Refer to Procedure 1 for identification procedure)

Part Number and Revision	Description
135077B-01L or later	**PXIe-5842**

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Volatile Memory

Volatile Memory						
Target Data	Type	Size	Battery Backup	User[1] Accessible	System Accessible	Sanitization Procedure
Waveform storage – Bank 1	DRAM	5 GB	No	Yes	Yes	Cycle Power
Waveform storage – Bank 2	DRAM	5 GB	No	Yes	Yes	Cycle Power
FPGA Image Memory	DRAM	64 MB	No	Yes	Yes	Cycle Power
Device Operation	FPGA	Xilinx XCKU085	No	Yes	Yes	Cycle Power
Device Operation	FPGA	Microchip M2GL025	No	No	Yes	Cycle Power
Storage	SRAM	2 MB	No	Yes	Yes	Cycle Power
Device Operation (x2)	FPGA	Lattice LCMXO3LF- 9400 (x2)	No	No	Yes	Cycle Power
Device Operation (x2)	FPGA	Lattice LCMXO3D- 4300 (x2)	No	No	Yes	Cycle Power
Device Operation	FPGA / Processor	Xilinx XCZU47 DR	No	Yes	Yes	Cycle Power
Processor RAM	DRAM	1 GB	No	No	Yes	Cycle Power

Non-Volatile Memory (incl. Media Storage)

Target Data	Type	Size	Battery Backup	User Accessible	System Accessible	Sanitization Procedure
Device configuration · Device information	Flash	256 MB	No	No	Yes	None
· FPGA bitstream				No	Yes	None
Calibration Storage · Calibration metadata	Flash	4 GB	No	Yes	Yes	Procedure 2
· Calibration data[2]				No	Yes	None
Boot Flash (x2)	Flash	64 MB (x2)	No	No	Yes	None
Device Settings	EEPROM	32 KB	No	No	Yes	None
Power Up Configuration	FPGA	Microchip M2GL025	No	No	Yes	None

| Power Up Configuration (x2) | FPGA | Lattice LCMXO3 LF- 9400 (x2) | No | No | Yes | None |
| Power Up Configuration (x2) | FPGA | Lattice LCMXO3 D- | No | No | Yes | None |

1. Refer to the Terms and Definitions section for clarification of User and System Accessible
2. Calibration constants that are stored on the device include information for the device's full operating range. Any implications resulting from partial self-calibration can be eliminated by running the full self-calibration procedure.

Notice: This document is subject to change without notice

Procedures

Procedure 1 – Board Assembly Part Number Identification
To determine the Board Assembly Part Number and Revision, refer to the label applied to the surface of your product. The Assembly Part Number should be formatted as "P/N: 135077#-01L" where "#" is the letter revision of the assembly (e.g. A, B, C…).

Procedure 2 – Calibration Storage Flash (Calibration Metadata)
Requirements: LabVIEW version 2019 or later and NI-RFSG version 2022 Q4 or later that supports this model. The user-accessible portion of the Calibration Storage Flash is limited to a programmable calibration password, which can be programmed through the NI-RFSG driver in the LabVIEW application. To clear the calibration password, complete the following steps in an empty LabVIEW VI and then run the VI:

1. Open an NI-RFSG session using the niRFSG Initialize VI.
2. To clear/reset the calibration password:
    - Add the niRFSG Change External Calibration Password VI after the niRFSG Initialize VI.
    - Specify the current password in the "password" input of the niRFSG Change External Calibration Password VI.
    - Wire an empty string (blank password) to the "new password" input of the niRFSG Change External Calibration Password VI.
3. Close the NI-RFSG session using the niRFSG Close VI.

Terms and Definitions

Cycle Power:
The process of completely removing power from the device and its components and allowing for adequate discharge. This process includes a complete shutdown of the PC and/or chassis containing the device; a reboot is not sufficient for the completion of this process.

Volatile Memory:
Requires power to maintain the stored information. When power is removed from this memory, its contents are lost. This type of memory typically contains application-specific data such as capture waveforms.

Non-Volatile Memory:
Power is not required to maintain the stored information. The device retains its contents when power is removed. This type of memory typically contains the information necessary to boot, configure, or calibrate the product or may include device power-up states.

User Accessible:
The component is read and/or write addressable such that a user can store arbitrary information to the component from the host using a publicly distributed NI tool, such as a Driver API, the System Configuration API, or MAX.

System Accessible:
The component is read and/or written addressable from the host without the need to physically alter the product.

Clearing:
Per NIST Special Publication 800-88 Revision 1, "clearing" is a logical technique to sanitize data in all User Accessible storage locations for protection against simple non-invasive data recovery techniques using the same interface available to the user; typically applied through the standard read and write commands to the storage device.

Sanitization

Per NIST Special Publication 800-88 Revision 1, "sanitization" is a process to render access to "Target Data" on the media infeasible for a given level of effort. In this document, clearing is the degree of sanitization described.

Documents / Resources

APEX WAVES PXIe-5842 PXI Vector Signal Transceiver [pdf] User Guide
PXIe-5842 PXI Vector Signal Transceiver, PXIe-5842, PXI Vector Signal Transceiver, Vector Signal Transceiver, Signal Transceiver, Transceiver

References

- [**Product Documentation - NI**](#)
- [**PXIe-5842 PXI Vector Signal Transceiver | Apex Waves**](#)