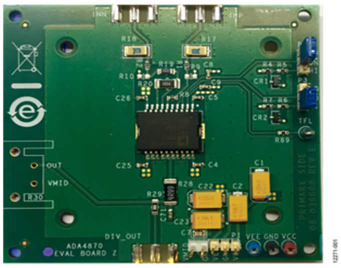

ANALOG DEVICES UG-685 Evaluating the ADA4870 High Speed High Output Current Amplifier User Guide

ADA4870ARR-EBZ User Guide
UG-685

Contents

1 UG-685 Evaluating the ADA4870 High-Speed High Output Current Amplifier
2 FEATURES
3 APPLICATIONS
4 GENERAL DESCRIPTION
5 REVISION HISTORY
6 EVALUATION BOARD HARDWARE
7 ASYMMETRICAL SUPPLIES AND MID-SUPPLY BIAS (VMID)
8 THERMAL PERFORMANCE
9 EVALUATION BOARD SCHEMATIC
10 BILL OF MATERIALS
11 Legal Terms and Conditions
12 Documents / Resources
  12.1 References
13 Related Posts

UG-685 Evaluating the ADA4870 High-Speed High Output Current Amplifier

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Evaluating the ADA4870 High Speed, High Output Current Amplifier

FEATURES

Enables easy evaluation of the ADA4870 Single-supply or dual-supply operation Robust thermal management

APPLICATIONS

Organic light-emitting diode (OLED) panel driver Active matrix organic light-emitting diode (AMOLED) panel driver Base transceiver station (BTS) envelope tracking Power field effect transistor (FET) driver Ultrasound Piezoelectric driver PIN diode driver Waveform generation Automatic test equipment (ATE) Charge-coupled device (CCD) panel driver

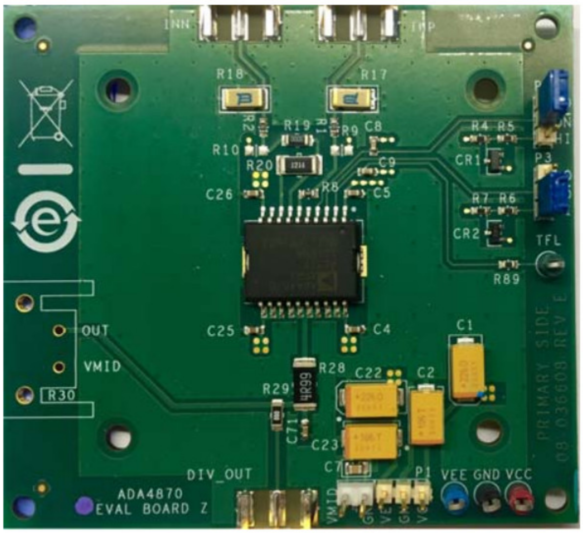


Figure 1. Evaluation Board, Top Side

GENERAL DESCRIPTION

The ADA4870 is a 40 V, unity-gain stable, high-speed current feedback amplifier capable of delivering 1 A of output current from a 40 V supply. Manufactured using Analog Devices, Inc., a proprietary high voltage XFCB process, the innovative architecture of the ADA4870 enables high output power, and high-speed signal processing solutions in a variety of demanding applications.

The ADA4870 is ideal for driving high-voltage power FETs, piezoelectric transducers, PIN diodes, and a variety of other demanding applications that require high speed from the high supply voltage and high current output.

The ADA4870 is available in a power SOIC package (PSOP_3) featuring an exposed thermal slug that provides high thermal conductivity to the printed circuit board (PCB) and heat sink enabling efficient heat transfer for improved reliability in demanding environments. The ADA4870 operates over the industrial temperature range of −40°C to +85°C.

The ADA4870ARR-EBZ evaluation board provides a platform for quick and easy evaluation of the ADA4870. Figure 1 shows the top side of the evaluation board. Figure 2 shows the bottom side of the board with the large exposed copper area for applying a heat sink as needed.

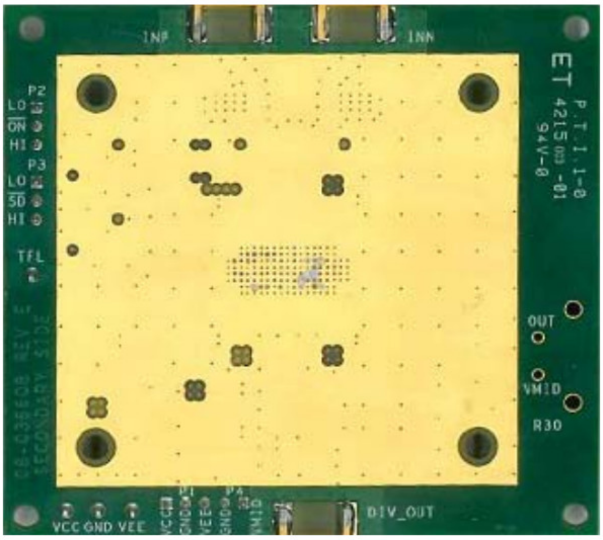


Figure 2. Evaluation Board, Bottom Side

PLEASE SEE THE LAST PAGE FOR AN IMPORTANT WARNING AND LEGAL TERMS AND CONDITIONS.

REVISION HISTORY

6/2016—Rev. 0 to Rev. A

Changes to Applications Section, Figure 1, and Figure 2 1
Changes to Board Stack Up Section, Power Supplies and Decoupling Section, and Input and Output Section 3
Added Symmetrical Supplies and DC-Coupled Inputs Section and Figure 3; Renumbered Sequentially 3
Added Asymmetrical Supplies and Mid Supply Bias (VMID) Section, Figure 4, and Figure 5 4
Changes to Table 1 4
Changes to ON, Initial Power-Up, Short Circuit Section, Shutdown (SD) Section, and Thermal Design and Heat Sink Section 5
Added Figure 6 5
Added Figure 7 6
Changes to Thermal Performance Section, Figure 8, and Figure 9 6
Changes to Figure 10.. 7
Changes to Table 2 8

6/2014—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

BOARD STACK-UP

The ADA4870ARR-EBZ evaluation board is a 6-layer board. All signal routing is on the top layer; the bottom layer is an exposed copper ground plane to facilitate the use of a heat sink. The heat sink is needed for high-power dissipation projects, such as driving a 20 Ω load with the maximum output swing. The internal layers (Layer 2 through Layer 5) consist of the GND, VCC, VMID, and VEE planes.

POWER SUPPLIES AND DECOUPLING

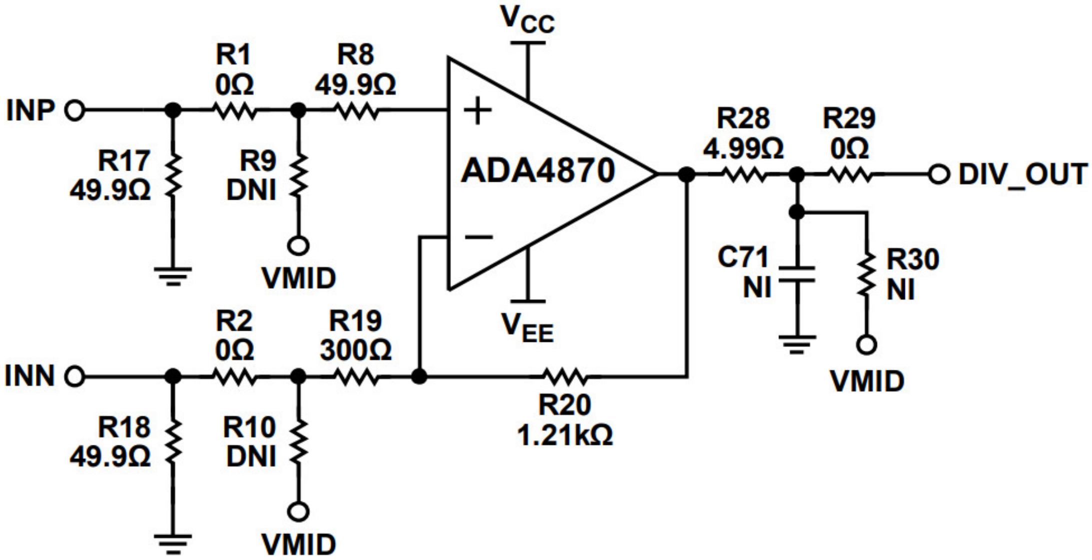
The evaluation board can be powered using a single supply or dual supply. The total supply voltage (VCC − VEE) must be between 10 V and 40 V. The board provides sufficient power supply decoupling for high current, fast slewing signals with 22 μF and 10 μF tantalum capacitors installed at C1 and C2 where the VCC supply voltage is applied to the board; 22 μF and 10 μF tantalum capacitors are installed at C22 and C23 where the VEE supply voltage is applied to the board. In addition, 0.1 μF ceramic chip capacitors (C4 and C5) are placed in close proximity to the VCC pins (Pin 1, Pin 18, Pin 19, and Pin 20). And 0.1 μF ceramic chip capacitors (C25 and C26) are placed in close proximity to the VEE pins (Pin 10, Pin 11, Pin 12, and Pin 13).

INPUT AND OUTPUT

Figure 10 shows the evaluation board schematic for the factory default settings when the board is shipped. The evaluation board uses edge-mount SMA connectors on the inputs and outputs for easy interfacing to signal sources and test equipment. When evaluating high voltage output signals using standard 50 Ω test equipment, R29 can be replaced with a 2.45 kΩ resistor that provides a signal division of 49.6 at the DIV_OUT SMA connector. The board can accommodate a capacitor load (C71) referenced to GND, and/or a power resistor in the TO-220 package (R30) referenced to VMID. When using input signals of 5 V and lower, the board is equipped with 49.9 Ω, 0.25 W resistors at R17 and R18 that are capable of handling the power when using the factory default settings. The factory default configuration provides for operation on dual symmetrical supplies in noninverting and inverting gains of +4.5 V/V, and −4.0 V/V respectively. For single-supply and asymmetrical supply operation, see the Asymmetrical Supplies and Mid Supply Bias (VMID) section and Table 1 for guidance on configuring the input terminations and supply settings.

SYMMETRICAL SUPPLIES AND DC-COUPLED INPUTS

Figure 3 shows the noninverting or inverting configuration schematic when using dual, symmetrical supplies. When using the factory default settings with noninverting input, the ground reference is established through the 49.9 Ω termination resistors (R17 and R18), and the gain can be calculated using R20/(R19 + R18). The gain is +4.5 V/V for the factory default settings. When using the factory default settings with inverting input, the gain can be calculated using R20/R19. The gain is −4.0 V/V for the factory default settings. In dual-supply operation when installing R30 in either inverting or noninverting applications, position the jumper at P4 to short VMID to GND.



NOTES

1. DNI = DO NOT INSTALL.
2. NI = NOT INSTALLED (USER-DEFINED VALUES).

Figure 3. Schematic of Dual, Symmetrical Supplies with Noninverting or Inverting Input

ASYMMETRICAL SUPPLIES AND MID-SUPPLY BIAS (VMID)

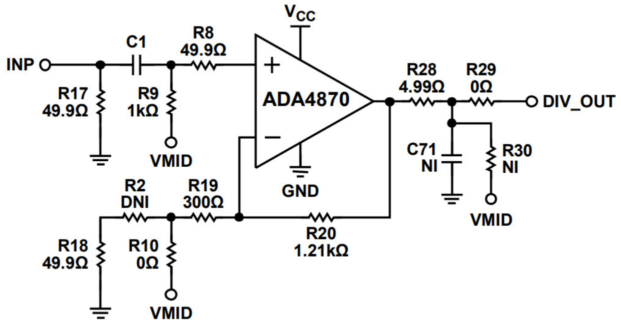
Figure 4 and Figure 5 show schematics when using a single supply with ac-coupled input.

The ADA4870 must be referenced to a dc operating point. When using a single supply or asymmetrical dual supplies, apply the appropriate reference voltage to the VMID pin of P4 using a low-impedance source, such as a dc supply. The recommended VMID reference voltage is VEE + (VCC – VEE)/2.

When a coupling into the noninverting input (INP), the dc operating point of the amplifier can be established by installing a resistor at R9 connected to VMID and replacing R1 with an ac coupling capacitor (C1), as shown in Figure 4. The ac coupling capacitor (C1) combined with the VMID bias resistor (R9) form a high-pass filter with the cutoff frequency at 1/(2 × π × R9 × C1).

The value of the ac coupling capacitor (C1) can be calculated based on the desired cutoff frequency.

When coupling into the inverting input (INN), the dc operating point of the amplifier can be established by shorting R9 to VMID. Do not install R1.



NOTES
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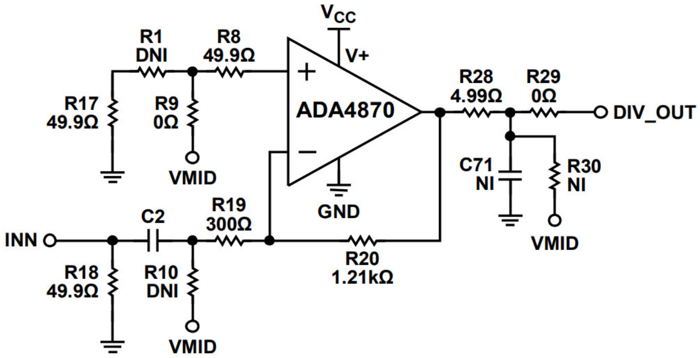
2. NI = NOT INSTALLED (USER-DEFINED VALUES).

Figure 4. Schematic of Single Supply with Noninverting Input



NOTES
1. DNI = DO NOT INSTALL.
2. NI = NOT INSTALLED (USER-DEFINED VALUES).

Figure 5. Schematic of Single Supply with Inverting Input

Table 1. Configuration of Input Components

Supply[1]	**Configuration**	**Coupling**	**Gain (V/V)**	**R9 (Ω)**	**R10 (Ω)**	**R1 (Ω)**	**R2 (Ω)**	**P4 (VMID)**
Dual	Noninverting	DC	+4.5	Do not insert	Do not insert	0	0	Open[2]
Dual	Inverting	DC	–4.0	Do not insert	Do not insert	0	0	Open[2]
Single	Noninverting	AC	+5.0	1,000	0	Capacitor[3]	Do not insert	DC voltage supply
Single	Inverting	AC	–4.0	0	Do not insert	Do not insert	Capacitor[3]	DC voltage supply

1. Dual means symmetrical supplies; single means any nonsymmetrical supplies.
2. If R30 is installed, short VMID to GND.
3. When input ac coupling is required, replace the dc coupling resister with an ac coupling capacitor.

ON, INITIAL POWER-UP, AND SHORT CIRCUIT

The board is shipped with the ON pin pulled low to VEE at P1 to ensure that the amplifier is enabled. Subsequently, floating the ON pin enables the short-circuit protection feature while the amplifier remains on. While ON is held low, the short-circuit protection feature is disabled.

The ON pin turns on the amplifier after the initial power-up and after a short-circuit event. The pin is referenced to the negative supply (VEE).

When a short-circuit condition is detected, the amplifier is disabled, the supply current drops to approximately 5 mA, and the TFL pin outputs a dc voltage of approximately 300 mV above VEE. To turn the amplifier back on after a short-circuit event, follow the previously described sequence for initial power-up.

Pulling the ON pin high disables the amplifier and causes the supply current to drop to approximately 5 mA as if a short circuit condition had been detected. Pin 3 of P2 uses a 5 V Zener diode (CR1) to set the high level at 5 V above VEE.

The impedance at ON is approximately 20 kΩ. The ON pin is decoupled to VEE via C8 to shunt noise away from ON and to help avoid false triggers.

SHUTDOWN (SD)

The board factory default setting for the (P3) jumper pulls the SD pin to the HI position, VEE + 5.2 V. Pulling the SD pin low to VEE places the amplifier in a low power shutdown state, reducing the quiescent current to approximately 750 µA. The SD pin must be pulled low to a maximum of VEE + 0.9 V for shutdown or pulled high to a minimum of VEE + 1.1 V to enable the amplifier. Do not float the pin. When turning the amplifier back on from the shutdown state, pull the SD pin high and then pull the ON pin low. Following this sequence is required to turn on the ADA4870. To enable short-circuit protection, the ON pin must float following the turn-on sequence.

THERMAL MONITOR/SHORT-CIRCUIT FLAG (TFL)

The TFL pin can be used to monitor relative changes in die temperature and to detect a short-circuit condition. During normal operation, the TFL pin outputs a dc voltage that is approximately 1.7 V (typical) above VEE and is related to the die temperature. The TFL voltage changes at approximately –3 mV/°C. When the die temperature exceeds approximately 140°C, the amplifier switches to an off state, dropping the supply current to approximately 5 mA while TFL continues to report a voltage indicative of the die temperature. When the die temperature returns to an acceptable level, the amplifier automatically resumes normal operation.

THERMAL DESIGN AND HEAT SINK SELECTION

In some applications, the ADA4870 may be required to dissipate as much as 10 W at elevated ambient temperatures of up to +85°C. The evaluation board provides robust thermal management under these conditions. The top of the board has an exposed copper area to which the ADA4870 PSOP package must be soldered. The exposed copper area allocated to the attachment of the PSOP slug is connected to the exposed copper ground plane on the bottom by an array of 136 thermal vias. A single internal ground layer (Layer 2) is also attached. Figure 6 shows a model of the ADA4870 package mounted to the evaluation board with an applied heat sink.

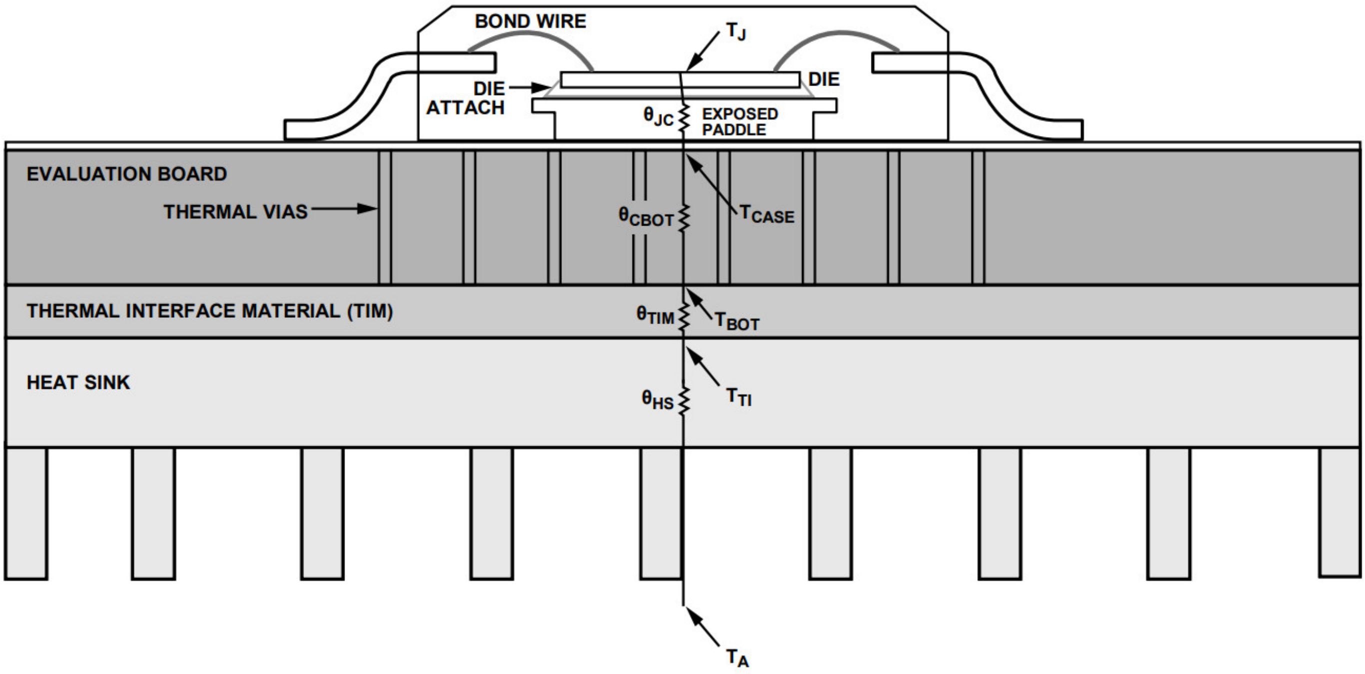


Figure 6. Thermal Model for ADA4870 with Heat Sink

UG-685

When necessary, a heat sink can be mounted to the bottom exposed copper using the mounting holes and an applied thermal interface material (TIM), such as the GC Electronics 10-8109. Refer to the manufacturer guidelines when applying the TIM; the TIM thermal resistance (θTIM) must be no more than 0.3°C/W. See Figure 7 for the dimensions of the heat sink and mounting hole locations. The approximate thermal resistance of the heat sink can be calculated from Equation 1, where θJC equals 1.1°C/W and θCBOT is approximately equal to 1.0°C/W. A heat sink having a thermal resistance of 4.2°C/W allows 10 W of power dissipation at an ambient temperature of 85°C.

$$\theta_{HS} = \left(\frac{T_J - T_A}{P_{DISS}}\right) - (\theta_{JC} + \theta_{CBOT} + \theta_{TIM}) \qquad (1)$$

where:

TJ is the junction temperature.

TA is the ambient temperature.

PDISS is the chip power dissipation.

θJC is the chip's thermal resistance.
θCBOT is the thermal resistance of the chip solder material and the PCB.
θTIM is the TIM thermal resistance.

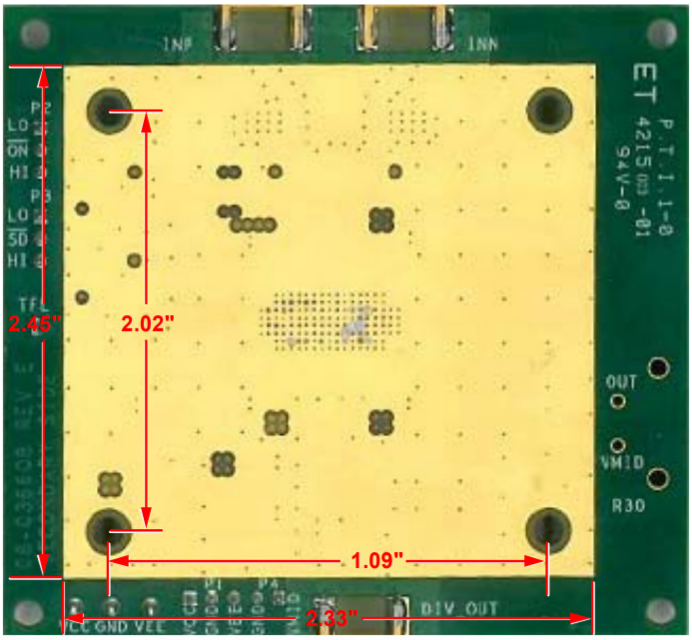


Figure 7. Dimensions of the Heat Sink and Mounting Holes

THERMAL PERFORMANCE

Figure 8 and Figure 9 show the die temperature vs. time while the internal power dissipation is increased over several hours. The ambient environment for Figure 8 is 25°C in still air; for Figure 9, the ambient environment is 85°C in still air. Figure 8 shows the die temperature in two conditions: one without a heat sink and the other with a heat sink rated at 5.4°C/W. Figure 9 shows the die temperature in three conditions: one without a heat sink, the second with a heat sink rated at 5.4°C/W, and the third with a heat sink rated at 4.2 °C/W. For both Figure 8 and Figure 9, the board is positioned with the bottom side or heat sink facing up to facilitate natural convection. Using ac power dissipation and/or forced convection results in lower temperatures.

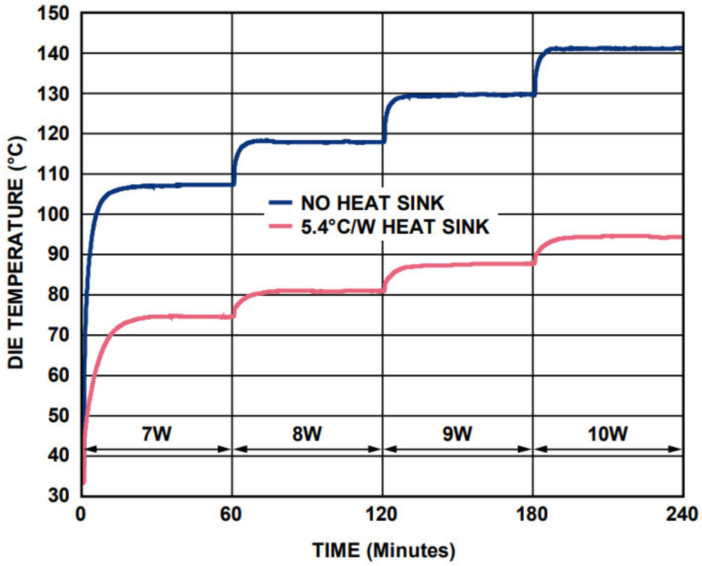


Figure 8. Die Temperature vs. Time and Internal Power Dissipation on the Evaluation Board, Ambient Temperature = 25°C, No Air Flow

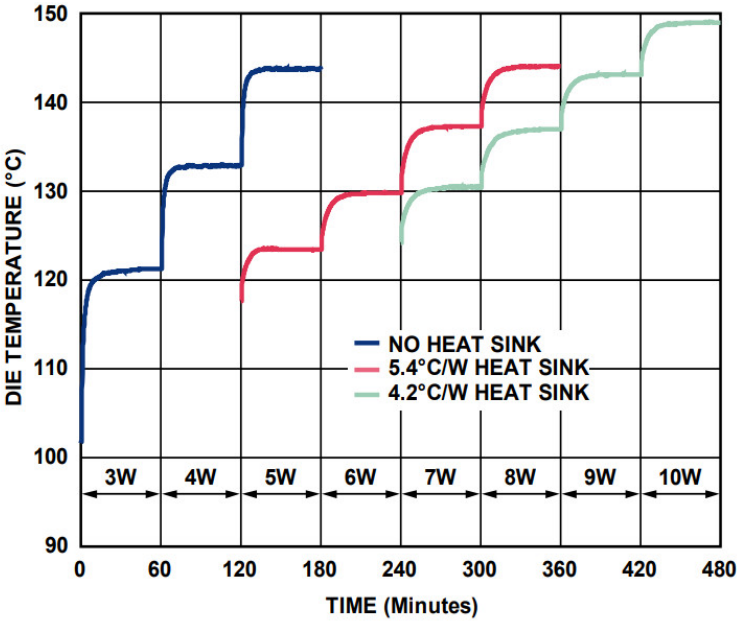
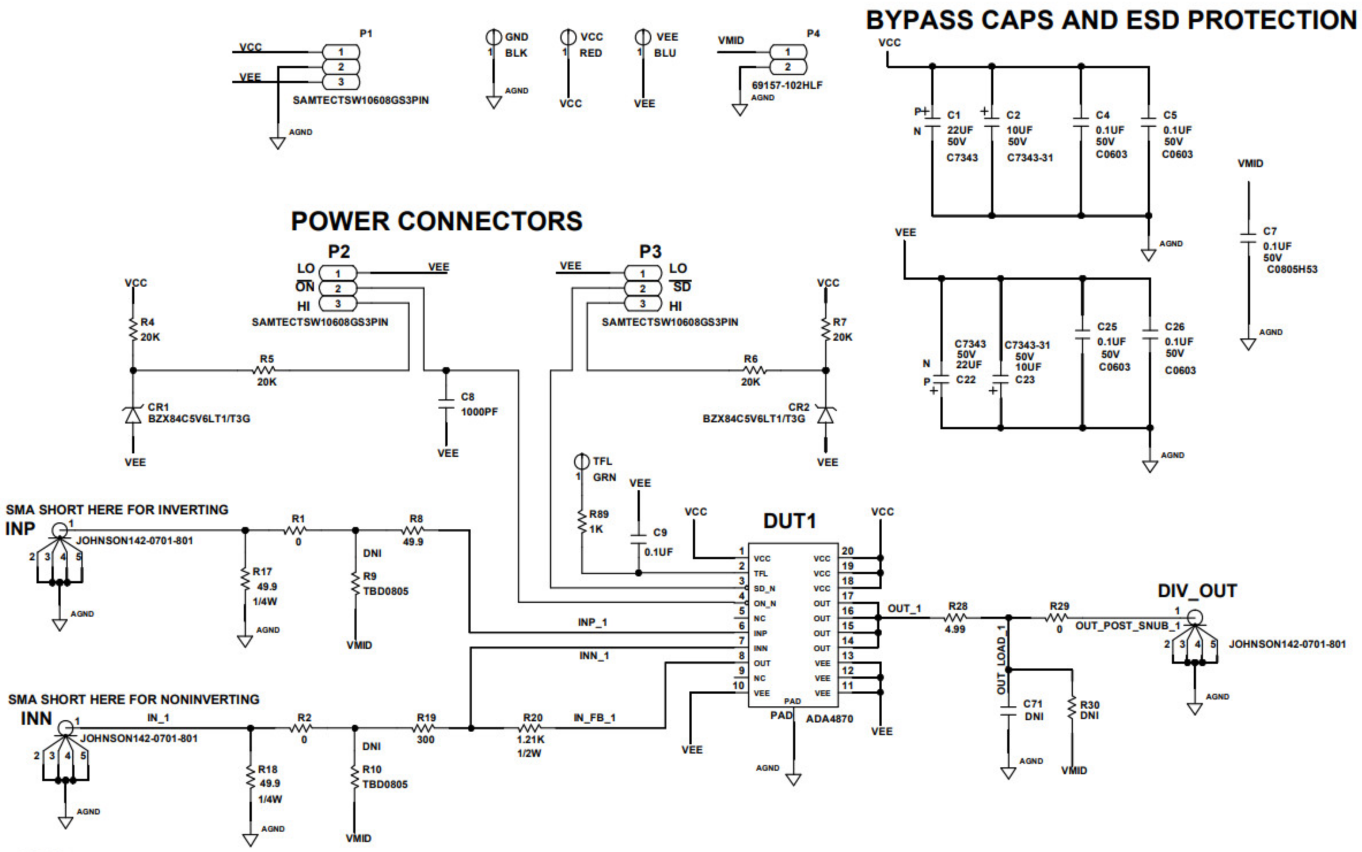


Figure 9. Die Temperature vs. Time and Internal Power Dissipation on the Evaluation Board, Ambient Temperature = 85°C, No Air Flow

EVALUATION BOARD SCHEMATIC



NOTES
1. CHANGE R1 OR R2 TO CAPACITOR (C1 OR C2) WHEN INPUT AC COUPLING IS REQUIRED.

Figure 10. Evaluation Board Schematic

BILL OF MATERIALS

Table 2.

Item	Qty	Reference Designator	Description	Value	Manufacturer/Part No.
1	1	Not applicable	ADA4870 evaluation board	Not applicable	Analog Devices/ADA4870ARR-EBZ
2	1	DUT1	ADA4870	Not applicable	Analog Devices/ADA4870
3	2	C1 ,C22	Capacitor, tantalum, 7343	22 µF	AVX/TAJD226K050R
4	2	C2, C23	Capacitor, tantalum, 7343	10 µF	AVX/TAJD106M050RNJ
5	5	C4, C5, C9, C25, C26	Capacitor, ceramic, X7R, 0603	0.1 µF	AVX/06035C104KAT2A
6	1	C7	Capacitor, ceramic, X7R,0805, 50 V	0.1 µF	Murata/GRM21BR71H104KA01L
7	1	C71	Capacitor, ceramic, COG, 0603, 50 V	Not installed	Murata/GRM1885C1H301JA01D
8	1	C8	Capacitor ceramic, X7R, 0603, 50 V	1000 pF	AVX/06035C102KAT2A
9	2	CR1, CR2	Diode, Zener, SOT-23	5.6 V	ON Semiconductor/BZX84C5V6LT1/T3G
10	3	INP, INN, DIV_OUT	Connector, SMA end launch	Not applicable	Johnson/142-0701-801
11	1	GND	Connector, test point	Black	Components Corporation/TP104-01-00
12	3	P1, P2, P3	Connector, PCB, berg, header, straight,	Not applicable	Samtec/TSW-103-08-G-S
			male, 3P		

13	1	P4	Connector, PCB, berg, jumper , straight,	Not applicable	FCI/69157-102HLF
			male, 2P		
14	2	R1, R2	Resistor, 0603, jumper	0 Ω	Panasonic/EERJ-3GEY0R00V
15	2	R9, R10	Resistor, 0805	Not installed	
16	2	R17, R18	Resister, 1206, 1%	49.9 Ω	Panasonic/ERJ-8ENF49R9V
17	1	R19	Resistor, 1206, 1%	300 Ω	Vishay Dale/CRCW1206300RFKEA
18	1	R20	Resistor, 2010, 1%	1.21 kΩ	Panasonic/ERJ-12SF1211U
19	1	R28	Resistor, 2512, 1%	4.99 Ω	Vishay Dale/CRCW25124R99FKEG
20	1	R29	Resistor, 1206, jumper	0 Ω	Vishay Dale/CRCW12060000Z0EA
21	1	R30	Resistor, TO-220	Not installed	
22	4	R4, R5, R6, R7	Resistor, 0603, 1%	20 kΩ	Panasonic/ERJ-3EKF2002V
23	1	R8	Resistor, 0603, 1%	49.9 Ω	Panasonic/ERJ-3EKF49R9V
24	1	R89	Resistor, 0603, 1%	1 kΩ	Panasonic/ERJ-3EKF1001V
25	1	TFL	Connector, test point	Green	Components Corporation/TP104-01-05
26	1	VCC	Connector, test point	Red	Components Corporation/TP104-01-02

27	1	VEE	Connector, test point	Blue	Components Corporation/TP104-01-06
28	2	Jumper	Jumper socket for P2 and P3	Not applicable	FCI/65474-001LF

NOTES ……

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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By using the evaluation board discussed herein (together with any tools, components documentation, or support materials, the “Evaluation Board”), you are agreeing to be bound by the terms and conditions set forth below (“Agreement”) unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you (“Customer”) and Analog Devices, Inc. (“ADI”), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. The customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term “Third Party” includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. The customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customers may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board.

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References

- Mixed-signal and digital signal processing ICs | Analog Devices