ANALOG DEVICES LTM4709 Triple 3A Ultralow Noise High PSRR Ultrafast Module Instruction Manual

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Contents

DESCRIPTION

Demonstration circuit 3211A features the LTM®4709, a triple 3A, ultralow noise, high PSRR, and ultrafast µModule® linear regulator with a configurable output array. The input voltage (VINn) range is from 0.6V to 5.5V. There are jumpers to set a 3-bit trilevel code that determines the output voltage (VOUTn) at preprogrammed levels that range from 0.5V to 4.2V. The maximum output current per channel is 3A. The DC3211A requires an external BIAS voltage (VBIASn) at least 1.2V higher than VOUTn and between 2.375V and 5.5V.

The LTM4709 of the DC3211A requires few external components, therefore, simplifying the circuit design and significantly reducing solution size. External component choice and carefully printed circuit board (PCB) design

help optimize noise, Power Supply Rejection Ratio (PSRR), load transient response, and VOUTn regulation performance. The LTM4709 only requires ceramic capacitors for the power input and the power output. The 22µF capacitor at the circuit output was chosen for high frequency PSRR performance and to minimize VOUTn deviation during load transients.

The capacitor that bypasses the VINn power for the LTM4709 and the corresponding VINn PCB layout can affect PSRR (see the Best PSRR Performance: PCB Layout for Input Traces section for additional information). The DC3211A decouples the VINn power with a 4.7µF capacitor (see the LTM4709 data sheet for the minimum capacitor value required for VINn). Note that an optional bulk 220µF tantalum polymer capacitor further reduces VINn variation during load transients and reduces input voltage ringing that can be caused by inductive input power leads.

The LTM4709 has a precision current monitor that provides accurate current monitoring for the energy management system and current limit. An IMONn terminal is available for the current monitoring of each channel. The IMONn voltage is the product of the resistance that programs the current limit and the IMONn pin current, which is 1/3000 of the output current. By default, the DC3211A has a 3.3A current limit per channel with IMONRn tied to GND. However, custom current limit levels can be programmed by floating IMONRn and connecting a resistor from IMONn to GND. The externally programmed current limit is triggered when the IMONn voltage is 1V.

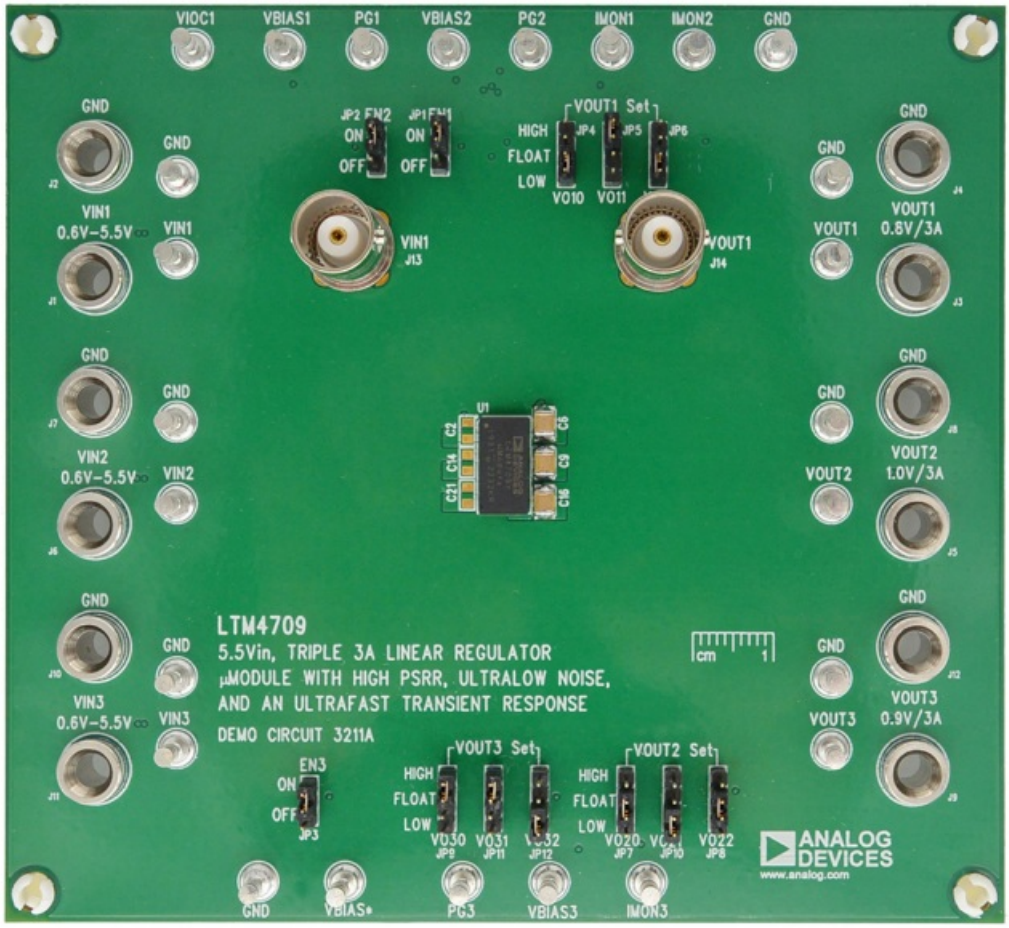
ENn jumpers (JP1, JP2, JP3) are available on the DC3211A to either connect each channel's ENn pin to VBIASn to turn the output on or to ground to disable the output. There is a PGn terminal for each channel that is pulled up to VBIASn by a 100k resistor when PGRn is connected to BIAS. PGn is pulled down by an open-drain, n-channel metal-oxide semiconductor (nMOS) output for indication of regulator output status, and other fault modes. The voltage inputto-output control (VIOC1) terminal allows connections for automatically regulating the difference between the input voltage and output voltage of the LTM4709 to be a fixed value.

The LTM4709 data sheet must be read in conjunction with this demo manual before working on or modifying demonstration circuit DC3211A.

Design files for this circuit board are available.

BOARD PHOTO

Part marking is either ink mark or laser mark



PERFORMANCE SUMMARY

Specifications are at TA = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		0.6		5.5V	V
BIAS Voltage Range	VBIAS ≥ VOUT + 1.2V, VBIAS ≥ VIN	2.375		5.5V	V
Output Voltage Range	VOUT = 0.5V, 10mA ≤ IOUT ≤ 3A, 0.7V ≤ VIN ≤ 0.9V VOUT = 1.0V, 10mA ≤ IOUT ≤ 3A, 1.2V ≤ VIN ≤ 1.4V VOUT = 1.2V, 10mA ≤ IOUT ≤ 3A, 1.4V ≤ VIN ≤ 1.6V VOUT = 3.3V, 10mA ≤ IOUT ≤ 3A, 3.5V ≤ VIN ≤ 3.7V VOUT = 4.2V, 10mA ≤ IOUT ≤ 3A, 4.4V ≤ VIN ≤ 4.6V	0.492 0.988 1.182 3.250 4.137	0.500 1.000 1.200 3.300 4.200	0.508 1.012 1.218 3.350 4.263	V V V V V
Output Current	Per Channel	10		3000	mA

QUICK START PROCEDURE

Demonstration circuit 3211A is an easy way to evaluate the performance of the LTM4709. See Figure 1 for proper measurement equipment setup and follow the procedure below.

1. With the input supplies off and turned down, make all the connections shown in Figure 1. Ensure that the VOn0, VOn1, and VOn2 jumpers to set VOUTn are in the proper positions for the desired output voltage according to the VOUTn selection matrix table in the LTM4709 data sheet. Also, ensure that the ENn jumpers (JP1, JP2, JP3) are in the ON position.
2. Turn on the input and bias supplies. Increase each input supply so it is 300mV above the programmed output voltage. Adjust VBIAS* so it is between 2.375V and 5.5V and at least 1.2V higher than the highest programmed VOUTn channel for proper operation. Note that when setting the input and bias voltages, a VINn or VBIASn that is too close to the programmed VOUTn (too low) can cause dropout operation and a loss of VOUTn regulation. Also, a VINn that is too high above the output can increase power dissipation to an unacceptable level.
3. Increase the load to the desired IOUTn. Readjust the input supply to be 300mV above the programmed output voltage. Verify that VOUTn is the expected voltage programmed by the jumpers. Note that for the most accurate measurements, measure the input and output voltages directly from the input and output capacitors. This will avoid any voltage drop from the vias or copper traces.
4. When the proper VOUTn is established, adjust the input voltages and load within the operating ranges and observe the VOUTn regulation, load transient response, and other parameters.
5. Refer to application notes AN83 and AN159 for measuring output noise and PSRR. Note that J13 and J14 are BNC connectors that are used for noise and PSRR measurements for channel 1.
6. Monitor power good at the PGn terminals and the output current at the IMONn terminals.
7. Refer to the LTM4709 data sheet for the usage of the VIOC1 terminal.

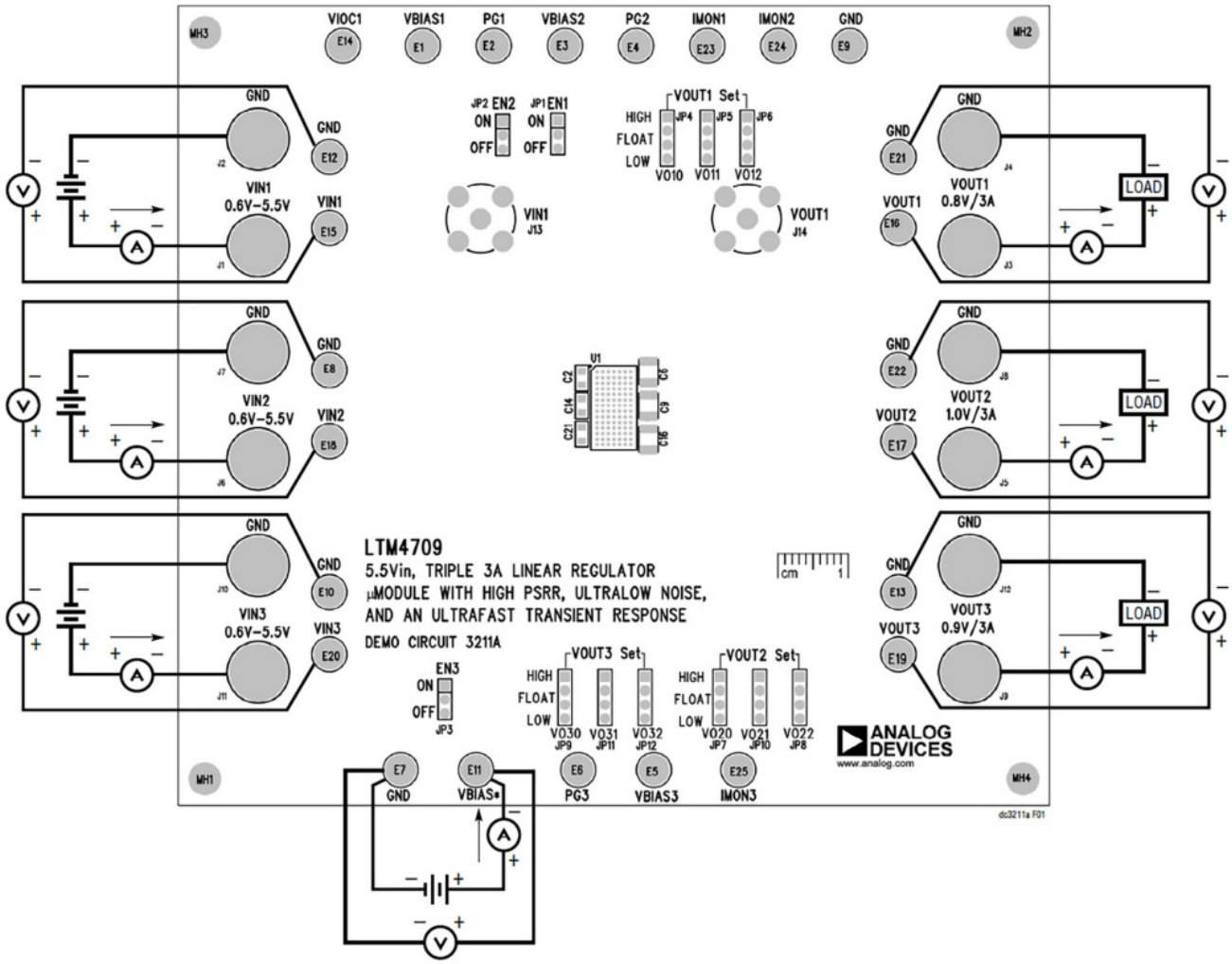


Figure 1. Measurement Setup of DC3211A

TYPICAL PERFORMANCE CHARACTERISTICS

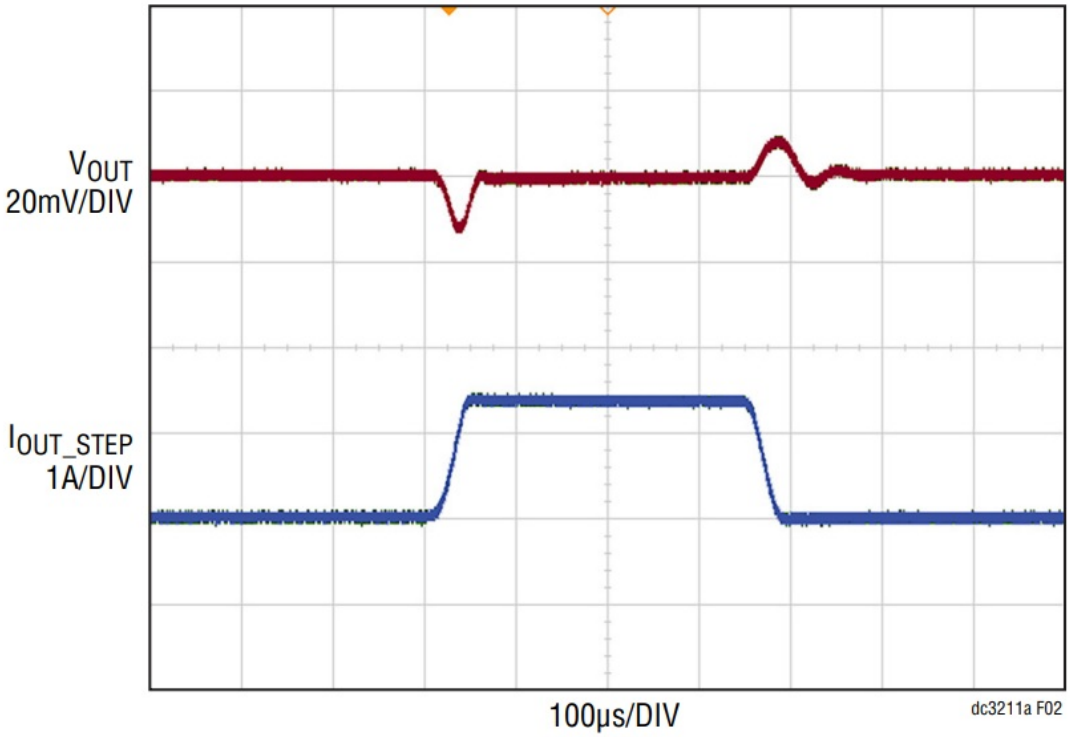


Figure 2. Load Step of LTM4709 on the DC3211A (Channel 1 Only) V_{BIAS} = 5V, V_{IN1} = 1.3V, V_{OUT1} = 1V, I_{OUT_STEP} = 0.3A to 3A, 3A/µs Slew Rate

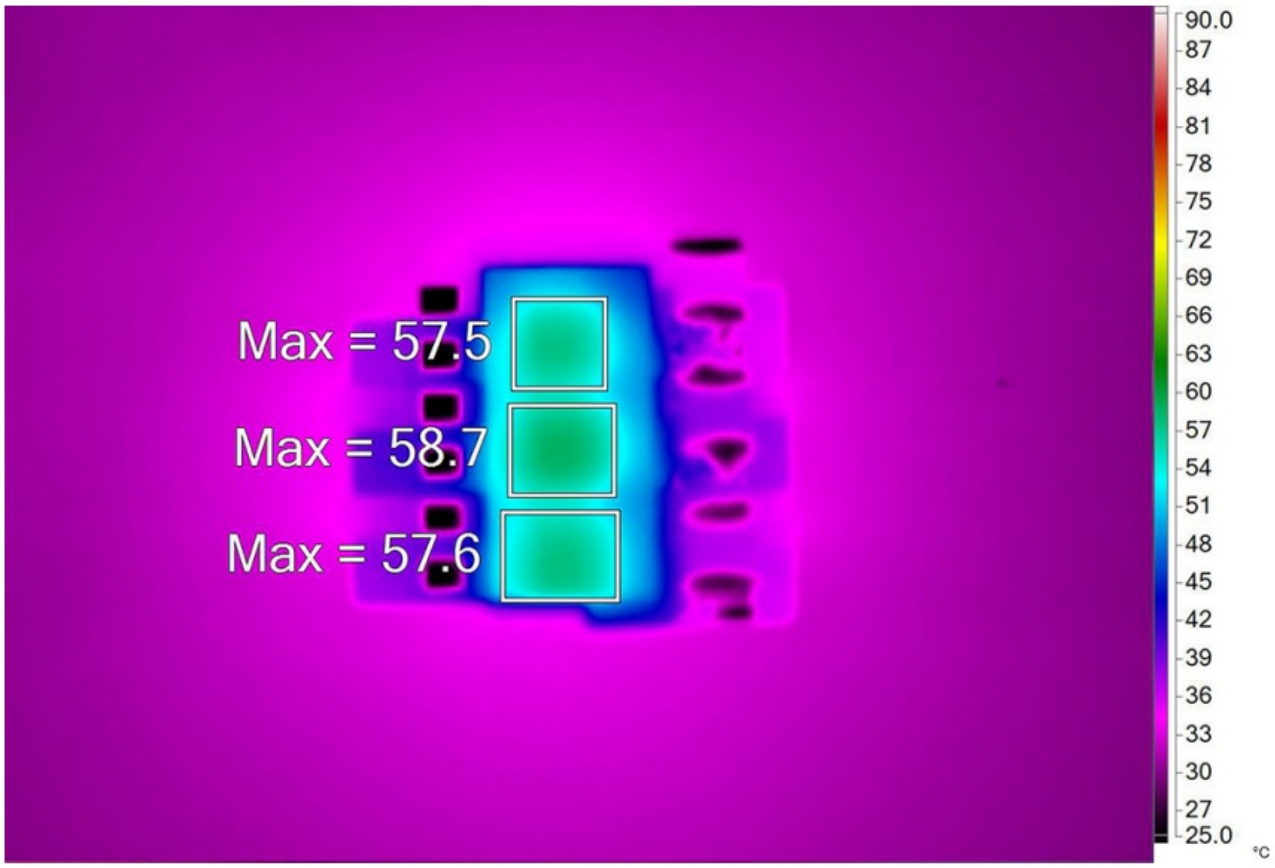


Figure 3. Thermal Image of LTM4709 on the DC3211A V_{BIAS} = 2.5V, V_{IN1} = 1.1V, V_{OUT1} = 0.8V, V_{IN2} = 1.3V, V_{OUT2} = 1V, V_{IN3} = 1.2V, V_{OUT3} = 0.9V, $I_{OUT1,2,3}$ = 3A, No Airflow, T_A = 25°C

PRINTED CIRCUIT BOARD (PCB) LAYOUT

BEST PSRR PERFORMANCE: PCB LAYOUT FOR INPUT TRACES

For applications using the LTM4709 for post-regulating switching converters, placing a capacitor directly at the LTM4709 input results in AC current (at the switching frequency) flowing near the LTM4709. Without careful attention to the PCB layout, this relatively high frequency switching current generates an electromagnetic field (EMF) that couples with the LTM4709 output, degrading its effective PSRR. While highly dependent on the PCB, the switching preregulator, the input capacitor size, and other factors, the PSRR can easily degrade at high frequencies. This degradation is present even if the LTM4709 is desoldered from the board because it effectively degrades the PSRR of the PCB itself. While negligible for conventional low PSRR low dropout (LDO) regulators, the high PSRR of the LTM4709 requires careful attention to higher order parasitics to realize the full performance offered by the regulator.

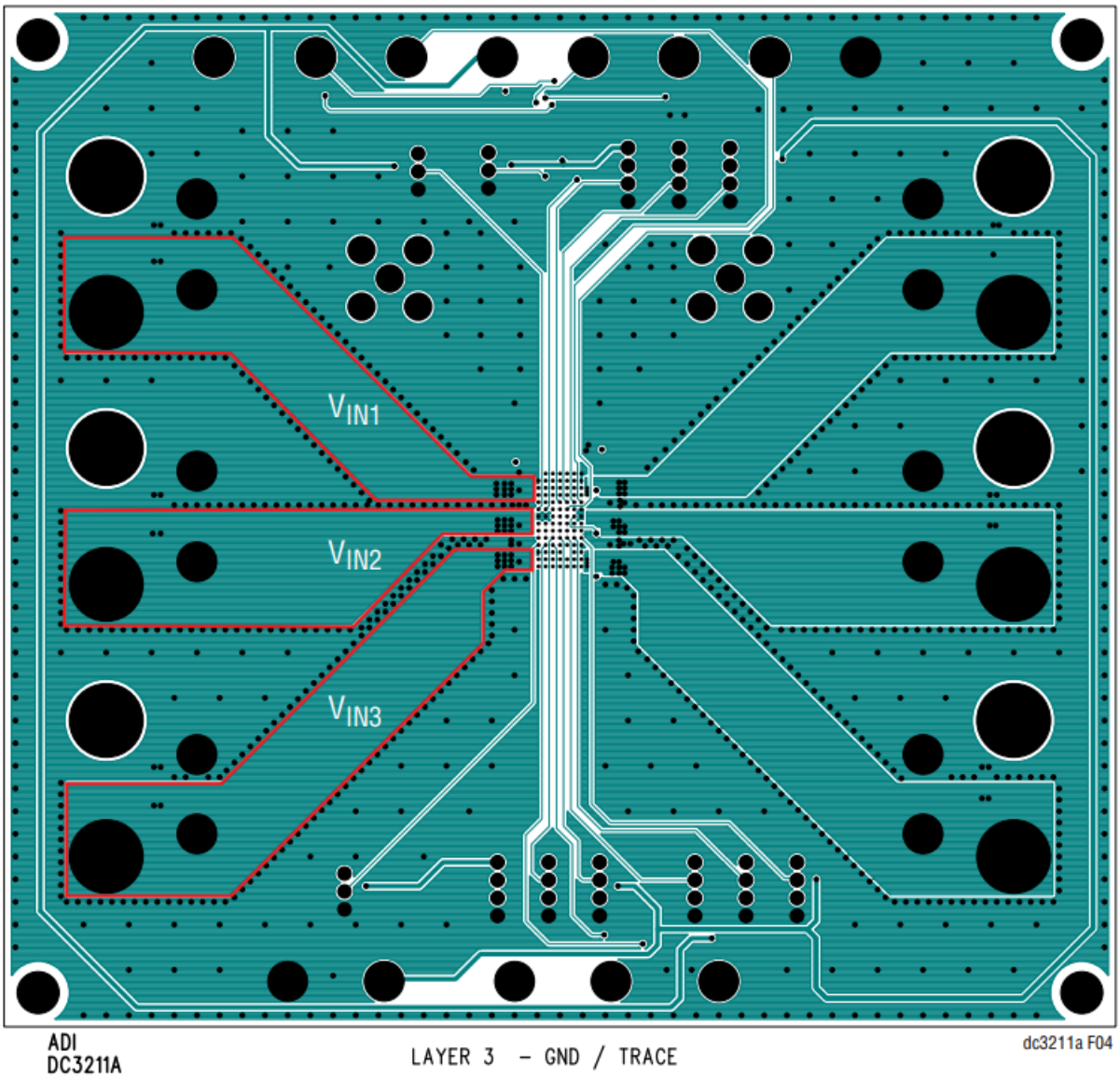


Figure 4. Layer 3 of DC3211A

The DC3211A alleviates this degradation in PSRR by using a specialized layout technique. On Layer 3, the input traces (VINn) are highlighted in red (see Figure 4) with the return paths (GNDn) highlighted on Layer 4, along with the input capacitors for each channel (see Figure 5). When an AC voltage is applied to the input of the DC3211A, AC current flows on the path formed through the input capacitors by the input and ground traces. Without the proper PCB layout, the AC current that flows on this path can generate EMFs that do not completely cancel and couple to the output capacitors and related traces, making the PSRR appear worse than it is. With the input trace directly above the return path, the EMFs are in opposite directions, and consequently, cancel each other out. Ensure that these traces exactly overlap each other to maximize the cancellation effect and thus provide the maximum PSRR offered by the regulator.

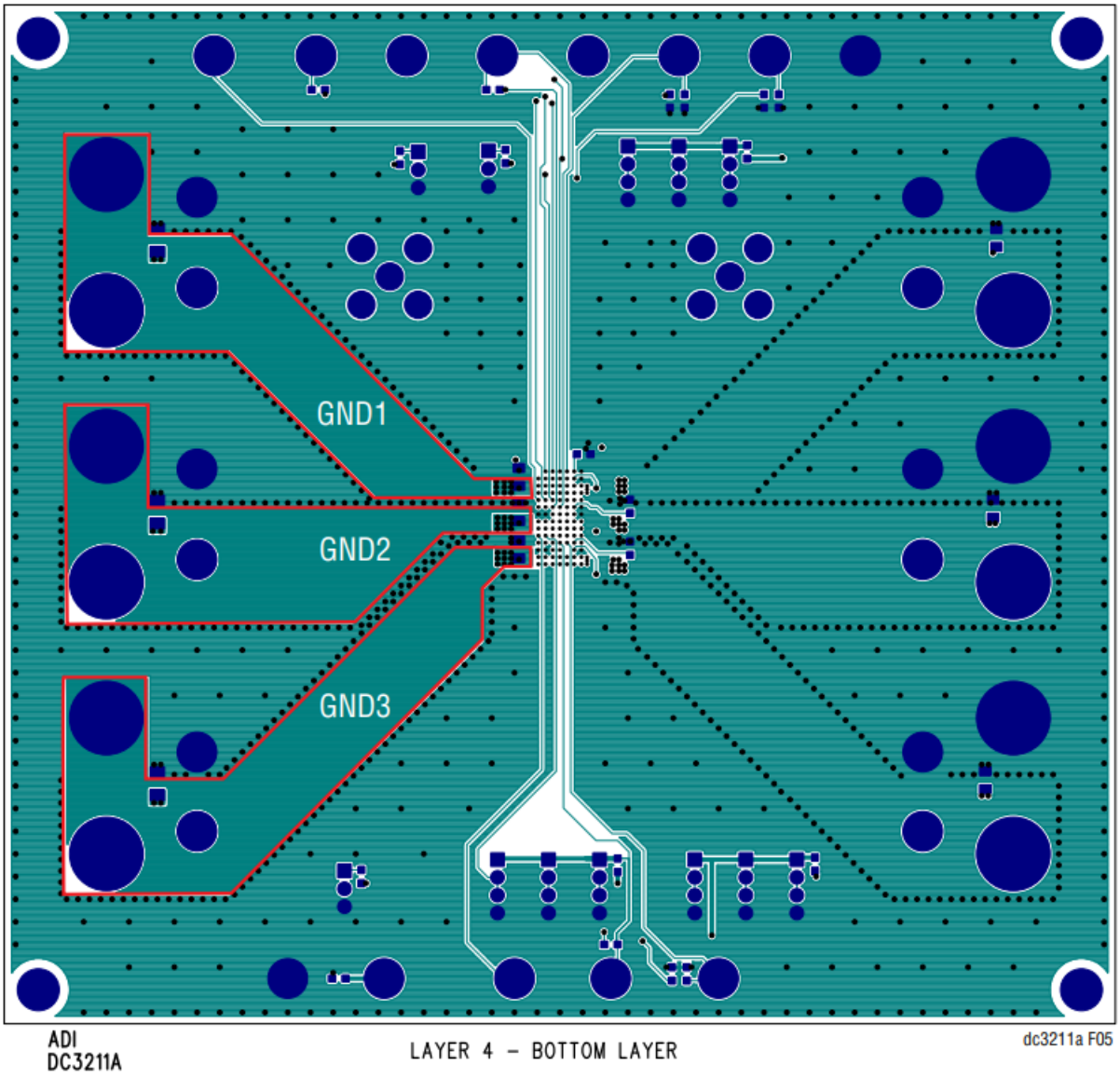


Figure 5. Layer 4 of DC3211A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER

Required Circuit Components

1	1	C1	CAP., 4.7µF, X5R, 16V, 10%, 0603	MURATA, GRM188R61C475KAAJD, GRM188R61C475KE11D; AVX, 0603YD475KAT2A; TDK, C1608X5R1C475K080AC
2	3	C4, C15, C22	CAP., 4.7µF, X7R, 16V, 10%, 0805	TAIYO YUDEN, MSASE21GSB7475KTNA01
3	3	C5, C13, C20	CAP., 22µF, X7R, 10V, 10%, 1206	MURATA, GRM31CR71A226KE15L; SAMSUNG, CL31B226KPHNNWE
4	3	C6, C9, C16	CAP., 22µF, X7R, 25V, 10%, 1210	MURATA, GRM32ER71E226KE15L
5	3	R1-R3	RES., 100k, 1%, 1/10W, 0603	STACKPOLE ELECTRONICS, RMCF0603FG100K; YAGEO, RC0603FR-07100KL
6	9	R4-R9, R11, R13, R15	RES., 0Ω, 1/10W, 0603	BURNS, CR0603-J/-000ELF; VISHAY, CRCW06030000Z0EAC; YAGEO, RC0603FR-070RL
7	1	U1	IC, TRIPLE 3A LINEAR REGULATOR µModule, BGA-98, LOW VOLTAGE, PRELIM	ANALOG DEVICES, LTM4709IY#PBF

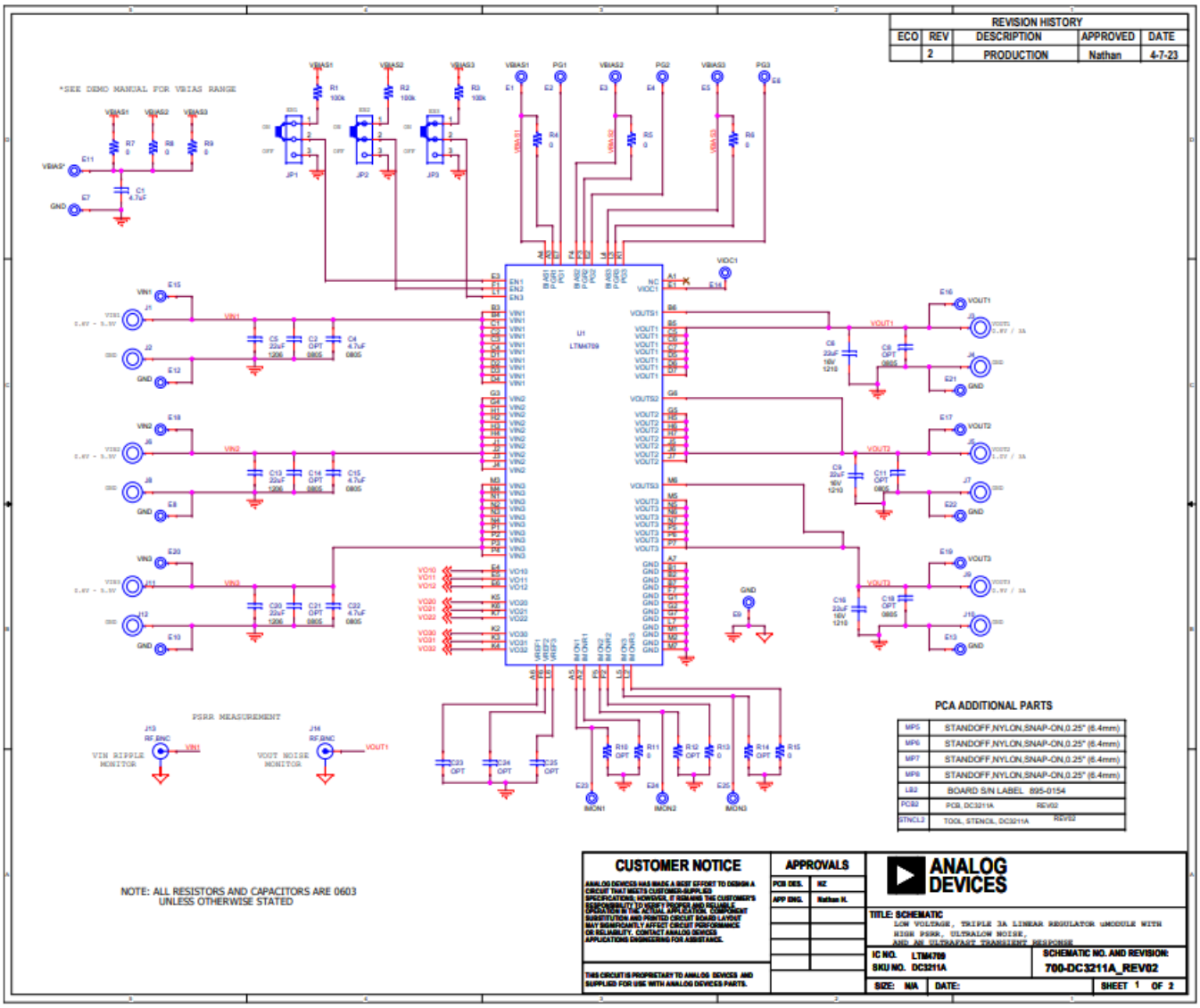
Additional Demo Board Circuit Components

1	0	C2, C8, C11, C14, C18, C21	CAP., OPTION, 0805	
2	0	C23-C25	CAP., OPTION, 0603	
3	0	R10, R12, R14	RES., OPTION, 0603	

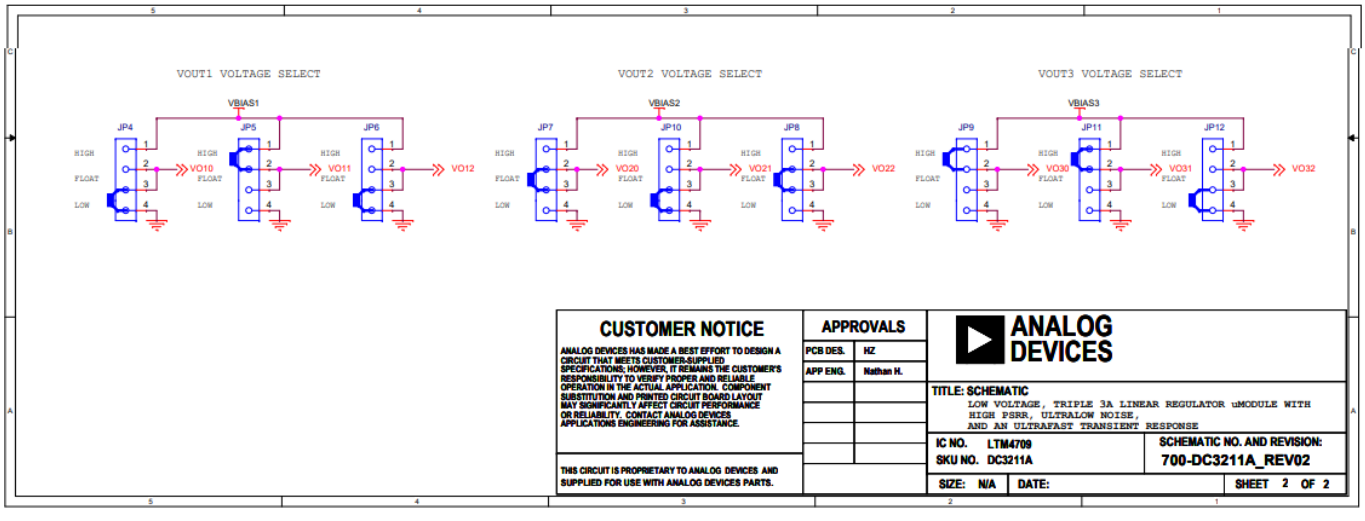
Hardware: For Demo Board Only

1	25	E1-E25	TEST POINT, TURRET, 0.094″ MTG. HOLE, PCB 0.062″ THK	MILL-MAX, 2501-2-00-80-00-00-07-0
2	12	J1-J12	CONN., BANANA JACK, FEMALE, THT, NON INSULATED, SWAGE, 0.218″	KEYSTONE, 575-4
3	2	J13, J14	CONN., RF, BNC, RCPT, JACK, 5-PIN, ST, THT, 50Ω	AMPHENOL RF, 112404
4	3	JP1-JP3	CONN., HDR., MALE, 1×3, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000311121
5	9	JP4-JP12	CONN., HDR, MALE, 1×4, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000411121
6	12	XJP1-XJP12	CONN., SHUNT, FEMALE, 2-POS, 2 mm	WURTH ELEKTRONIK, 60800213421
7	4	MP5-MP8	STANDOFF, NYLON, SNAP-ON, 0.25″ (6.4mm)	WURTH ELEKTRONIK, 702931000
8	1	LB1	LABEL SPEC, DEMO BOARD SERIAL NUMBER	BRADY, THT-96-717-10
9	1	PCB1	PCB, DC3211A	ADI APPROVED SUPPLIER, 600-DC3211A
10	1	STNCL1	TOOL, STENCIL, DC3211A	ADI APPROVED SUPPLIER, 830-DC3211A

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	07/23	Initial Release	—

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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- Mixed-signal and digital signal processing ICs | Analog Devices