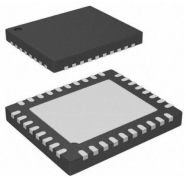

ANALOG DEVICES LTC4417 Prioritized PowerPath Controller User Guide

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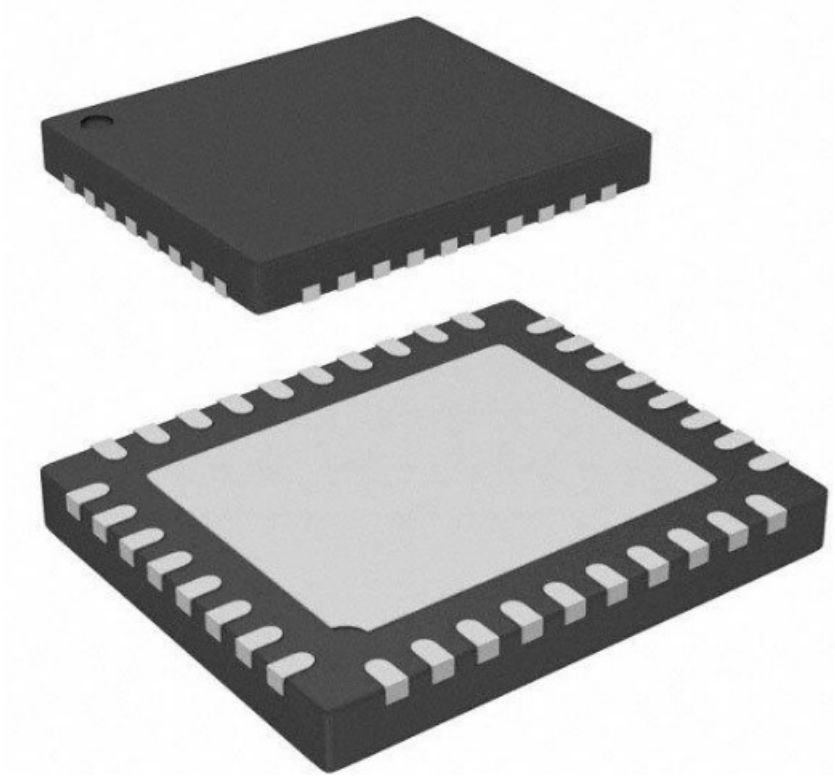


Product Information

Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V1-V3, VOUT	V1 to V3, VOUT Operating Supply Range		2.5		36	V
VG	Open (VS-VG) Clamp Voltage	VOUT = 11V, G1 to G3 = Open	5.4	6.2	6.7	V
VG(SOURCE)	Sourcing (VS-VG) Clamp Voltage		5.8	6.6	7	V
VG(SINK)	Sinking (VS-VG) Clamp Voltage		4.5	5.2	6	V
VG(OFF)	G1 to G3 Off (VS-VG) Threshold	V1 = V2 = V3 = 2.8V, VOUT = 2.6V, G1 to G3 Rising Edge	0.12	0.35	0.6	V
VG(SLEW,ON)	G1 to G3 Pull-Down Slew Rate	VOUT = 11V, CGATE = 10nF	4	9	20	
VG(SLEW,OFF)	G1 to G3 Pull-Up Slew Rate	VOUT = 11V, CGATE = 10nF	7.5	13	22	
IGATE(LOW)	G1 to G3 Low Pull-Down Current	VOUT = 2.6V, V1 to V3 = 2.8V, (G1 to G3) = VG + 300mV	0.8	2	7	
VREV	Reverse Voltage Threshold		30	120	200	mV

tG(SWITCHOVER)	Break-Before-Make Time	VOUT = 11V, CGATE = 10nF	0.7	2	3	
VVALID(OL)	VALID1 to VALID3 Output Low Voltage	I = 1mA, (V1 to V3) = 2.5V, VOUT = 0V	0.2	0.55		V
tPVALID(OFF)	VALID1 to VALID3 Delay OFF from OV/UV Fault		5	8	13	
VSHDN(THR)	SHDN Threshold Voltage		0.4	0.8	1.2	V
VSHDN_EN(HYS)	SHDN, EN Threshold Hysteresis		100			mV
ISHDN_EN	EN Pull-Up Current					
VOV_UV(THR)	OV1 to O3, UV1 to UV3 Comparator Threshold	SHDN Rising, SHDN = EN = 0V VOUT = 11V, OV1 to OV3 Rising, UV1 to UV3 Falling		0.985	1.015	V
VOV_UV(HYS)	OV1 to O3, UV1 to UV3 Comparator Hysteresis	VOUT = 11V	15	30	45	mV
tVALID	V1 to V3 Validation Time		100	256	412	ms
V1	Operating Voltage of Channel V1		9.6	12	14.4	V
V2	Operating Voltage of Channel V2		4	5	6	V
V3	Operating voltage of Channel V3		6.4	8	9.6	V
ILOAD AVI	Load Current Auxiliary Voltage Input		2		6	A, V

Product Usage Instructions

Overview

The LTC4417 is a prioritized PowerPathTM controller thatcontrols three sets of external back-to-back P-channel MOSFETs to connect the proper rail to the load. It uses precision comparators to monitor each of the three input rails for undervoltage (UV) and overvoltage (OV) conditions. The highest priority input supply whose voltage is within its respective OV/UV window for at least 256ms is considered valid and connected to the load. The VALID1, VALID2, and VALID3 pins indicate the validation of the V1, V2, and V3 voltages. Logic and LEDs are included to provide visual information aboutthe operating status. The circuits are powered from a 6V to 24V auxiliary voltage input (AVI) which is regulated by an LT3060 (U4) to 5V. The auxiliary 5V rail also powers 100k pull-ups for VALID pins. The presence of AVI is necessary for the board to operate.

Operating Principles

To eliminate back-and-forth switching during rail switchover, the LTC4417 provides a 30mV hysteresis in the OV and UV comparators. The OV/UV resistive dividers allow for an externally adjustable current mode hysteresis. The DC1717B board has a default input reference hysteresis of 6%, but it can be changed to 3% by moving the JP1 jumper to the 30mV position.

DESCRIPTION

Demonstration circuit DC1717B uses the LTC®4417 arbitrate between three input supply rails, selecting the highest priority, valid supply to power the load. The rail's priority is defined by the input connection (V1-V3). Each rail has overvoltage and undervoltage thresholds set by external resistors. If the highest priority rail voltage falls out of the defined window (overvoltage or undervoltage), the rail with the next highest priority, which is valid, is enabled and powers the load. Two or more LTC4417s can be cascaded to provide switchover between more than three rails. Design files for this circuit board are available at **www.analog.com/DC1717B**.

PERFORMANCE SUMMARY

Specifications are at TA = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V1-V3, VOUT	V1 to V3, VOUT Operating Supply Range		2.5		36	V
ΔVG	Open (VS-VG) Clamp Voltage	VOUT = 11V, G1 to G3 = Open	5.4	6.2	6.7	V
ΔVG(SOURCE)	Sourcing (VS-VG) Clamp Voltage	VOUT = 11V, I = –10µA	5.8	6.6	7	V
ΔVG(SINK)	Sinking (VS-VG) Clamp Voltage	VOUT = 11V, I = 10µA	4.5	5.2	6	V
ΔVG(OFF)	G1 to G3 Off (VS-VG) Threshold	V1 = V2 = V3 = 2.8V, VOUT = 2.6V, G1 to G3 Rising Edge	0.12	0.35	0.6	V
ΔVG(SLEW,ON)	G1 to G3 Pull-Down Slew Rate	VOUT = 11V, CGATE = 10nF	4	9	20	V/µs
ΔVG(SLEW,OFF)	G1 to G3 Pull-Up Slew Rate	VOUT = 11V, CGATE = 10nF	7.5	13	22	V/µs
IGATE(LOW)	G1 to G3 Low Pull-Down Current	VOUT = 2.6V, V1 to V3 = 2.8V, (G1 to G3) = ΔVG + 300mV	0.8	2	7	µA
VREV	Reverse Voltage Threshold	Measure (V1 to V3) – VOUT, VOUT Falling	30	120	200	mV
tG(SWITCHOVER)	Break-Before-Make Time	VOUT = 11V, CGATE = 10nF	0.7	2	3	µs
VVALID(OL)	VALID1 to VALID3 Output Low Voltage	I = 1mA, (V1 to V3) = 2.5V, VOUT = 0V		0.2	0.55	V
tPVALID(OFF)	VALID1 to VALID3 Delay OFF from OV/UV Fault		5	8	13	µs
VSHDN(THR)	SHDN Threshold Voltage	SHDN Rising	0.4	0.8	1.2	V
VSHDN_EN(HYS)	SHDN, EN Threshold Hysteresis		100			mV

ISHDN_EN	SHDN, EN Pull-Up Current	SHDN = EN = 0V	–0.5	–2	–5	µA
VOV_UV(THR)	OV1 to O3, UV1 to UV3 Comparator Threshold	VOUT = 11V, OV1 to OV3 Rising, UV1 to UV3 Falling	0.985	1	1.015	V
VOV_UV(HYS)	OV1 to O3, UV1 to UV3 Comparator Hysteresis	VOUT = 11V	15	30	45	mV
tVALID	V1 to V3 Validation Time		100	256	412	ms
V1	Operating Voltage of Channel V1		9.6	12	14.4	V
V2	Operating Voltage of Channel V2		4	5	6	V
V3	Operating voltage of Channel V3		6.4	8	9.6	V
ILOAD	Load Current		2			A
AVI	Auxiliary Voltage Input		6		24	V

OVERVIEW

The LTC4417 controls three sets of external back-to-back P-channel MOSFETs to connect the proper rail to the load. Precision comparators are used to monitor each of the three input rails for both UV and OV conditions. The highest priority input supply whose voltage is within its respective OV/UV window for at least 256ms is considered valid and connected to the load. Low signals on the VALID1, VALID2, and VALID3 pins indicate validation of the V1, V2, and V3 voltages.

DC1717B is designed to operate from inputs of 12V, 5V, and 8V, applied to V1, V2 and V3 respectively. The valid range of each supply is ±20%, as set by OV and UV comparators and their associated resistive dividers. V1 has the highest priority, V3 has the lowest. The highest priority input that is also within its valid range is selected to power the output. V1, V2 and V3 inputs are protected against input glitches of up to ±42V. Maximum load cur- rent is 2A, limited by MOSFET capability.

Logic and LEDs are included to provide visual information about the operating status. These circuits are powered from a 6V to 24V auxiliary voltage input (AVI) which is regulated by an LT3060 (U4) to 5V. This auxiliary 5V rail also powers 100kΩ pull-ups for VALID pins. AVI must be present in order for the board to operate. See the Modifica- tion section for a means of eliminating AVI.

OPERATING PRINCIPLES

To eliminate back-and-forth switching during rail switcho- ver, the LTC4417 provides a 30mV hysteresis in the OV and UV comparators, and an externally adjustable current mode hysteresis using the OV/UV resistive dividers. DC1717B's input reference hysteresis is 6%, and can be changed to 3% by moving the JP1 jumper to the 30mV position. The controller's "break-before-make" switching method prevents cross conduction between input channels and reverse current from the output capacitor into the selected input supply. Each channel's control circuit of the LTC4417 has a REV comparator, which monitors the connecting input supply and output load voltage. The REV comparator delays the connection until the output voltage droops 120mV below the input voltage. This prevents reverse current.

The LTC4417 has two common control pins: EN and SHDN. Pulling the EN pin below 1V turns off all external back-to- back P-channel MOSFETs. When this pin is driven above 1V, the highest priority valid channel is connected to the load. All these actions are provided without resetting the 256ms OV/UV timers. Pulling the SHDN

pin below 0.8V turns off all external back-to-back P-channel MOSFETs, placing the controller in a low current state and resetting the 256ms timers used to validate input rail voltages. It requires at least 256ms to validate each rail voltage after the SHDN pin signal goes high. The LTC4417 features two different driving modes for the P-channel MOSFET gates. One mode is provided by the internal soft-start circuitry, which limits output voltage slew rate to no more than 5V/ms. As the highest output voltage slew rate, usually, can impose the highest requirements for circuit components, 5V/ms should be taken into account as a worst case for component selection.

The soft-start circuitry is enabled each time under the following conditions:

- If the LTC4417 is first powered on, or
- If SHDN is forced low, or
- If VOUT falls below ~0.7V Soft-start is disabled when:
    - any channel turns off, including the channel that is soft
    - 32ms validation delay time has elapsed during the soft- start interval.

The other driving mode of the P-channel MOSFETs is used in the voltage switching operation, when the higher priority rail replaces the rail losing validity. The gate driver oper- ates with a fixed current, which is defined by the external component parameters RS and CS shown in Figure 1. The LTC4417 circuit designer should select the value of RS and CS based on the MOSFET parameters, power rail source characteristics, acceptable output voltage droop during transient, and the value of load capacitance.

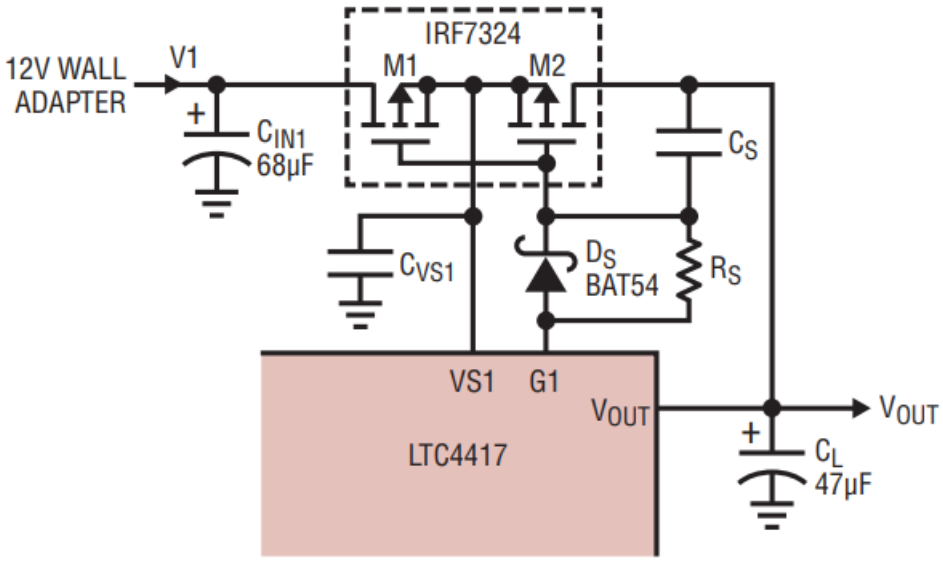


Figure 1

DESIGN PROCEDURE FOR MODIFICATION OF DC1717B

The valid input range for any supply is controlled by the OV and UV comparators with resistive dividers (R4-R13). See the LTC4417 data sheet for design equations to select resistors to match a particular requirement. Dual MOSFETs, Q1-Q3, may be replaced with single devices Q4-Q9 by simply removing Q1-Q3. Pads for Q4-Q9 are located on the bottom side of the board. The requirement for AVI may be eliminated by removing jumpers JP2 and JP3, and removing resistor R19. This modification leaves the LEDs unpowered and the inputs of U2 and U3 clamp the VALID pins at 0.7V, but otherwise leaves the LTC4417 operating autonomously. The following design considerations and equations dem-onstrate the interrelation of the main component values and transient parameters in the rail transitions, when the output voltage exceeds 0.7V. The variables CS and RS used in the design equations correspond to the following board components:

- C20, R23 for V1 (+12V channel)

- C21, R26 for V2 (+5.0V channel)
- C22, R28 for V3 (+8.0V channel)

To have dominant influence on the transient time CS should be at least ten times larger than the P-channel MOSFET's reverse transfer capacitance (Miller). In this design, for all rails, CS (C20, C21,and C22) equals 47nF.

The slew rate of the output voltage can be expressed as a function of CS:

$$\frac{dV_{OUT}}{dt} = \frac{dV_{CS}}{dt} = \frac{V_{SINK} - |V_{THRES}|}{R_S \bullet C_S} \qquad (1)$$

where:

- VSINK is the LTC4417 parameter rated in the data sheet as ΔVG(SINK) = 4.5V-6V.
- VTHRES is the P-channel gate threshold voltage, which is between –1.5V and –3.5V for the Si7905DN installed on the board.
- RS = 249Ω and CS = 47nF.

Given that dVOUT/dt is based on the transient time require-ment, it is possible to define RS from equation 1. The output voltage slew rate, dVOUT/dt, range for the circuit with the listed parameters is between 85V/ms and 385V/ms. During the transition of rails, the load can be disconnected from any rail for a time: TDISCON = tG(SWITCHOVER) + tpVALID(OFF) + tGATE_THRES Two first summands of the TDISCON are rated in the LTC4417 data sheet as:

1. tG(SWITCHOVER) = (0.3 to 3)µs
2. tpVALID(OFF) = (5 to 13)µs

The second summand, tpVALID(OFF), should be taken into account if the associated LTC4417 input does not have any bypass capacitor and the rail can be disconnected from the input instantly.

The third one must be calculated as:

$$t_{GATE\_THRES} = R_S \bullet C_S \left[-\ln\left(1 - \frac{V_{THRES}}{V_{SINK}}\right) \right] \qquad (2)$$

It is possible to determine the minimum capacitive load required to hold the output up during switchover as a:

$$C_{LOAD(MIN)} \geq \frac{I_{LOAD(MAX)} \bullet T_{DISCON}}{V_{OUT(DROOPMAX)}} \qquad (3)$$

where:

- ILOAD(MAX) is the maximum load current, A

- VOUT(DROOPMAX) is the maximum acceptable voltage droop, V

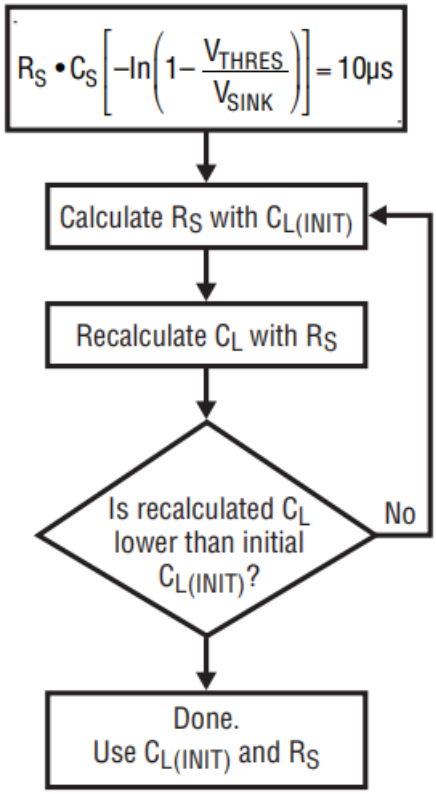


Figure 2

As shown in the equation (3), the use of external slew rate control will add additional delay to the total switchover time. Unfortunately, the actual components cannot be chosen until the load capacitance is known. This circular issue can only be resolved through an iterative process. The process starts by calculating the CLOAD(MIN), assuming that tGATE_THRES =10µs. For clarity this value will be labeled CLOAD(INIT). Using the calculated CLOAD(INIT), calculate RS from the expression of the TDISCON. To ensure the newly calculated RS based on CLOAD(INIT) is sufficient, calculate CLOAD with the calculated RS. If CLOAD(INIT) (the initial calculated CLOAD) is higher than the newly calculated CLOAD then the process is completed. If the CLOAD(INIT) is lower than the newly calculated CLOAD, calculate RS using the higher value and repeat this process.

TURRETS

- V1: 12V supply input; do not exceed ±42V.
- V2: 5V supply input; do not exceed ±42V.
- V3: 8V supply input; do not exceed ±42V.
- GND: Adjacent ground connection for input supplies. VOUT: Output for up to 2A load.
- GND: Adjacent ground connection for load.
- AVI: Auxiliary Voltage Input. 6V to 24V input regulated by U4 to 5V for LEDs, logic and pull ups on various pins.
- GND: Adjacent ground connection for auxiliary supply.
- 5V: 5V regulated output provided by U4, for powering logic, LEDs and pull ups. Use this turret to verify that 5V is present.

Each of the following turrets is a direct connection to the like-name LTC4417 pin:

- VALID1: pulled up with 100kOhm to auxiliary 5V supply.
- VALID2: pulled up with 100kOhm to auxiliary 5V supply.

- VALID3: pulled up with 100kOhm to auxiliary 5V supply.
- EN: pulled up by 2µA internal to the LTC4417. Optional R33 may be added as a pull-up to the auxiliary 5V power supply.
- SHDN: pulled up by 2µA internal to the LTC4417. Optional R36 may be added as a pull-up to the auxiliary 5V power supply.
- CAS: used to cascade a second DC1717B. Connect the CAS turret of the high priority DC1717B to the EN turret of the lower priority DC1717B.

Grounds must be connected in common.

JUMPERS

1. JP1, HYS: Add 30mV fixed hysteresis to the OV and UV comparators, or 3% referred to actual supply input. In the RHYS position input-referred hysteresis is set to 6.4%, as controlled by R11. Default stuffing position is for 30mV.
2. JP2, EN: Directly controls EN pin. Default stuffing position is ON, pulled up by internal 2µA current source.

LEADS
No more than one of D8, D9 and D10 will be illuminated at any given moment:

- D8: indicates power is being taken from V1.
- D9: indicates power is being taken from V2.
- D10: indicates power is being taken from V3.

D11, D16 and D17 indicate the presence of a valid input on any of the three supplies:

- D17: V1 is 12V±20%.
- D11: V2 is 5V±20%.
- D16: V3 is 8V±20%.

QUICK START PROCEDURE

Refer to the Figure 3 for proper measurement equipment setup and follow the procedure below: Initially, the LTC4417 should be disabled by:

- placing the jumper JP2 (EN) header in the OFF position, and
- placing the jumper JP3 (SHDN) header in the OFF position

1. Connecting the auxiliary power source (6V to 24V) to the DC1717B (AVI and GND turrets) lights the green LED (LDO-D12) indicating the presence of auxiliary +5V supply for powering logic.
2. With power off, connect three power supplies with output voltages of 12V, 5V, and 8V to corresponding DC1717B turrets or banana jacks V1(+12V), V2(+5V), V3(+8V), and GND.
3. Connect 6Ω load resistor (30W) to the DC1717B output turret or banana jack (VOUT). Do not use an electronic load in constant current mode.
4. Turn on three power supplies. No additional LEDs should light.

5. Change the jumper JP3 (SHDN) header position from OFF to ON. Three LEDs (VALID1, VALID2, and VALID3) validating the input rail voltages should light.
6. Placing the jumper JP2 (EN) in the ON position turns on the LTC4417 powering the load with 12V (2.0A). In an initial power up the LTC4417 uses a fixed slew rate for the output voltage, which should be not larger than 5V/ms.
7. The prioritizing function is demonstrated by simply turning off one or two of the V1, V2 and V3 supplies. The output will be powered from the remaining supply of the high-est priority. V1, V2 and V3 may be adjusted up and down beyond ±20% to invalidate a given input.

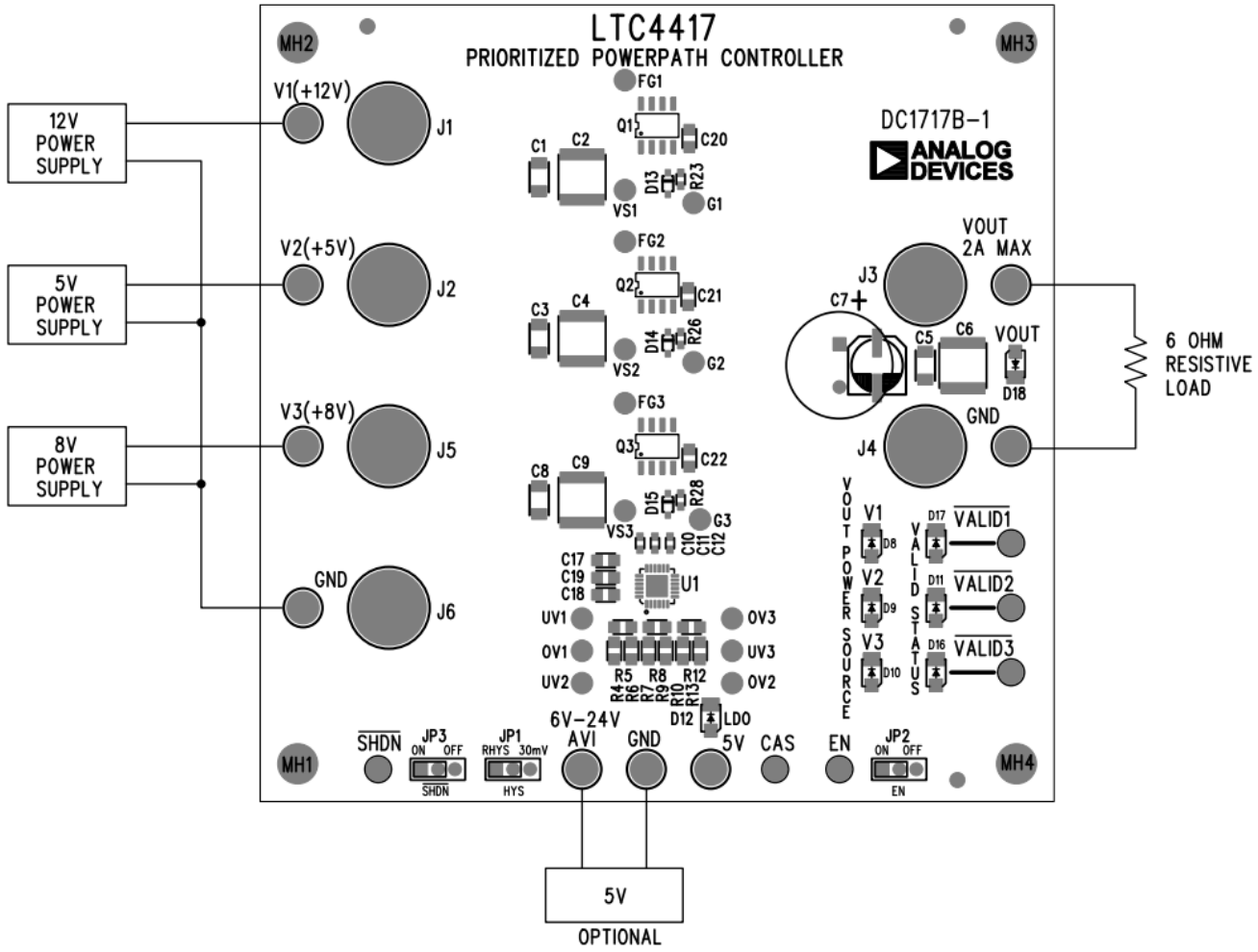


Figure 3

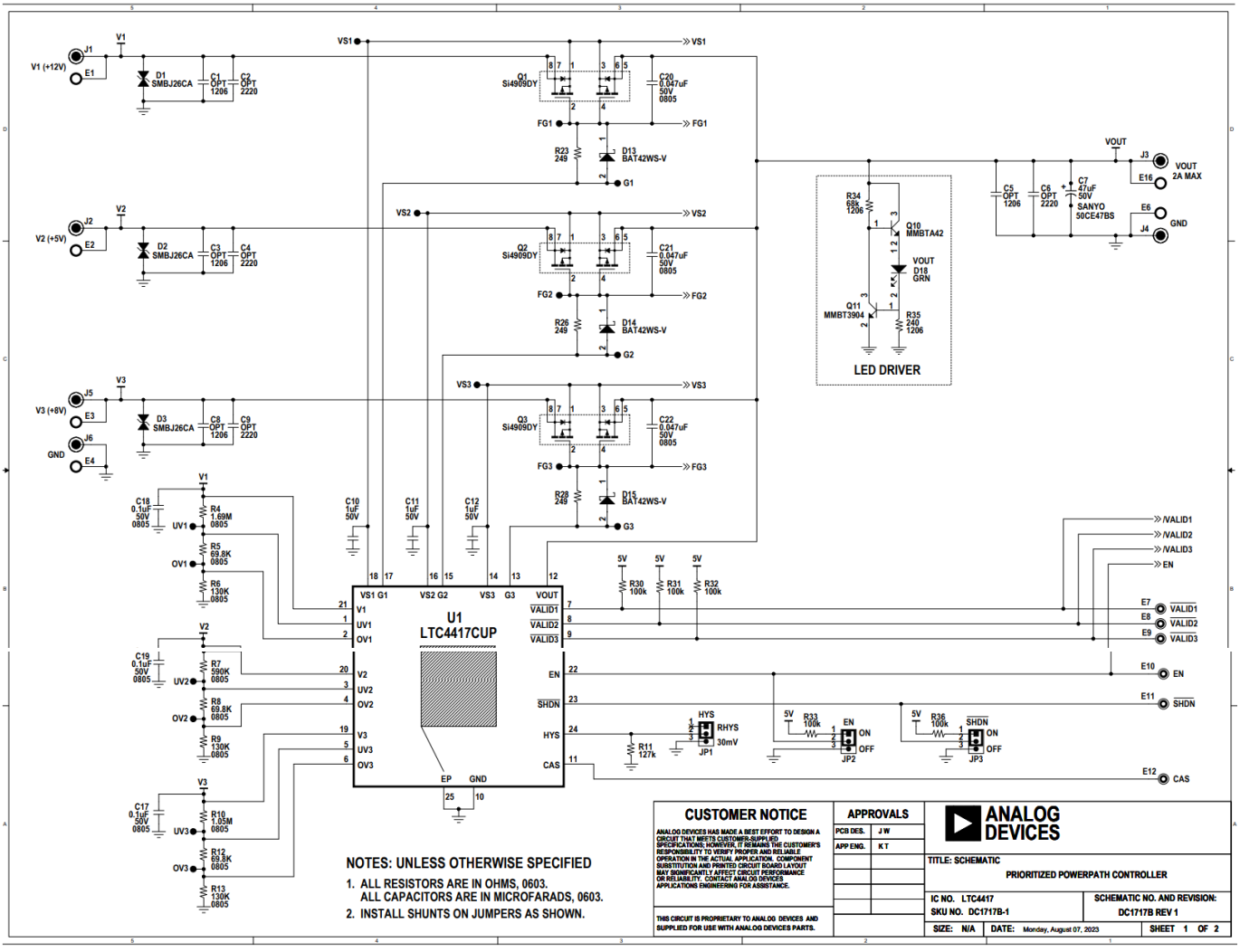
PARTS LIST

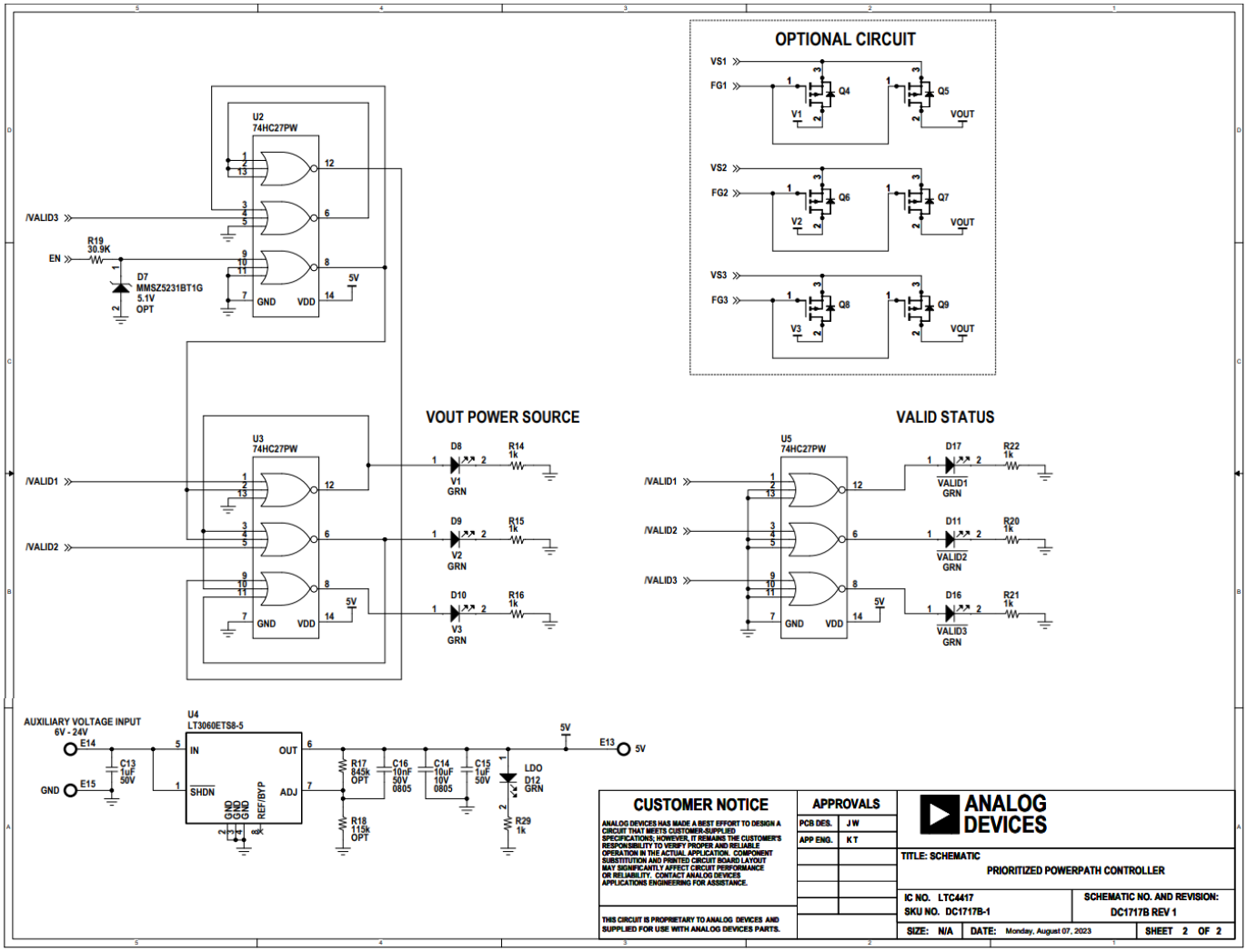
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	0	C1, C3, C5, C8	CAP., 1206	OPT
2	0	C2, C4, C6, C9	CAP., 2220	OPT
3	1	C7	CAP., ALUM., 47µF 50V 20% SMT	SUN ELECT., 50CE47BS
4	5	C10, C11, C12, C13, C15	CAP., X5R, 1µF 50V, 10%, 0603	TAIYO YUDEN UMK107BJ105KA-T
5	1	C14	CAP., X5R 10µF 10V 20% 0805	TAIYO YUDEN LMK212ABJ106MG-T

6	1	C16	CAP., NPO 10nF 50V 5% 0805	NIC, NMC0805NPO103J50TRPF
7	3	C17, C18, C19	CAP., X5R 0.1µF 50V 10% 0805	TAIYO YUDEN UMK212BJ104KG-T
8	3	C20, C21, C22	CAP., X7R 0.047µF 50V, 10%, 0805	MURATA, GRM21BR71H473KA01L
9	3	D1, D2, D3	DIODE, TVS BI-DIRECTIONAL, 26V, 600W	DIODES/ZETEX SMBJ26CA-13-F
10	0	D7	ZENER DIODE, 5.1V SOD-123	OPT
11	8	D8-D12, D16, D17, D18	LED, GREEN, LED-ROHM-SML-01	ROHM, SML-012P8TT86
12	3	D13, D14, D15	DIODE, SCHOTTKY, SOD323	VISHAY SEMI., BAT42WS-E3-08
13	9	E1-E4, E6, E13-E16	TURRET, 0.094″	MILL-MAX 2501-2-00-80-00-00-07-0
14	6	E7, E8, E9, E10, E11, E12	TURRET, 0.063″	MILL-MAX 2308-2-00-80-00-00-07-0
15	3	JP1, JP2, JP3	HEADERS, SGL. ROW 3 PINS 2mm CTRS.	SAMTEC TMM-103-02-L-S
16	3	SHUNTS ON JP1-JP3 (1&2)	SHUNT, 2mm CTRS.	SAMTEC 2SN-BK-G
17	6	J1, J2, J3, J4, J5, J6	JACK, BANANA	KEYSTONE 575-4
18	3	Q1, Q2, Q3	MOSFET 2P-CH 40V 8A 8SO	VISHAY Si4909DY-T1-GE3
19	0	Q4, Q5, Q6, Q7, Q8, Q9	MOSFET P-CHAN., 40V, FDD4685, DPAK	OPT
20	1	Q10	XTOR N-CHAN., SOT23	DIODE INC., MMBTA42-7-F
21	1	Q11	XTOR N-CHAN., SOT23	DIODE INC., MMBT3904-7-F
22	1	R4	RES., CHIP 1.69M 0.125W 1% 0805	VISHAY, CRCW08051M69FKEA
23	3	R5, R8, R12	RES., CHIP 69.8k 0.125W 1% 0805	VISHAY, CRCW080569K8FKEA
24	3	R6, R9, R13	RES., CHIP 130k 0.125W 1% 0805	NIC, NRC10F1303TRF
25	1	R7	RES., CHIP 590k 0.125W 1% 0805	VISHAY, CRCW0805590KFKEA
26	1	R10	RES., CHIP 1.05M 0.125W 1% 0805	VISHAY, CRCW08051M05FKEA
27	1	R11	RES., CHIP 127k 0.1W 1% 0603	VISHAY, CRCW0603127KFKED
28	7	R14-R16, R20-R22, R29	RES., CHIP 1k 0.1W 5% 0603	VISHAY, CRCW06031K00JNEA
29	0	R17	RES., CHIP 845k 0.1W 1% 0603	OPT

30	0	R18	RES., CHIP 115k 0.06W 1% 0603	OPT
31	1	R19	RES., CHIP 30.9k 0.1W 1% 0603	VISHAY, CRCW060330K9FKEA
32	3	R23, R26, R28	RES., CHIP 249 0.1W 1% 0603	VISHAY, CRCW060249RFKEA
33	5	R30, R31, R32, R33, R36	RES., CHIP 100k 0.1W 5% 0603	NIC, NRC06J104TRF
34	1	R34	RES., CHIP 68k 0.25W 5% 1206	NIC, NRC12J683TRF
35	1	R35	RES., CHIP 240Ω 0.25W 1% 1206	VISHAY, CRCW1206240RFKEA
36	1	U1	I.C., POWERPATH CONTROLLER, QFN24UF-4×4	LINEAR TECH CORP. LTC4417CUF
37	3	U2,U3,U5	I.C., TRIPPLE 3-INPUT NOR GATE TSSOP14	NXP/PHILIPS SEMI. 74HC27 PW
38	1	U4	I.C., LOW DROPOUT REG. TSOT23-8	LINEAR TECH CORP. LT3060ETS8-5
39	4	MH1-MH4	STANDOFF, NYLON, 0.50, 1/2″	KEYSTONE, 8833 (SNAP ON)

SCHEMATIC DIAGRAM





ESD Caution

ESD (electrostatic discharge) sensitive device
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the “Evaluation Board”), you are agreeing to be bound by the terms and conditions set forth below (“Agreement”) unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you (“Customer”) and Analog Devices, Inc. (“ADI”), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose.

Furthermore, the license granted is expressly made subject to the following additional limitations:

Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term “Third Party” includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is

NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time.

LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED “AS IS” AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER’S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI’S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00).

EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

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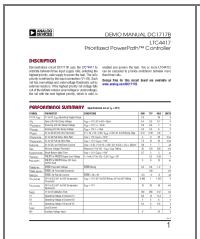
Documents / Resources

	ANALOG DEVICES LTC4417 Prioritized PowerPath Controller [pdf] User Guide LTC4417 Prioritized PowerPath Controller, LTC4417, Prioritized PowerPath Controller, PowerPath Controller, Controller

References

- Mixed-signal and digital signal processing ICs | Analog Devices
- DC1717B Evaluation Board | Analog Devices
- Mixed-signal and digital signal processing ICs | Analog Devices
- User Manual