ANALOG DEVICES EVAL-ADN4620 Evaluation Board Photographs User Guide

Contents hide

ANALOG DEVICES EVAL-ADN4620 Evaluation Board Photographs

FEATURES

- Isolated ground planes (logic side and bus side)
- High speed layout supports 2.5 Gigabit operation and precision jitter measurements (<1 ps rms for random jitter)
- Convenient connections through SMA terminals
- 1.8 V power on Side 1 (VDD1) and Side 2 (VDD2)
- 3.3 V power for LVDS receivers on Side 1 (VIO1) and Side 2 (VIO2, used with ADN4621 only)
- Ground on Side 1 (GND1) and ground on Side 2 (GND2)
- Side 1 LVDS signals: DIN1+, DIN1−, DIN2+ or DOUT2+, DIN2− or DOUT2−
- Side 2 LVDS signals: DOUT1+, DOUT1−, DOUT2+ or DIN2+, DOUT2− or DIN2−
- Jumper-selectable refresh mode
- Termination resistors on all LVDS receivers EVALUATION KIT CONTENTS
- EVAL-ADN4620EBZ or EVAL-ADN4621EBZ DOCUMENTS NEEDED
- ADN4620/ADN4621 data sheet
  EQUIPMENT NEEDED
- Signal generator
- Oscilloscope
- Power supply

GENERAL DESCRIPTION

The EVAL-ADN4620EBZ and EVAL-ADN4621EBZ allow quick and easy evaluation of the ADN4620/ADN4621 low voltage differential signaling (LVDS) isolators without the need for external compo-nents. The ADN4620/ADN4621 employ the Analog Devices, Inc., iCoupler® technology to combine a 2-channel isolator with LVDS receivers and drivers into a single, 20-lead SSOP package. The ADN4620/ADN4621 are capable of running at data rates of up to 2.5 Gbps with low jitter.
The EVAL-ADN4620EBZ/EVAL-ADN4621EBZ have separate ground and power planes for each side of the isolator, with indi-vidual 1.8 V power supplies required on each side of the ADN4620/ADN4621. This separation enables the evaluation of the ADN4620/ADN4621 with galvanic isolation between both sides of the devices. An additional power supply providing 3.3 V is required on Side 1 (and also Side 2 for the ADN4621).
For full details on the ADN4620/ADN4621, see the ADN4620/ADN4621 data sheet, which must be consulted in conjunction
PLEASE SEE THE LAST PAGE FOR AN IMPORTANT
WARNING AND LEGAL TERMS AND CONDITIONS. with this user guide when using the EVAL-ADN4620EBZ or EVAL-ADN4621EBZ.

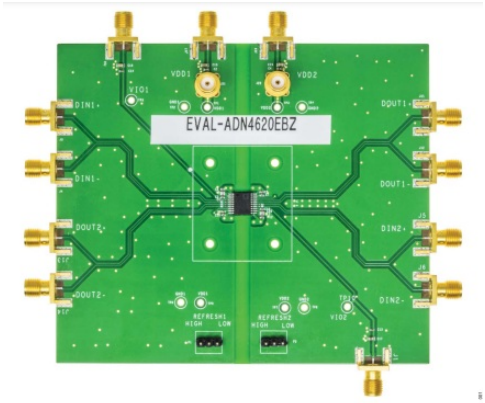

Figure 1. EVAL-ADN4620EBZ Photograph

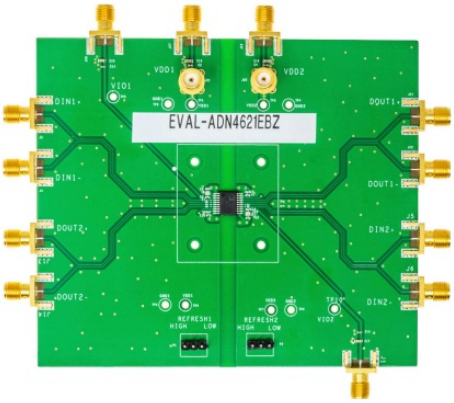

Figure 2. EVAL-ADN4621EBZ Photograph

EVALUATION BOARD PHOTOGRAPHS
EVALUATION BOARD CONFIGURATION

SETTING UP THE EVALUATION BOARD

On the EVAL-ADN4620EBZ or EVAL-ADN4621EBZ, connect a 3.3 V power supply to the J18 subminiature Version A (SMA) connector and connect 1.8 V power supplies to the J17 or J21 SMA connectors for Side 1 and the J19 or J22 SMA connectors for Side 2 (see Table 2). For the EVAL-ADN4621EBZ, also connect another 3.3 V power supply to the J1 SMA connector. At 1.25 GHz, with a load resistance of 100 Ω, the maximum operating current is 80 mA from each 1.8 V power supply, 14 mA from the 3.3 V supply on Side 1, and 7 mA from the 3.3 V supply on Side 2. VDD1 (Pin 1 and Pin 10 on the ADN4620/ADN4621) is bypassed to GND1 and VDD2 (Pin 11 and Pin 20 on the ADN4620/ADN4621) is bypassed to GND2. Similarly, VIO1 (Pin 3 on the ADN4620/ ADN4621) is bypassed to GND1 and VIO2 (Pin 13 on the ADN4621 only) is bypassed to GND2. Bypass capacitors of 0.1 µF are used in all cases. The ADN4620/ADN4621 integrates a refresh function to correct, if necessary, the output state in the absence of any input transitions. This function ensures the correct output state at power-up, for example. To reduce internal switching noise and provide even lower jitter, the refresh function can be disabled. This functionality is accessed on the EVAL-ADN4620EBZ or EVAL-ADN4621EBZ by changing the position of the P1 and P2 jumpers for Side 1 and Side 2, respectively, as described in Table 1.

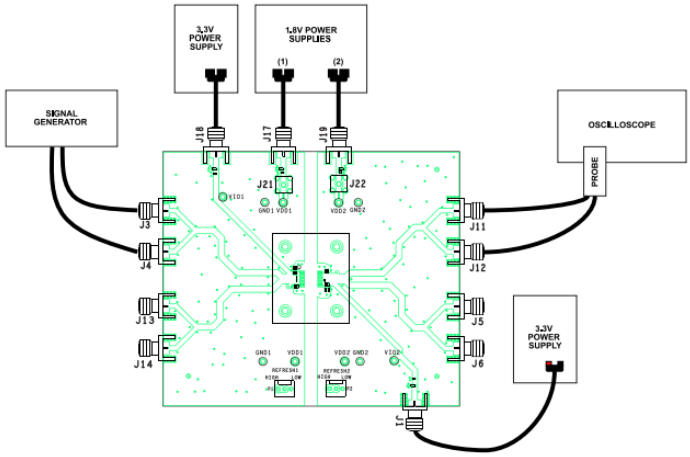

Figure 4. Basic LVDS Isolator Evaluation Board Operation for the EVAL-ADN4621EBZ

Figure 4 shows an example operation of the EVAL-ADN4621EBZ. The EVAL-ADN4620EBZ is set up similarly with the exception of no connection to J1. The SMA connectors reveal all LVDS inputs and outputs for the EVAL-ADN4620EBZ or EVAL-ADN4621EBZ (seeTo evaluate Channel 1 on the EVAL-ADN4620EBZ or EVAL-ADN4621EBZ, connect a signal generator to the evaluation board using the J3 connector and J4 connector and set up a 1.25 GHz square wave clock with an amplitude of 200 mV (400 mV peak-to-peak) and an offset of 1.2 V. Connect the oscilloscop to the J11 connector and J12 connector to perform timing measurements, including propagation delay, skew, and jitter. A differential probe with an SMA connector is recommended, terminating each output trace to 50 Ω connected to 1.24 V (providing 100 Ω differential termination and matching the ADN4620/ADN4621 driver offset voltage (VOS)). Refer to Table 3 for the connectors to use to evaluate Channel 2 on the EVAL-ADN4620EBZ or EVAL-ADN4621EBZ. Figure 3 shows a plot of the oscilloscope connected via the

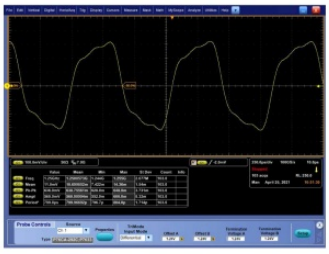

Figure 3. D_{OUT1-} and D_{OUT1+} with a 1.25 GHz Clock, Differential

J11 connector and J12 connector. The oscilloscope shows the differential voltage, that is, DOUT1+ − DOUT1−.

Table 1. Jumper Configuration for EVAL-ADN4620EBZ and EVAL-ADN4621EBZ

Side 1	
J17, J21 J18	Power supply, Side 1, connect 1.8 V to one connector option Input/output power supply, Side 1, connect 3.3 V
Side 2	
J19, J22	Power supply, Side 2, connect 1.8 V to one connector option
J1	Input/output power supply, Side 2, connect 3.3 V (leave open for EVAL-ADN4620EBZ)

Table 2. Power Supply Connector Descriptions for EVAL-ADN4620EBZ and EVAL-ADN4621EBZ

J3	D_{IN1+}, noninverted LVDS input for Channel 1
J4	D_{IN1-}, inverted LVDS input for Channel 1
J13	D_{IN2+}, noninverted LVDS input for Channel 2
J14	D_{IN2-}, inverted LVDS input for Channel 2
J11	D_{OUT1+}, noninverted LVDS output for Channel 1
J12	D_{OUT1-}, inverted LVDS output for Channel 1
J5	D_{OUT2+}, noninverted LVDS output for Channel 2
J6	D_{OUT2-}, inverted LVDS output for Channel 2

Table 3. Input and Output Connector Descriptions for EVAL-ADN4620EBZ

J3	D_{IN1+}, noninverted LVDS input for Channel 1
J4	D_{IN1-}, inverted LVDS input for Channel 1
J13	D_{IN2+}, noninverted LVDS input for Channel 2
J14	D_{IN2-}, inverted LVDS input for Channel 2
J11	D_{OUT1+}, noninverted LVDS output for Channel 1
J12	D_{OUT1-}, inverted LVDS output for Channel 1
J5	D_{OUT2+}, noninverted LVDS output for Channel 2
J6	D_{OUT2-}, inverted LVDS output for Channel 2

Table 4. Input and Output Connector Descriptions for EVAL-ADN4621EBZ

J3	D_{IN1+}, noninverted LVDS input for Channel 1
J4	D_{IN1-}, inverted LVDS input for Channel 1
J13	D_{OUT2+}, noninverted LVDS output for Channel 2
J14	D_{OUT2-}, inverted LVDS output for Channel 2
J11	D_{OUT1+}, noninverted LVDS output for Channel 1
J12	D_{OUT1-}, inverted LVDS output for Channel 1
J5	D_{IN2+}, noninverted LVDS input for Channel 2
J6	D_{IN2-}, inverted LVDS input for Channel 2

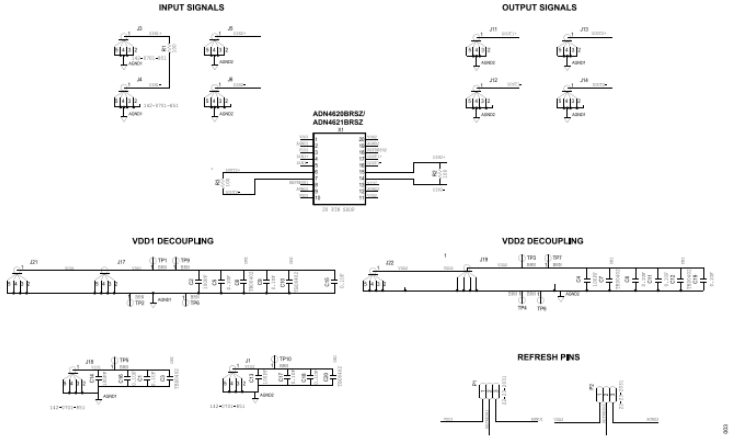

Figure 5. EVAL-ADN4620EBZ and EVAL-ADN4621EBZ Schematic

EVALUATION BOARD SCHEMATICS AND ARTWORK

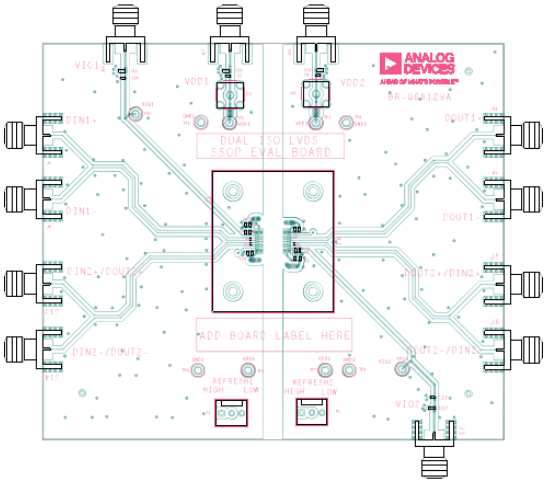

Figure 6. EVAL-ADN4620EBZ or EVAL-ADN4621EBZ Component Side and Silkscreen

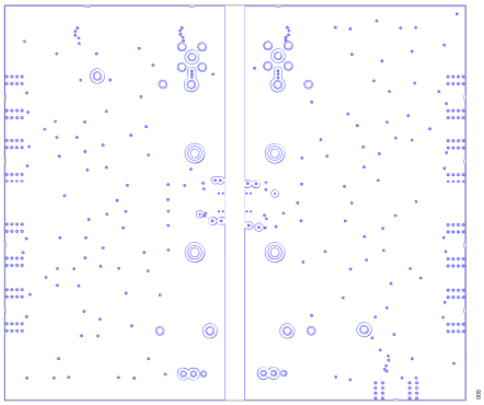

Figure 7. EVAL-ADN4620EBZ or EVAL-ADN4621EBZ Inner Layer 2, Ground

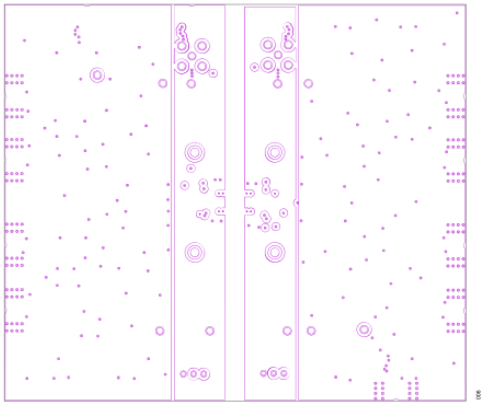

Figure 8. EVAL-ADN4620EBZ or EVAL-ADN4621EBZ Inner Layer 3, Power

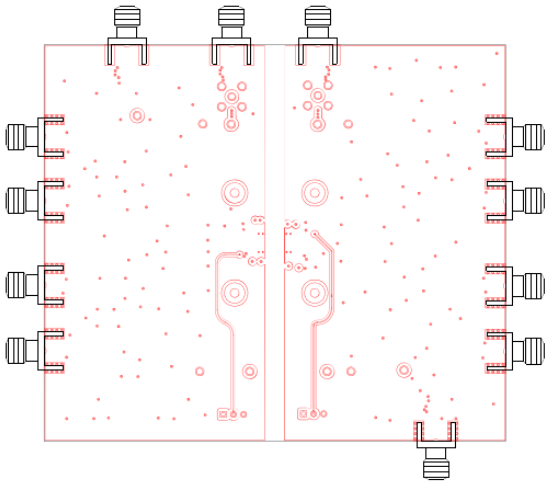

Figure 9. EVAL-ADN4620EBZ or EVAL-ADN4621EBZ Solder Side

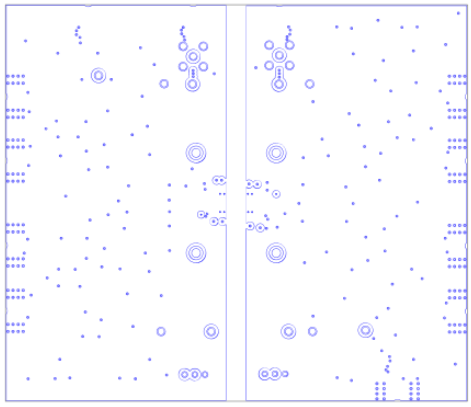

Figure 7. EVAL-ADN4620EBZ or EVAL-ADN4621EBZ Inner Layer 2, Ground

ORDERING INFORMATION

BILL OF MATERIALS

Table 5. EVAL-ADN4620EBZ Bill of Materials

Quantity	Reference Designator	Description	Manufacturer	Part Number

5	C1, C5, C8, C9, C11	Capacitors, 0.1 µF, 0402	Kemet	C0402C104K4RACTU
3	C2, C4, C14	Capacitors, 100 pF, 0402	Murata	GRM1555C1H101JA01D
8	C3, C6, C7, C10, C12, C13, C18, C20	Capacitors, 0402	Not fitted	Not applicable
3	C15, C16, C19	Capacitors, 0.1 µF, 0603	AVX	06035C104KAT2A
1	C17	Capacitor, 0603	Not fitted	Not applicable
1	J1	Connector, SMA, edge	Not fitted	Not applicable
11	J3 to J6, J11 to J14, J17 to J19	Connectors, SMA, edge	Johnson – Cinch	142-0701-851
2	J21, J22	Connectors, SMA	Pasternack Enterprises	PE4117
2	P1, P2	3-pin, header (and jumper)	Molex (and Sullins)	22-23-2031 (and QPC02SXGN-RC)
2	R1, R3	Resistors, 100 Ω, 0201	Panasonic	ERJ-1GNF1000C
1	R2	Resistor, 0201	Not fitted	Not applicable
9	TP1 to TP9	Test points	Components Corporation	TP104-01-01
1	TP10	Test point	Not fitted	Not applicable
1	X1	**ADN4620** 3.75 kV rms, dual-channel LVDS, 2.5 Gigabit isolator	Analog Devices	**ADN4620BRSZ**

Table 6. EVAL-ADN4621EBZ Bill of Materials

6	C1, C5, C8, C9, C11, C18	Capacitors, 0.1 µF, 0402	Kemet	C0402C104K4RACTU
4	C2, C4, C13, C14	Capacitors, 100 pF, 0402	Murata	GRM1555C1H101JA01D
6	C3, C6, C7, C10, C12, C20	Capacitors, 0402	Not fitted	Not applicable
4	C15, C16, C17, C19	Capacitors, 0.1 µF, 0603	AVX	06035C104KAT2A
12	J1, J3 to J6, J11 to J14, J17 to J19	Connectors, SMA, edge	Johnson – Cinch	142-0701-851
2	J21, J22	Connectors, SMA	Pasternack Enterprises	PE4117
2	P1, P2	3-pin, header (and jumper)	Molex (and Sullins)	22-23-2031 (and QPC02SXGN-RC)
2	R1, R2	Resistors, 100 Ω, 0201	Panasonic	ERJ-1GNF1000C
1	R3	Resistor, 0201	Not fitted	Not applicable
10	TP1 to TP10	Test points	Components Corporation	TP104-01-01
1	X1	**ADN4621** 3.75 kV rms, dual-channel LVDS 2.5 Gigabit isolator	Analog Devices	**ADN4621BRSZ**

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the “Evaluation Board”), you are agreeing to be bound by the terms and conditions set forth below (“Agreement”) unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you (“Customer”) and Analog Devices, Inc. (“ADI”), with its principal place of business at Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal,temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term “Third Party” includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED “AS IS” AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER’S POSSESSION

OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement
shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

One Analog Way, Wilmington, MA 01887-2356, U.S.A.

Documents / Resources

ANALOG DEVICES EVAL-ADN4620 Evaluation Board Photographs [pdf] User Guide
EVAL-ADN4620, EVAL-ADN4621, Evaluation Board Photographs, Evaluation Board, EVAL-ADN4620, Board

References

- **Mixed-signal and digital signal processing ICs | Analog Devices**
- **EVAL-ADN4620 Evaluation Board | Analog Devices**
- **EVAL-ADN4621 Evaluation Board | Analog Devices**
- **ADN4620 Datasheet and Product Info | Analog Devices**
- **ADN4621 Datasheet and Product Info | Analog Devices**