


ANALOG DEVICES ADRF5142 Product Evaluation Boards and Kits User Guide

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User Guide | EVAL-ADRF5142

UG-2215

Evaluating the ADRF5142 High Power, 40 W Peak,
Silicon SPDT Switch, 8GHz to 11 GHz

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FEATURES

- Full-featured evaluation board for the ADRF5142
- Easy connection to the test equipment
- Through line for calibration

EQUIPMENT NEEDED

- DC power supplies
- Network analyzer

GENERAL DESCRIPTION

The ADRF5142 is a single-pole, double-throw (SPDT) switch manufactured in the silicon process. This user guide describes the ADRF5142-EVALZ evaluation board, designed to evaluate the features and performance of the ADRF5142. The evaluation board is shown in Figure 1. The ADRF5142 data sheet provides its full specifications. Refer to the ADRF5142 data sheet in conjunction with this user guide when using the ADRF5142-EVALZ.

ADRF5142-EVALZ EVALUATION BOARD PHOTOGRAPH

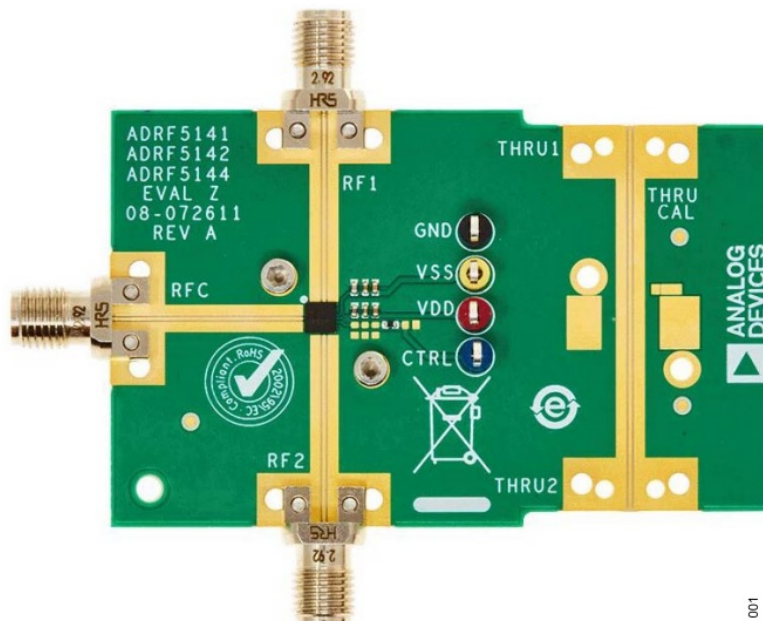


Figure 1. Evaluation Board Photograph

PLEASE SEE THE LAST PAGE FOR AN IMPORTANT WARNING AND LEGAL TERMS AND CONDITIONS.

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5142-EVALZ is a board fitted with connectors, assembled with the ADRF5142 and its application circuitry. All components are placed on the primary side of the ADRF5142-EVALZ. An assembly drawing for the ADRF5142-EVALZ is shown in Figure 6, and an evaluation board schematic is shown in Figure 5.

BOARD LAYOUT

The ADRF5142-EVALZ is designed using RF circuit design techniques on an 8-layer printed circuit board (PCB). The PCB stackup is shown in Figure 2.

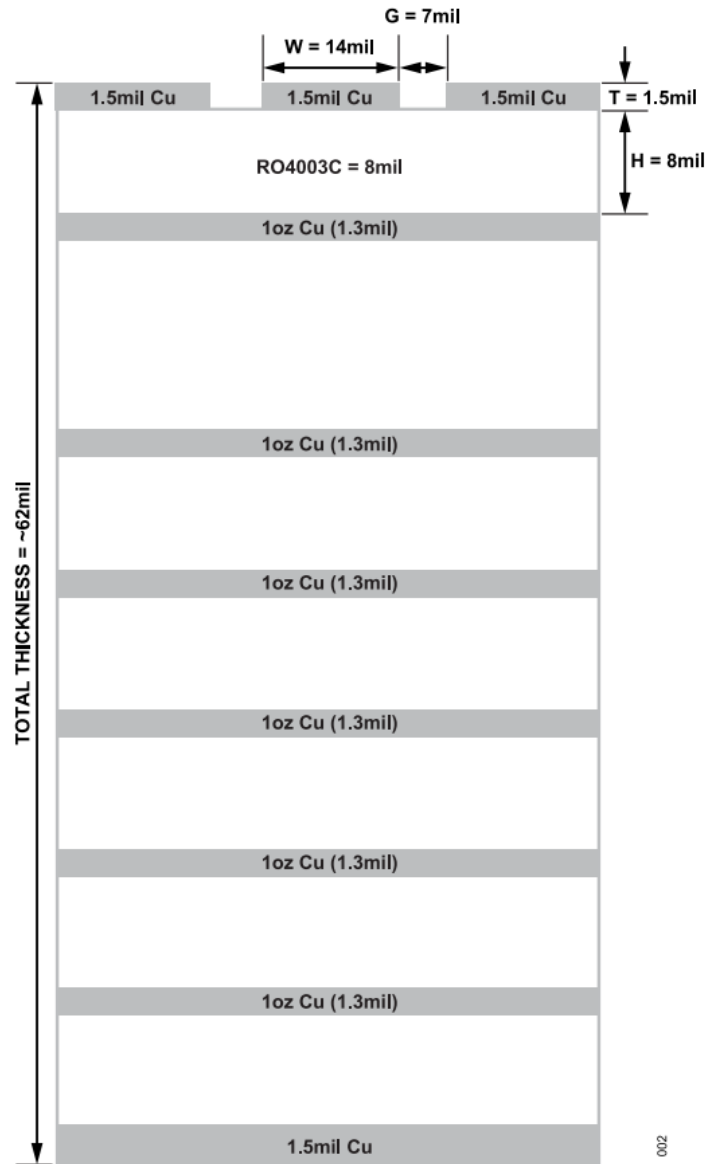


Figure 2. Evaluation Board Stackup

The outer copper layers are 1.5 mil thick, and the inner layers are 1.3 mil thick.

The top dielectric material is 8 mil Rogers 4003C, which provides 50 Ω controlled impedance and optimizes the high-frequency performance. All RF traces are routed on the top layer, and the second layer is used as the ground plane for RF transmission lines. The remaining six layers are also ground planes filled with FR4 material to manage the thermal rise during high-power operations, and are supported with dense and filled vias to the PCB bottom for thermal relief. The overall board thickness is approximately 62 mil for mechanical strength.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 14 mil and ground spacing of 7 mil to have a 50 Ω characteristic impedance. Ground via fences are arranged on both sides of a CPWG to improve isolation between nearby RF lines and other signal lines.

The exposed ground pad of the ADRF5142, which is soldered on the PCB ground pad, is the main thermal conduit for heat dissipation. The PCB ground pad is densely populated with filled, through vias to provide the lowest possible thermal resistance path from the top to the bottom of the PCB. The connections from the package ground lead to ground are kept as short as possible.

POWER-SUPPLY AND CONTROL INPUTS

The ADRF5142-EVALZ has two power-supply inputs, one control input, and a ground, as shown in Table 1. The DC test points are populated on VDD, VSS, CTRL, and GND pins. A 3.3 V supply is connected to the DC test points on VDD, and a -3.3 V supply is connected to the DC test points on VSS. Ground reference can be connected to GND. Connect the control input, CTRL, to 3.3 V or 0 V. The typical total current consumption for the ADRF5142 is 630 μ A.

The VDD supply pin of the ADRF5142 are decoupled with 100 pF and 100 nF capacitors, while the VSS supply pin and the CTRL control pin are decoupled with a 100 pF capacitor.

Table 1. Power-Supply and Control Inputs

Test Points	Description
VDD	Positive supply voltage
VSS	Negative supply voltage
CTRL	Control Input
GND	Ground

RF INPUTS AND OUTPUTS

The ADRF5142-EVALZ has five edge-mounted, 2.92 mm connectors for the RF inputs and outputs, as shown in Table 2.

Table 2. RF Inputs and Outputs

2.92 mm Connectors	Description
RFC	RF common port
RF1	RF Throw Port 1
RF2	RF Throw Port 2
THRU1	Through-line input and output
THRU2	Through-line input and output

The through calibration line, which connects the THRU1 and THRU2 RF connectors, calibrates out the board loss effects from the measurements of the ADRF5142-EVALZ to determine the device performance at the pins of the IC. Figure 3 shows the typical board loss for the ADRF5142-EVALZ at room temperature, as well as the embedded and deembedded insertion loss for the ADRF5142.

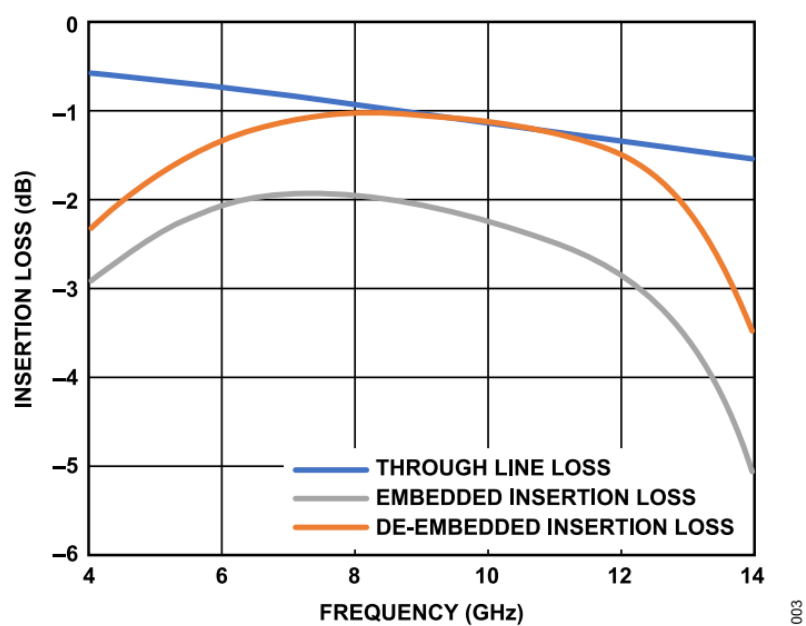


Figure 3. Insertion Loss vs. Frequency

TEST PROCEDURE

BIASING SEQUENCE

To bias up the ADRF5142-EVALZ, perform the following steps:

1. Ground the GND test point.
2. Bias up the VDD test point.
3. Bias up the VSS test point.
4. Bias up the CTRL test point.
5. Apply an RF input signal.

The ADRF5142-EVALZ is shipped fully assembled and tested. Figure 4 provides a basic test setup diagram to evaluate the s-parameters using a network analyzer. Perform the following steps to complete the test setup and verify the operation of the ADRF5142EVALZ:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the VDD test point to the voltage-output terminal of the 3.3 V supply.
3. Connect the VSS test point to the voltage-output terminal of the –3.3 V supply.
4. Connect the CTRL test point to the voltage-output terminal of the 3.3 V supply. The ADRF5142 can be configured in different modes by connecting the CTRL test point to 3.3 V or 0 V, as shown in Table 3.
5. Connect a calibrated network analyzer to the RFC, RF1, and RF2 2.92 mm connectors. If network analyzer port count is not enough, terminate unused RF ports with 50 Ω . Sweep the frequency from 4 GHz to 14 GHz and set the power to –10 dBm.

Additional test equipment is needed to fully evaluate the device functions and performance.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high-isolation power combiner is also recommended.

For power compression and power handling evaluations, use a 2channel power meter and a signal generator. A high enough power amplifier is also recommended at the input. Test accessories, such as couplers and attenuators, must have enough power handling.

The ADRF5142-EVALZ comes with a support plate attached to the bottom side. To ensure maximum heat dissipation and to reduce thermal rise on the board during high power evaluations, this support plate must be attached to a heatsink using thermal grease.

Note that the measurements performed at the 2.92 mm connectors of the ADRF5142-EVALZ include the losses of the 2.92 mm connectors and the PCB. The through line must be measured to calibrate out the effects on the ADRF5142-EVALZ. The through line is the summation of an RF input and output lines that are connected to the device and equal in length.

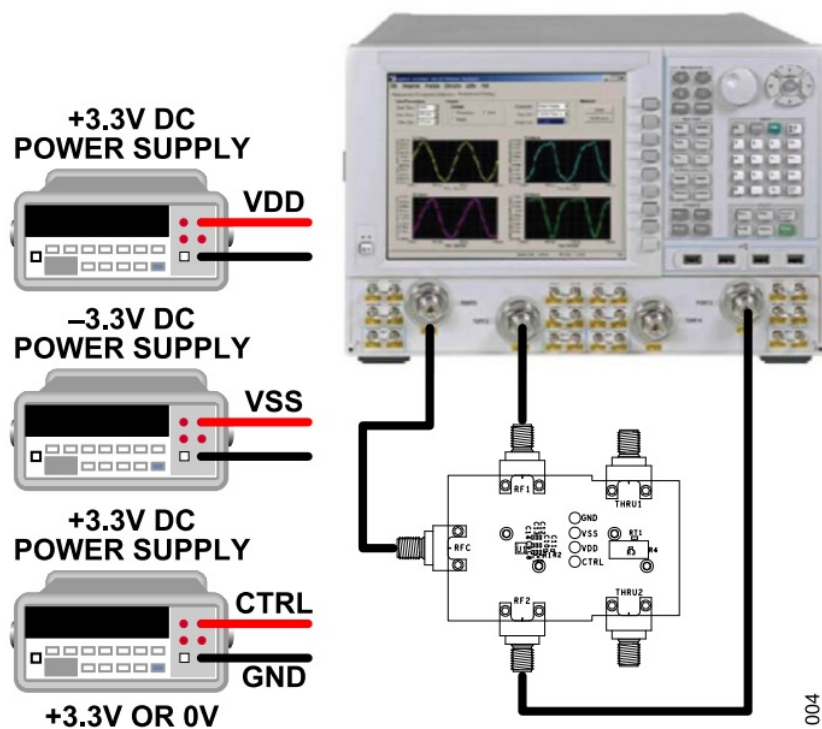


Figure 4. Test Setup Diagram

Table 3. Control Voltage Truth Table

Digital Control Input, V CTRL	RF Paths	
	RF1 to RFC	RF2 to RFC
Low	Insertion loss (on)	Isolation (off)
High	Isolation (off)	Insertion loss (on)

EVALUATION BOARD SCHEMATIC AND ASSEMBLY DIAGRAM

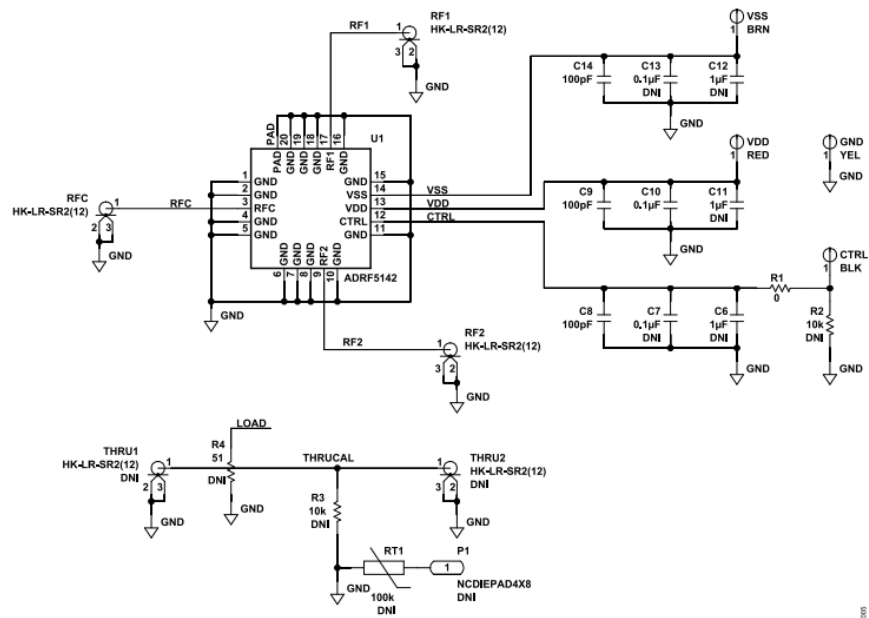


Figure 5. ADRF5142-EVALZ Evaluation Board Schematic

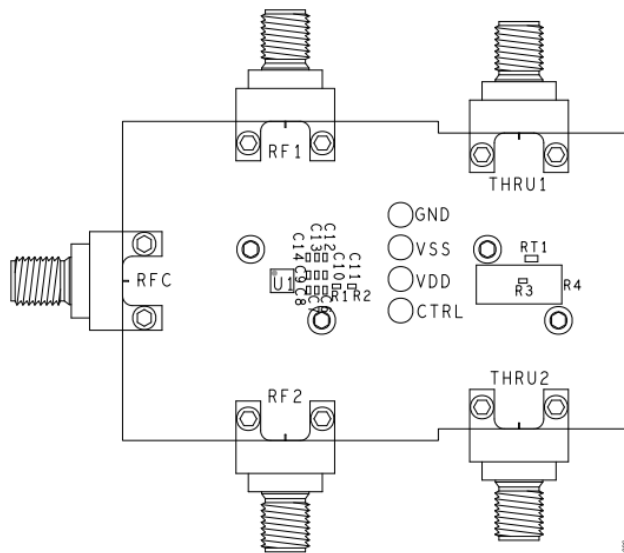


Figure 6. ADRF5142-EVALZ Evaluation Board Assembly Diagram

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. Bill of Materials for ADRF5142-EVALZ

Quantity	Reference Designator	Description	Manufacturer	Part Number
3	C8. C9. C14	Capacitors, 100 pF, 50 V. C0402 package	Murata	GCM1555C1H101JA16D
1	10	Capacitor, 0.1 pF. 50 V. C0402 package	Murata	GCM155R71H104KE02D
1	R1	Resistor, 0 Ω. 0.1 W. 0402 package	Panasonic	ERJ-2GEOROOX
3	RFC. RF1. RF2	Edge mount 2.92 mm connectors	Hirose Electric Co.	HK-LR-SR2(12)
4	GND, CTRL. VDD, and VSS	Surface-mount test points	Components Corporation	TP-104-01-xx
1	U1	40 W peak, silicon SPDT switch, 8 GHz to 11 GHz	Analog Devices, Inc.	ADRF5142BCCZN
1	PCB	ADRF5142-EVALZ	Analog Devices	BR-072611



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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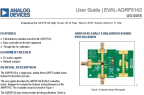
REVISION HISTORY

4/2024—Revision 0: Initial Version



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References

- [User Manual](#)

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