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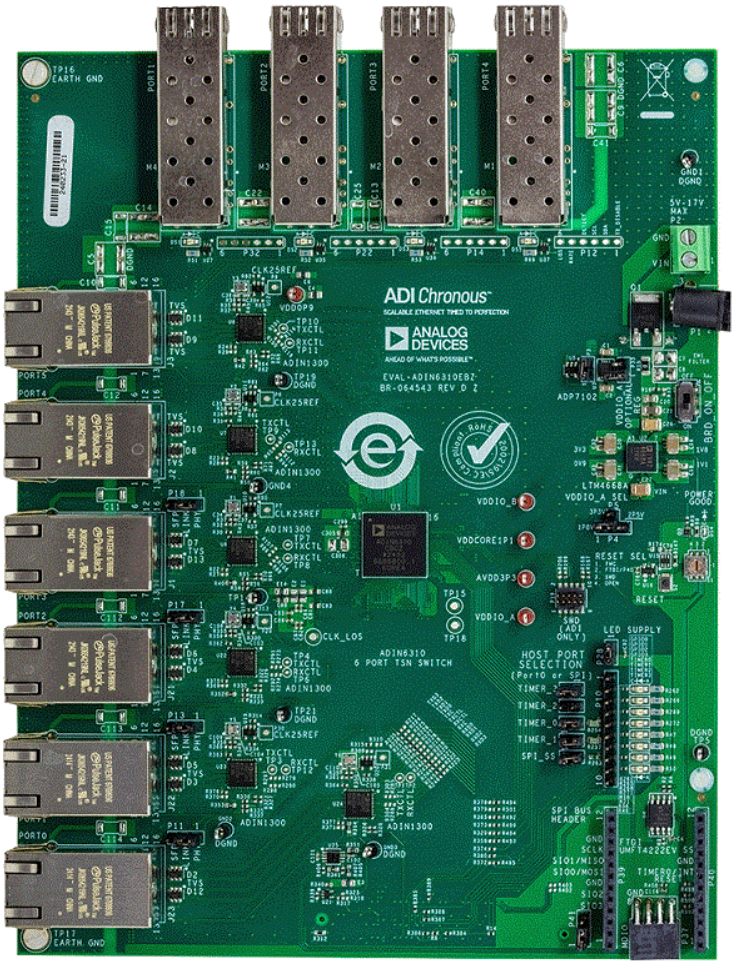
ANALOG DEVICES ADIN6310 Field Switch Reference Design



Product Specifications

- 6-port Ethernet switch ADIN6310
- 2 Gb trunk ports: SGMII by SMA or ADIN1300 by RGMII
- 4 spur 10BASE-T1L ports: ADIN1100 by RGMII
- IEEE 802.3cg-compliant SPoE PSE controller: LTC4296-1
- Power Class 12
- Zephyr open source software project
- Unmanaged mode with a basic switch and PSE power
- VLAN IDs 1-10 enabled on all ports
- Power coupled to 10BASE-T1L cable for all spur ports
- DIP switch options to enable other features (Time Sync, LLDP, IGMP Snooping)
- Managed mode using the switch evaluation package TSN/Redundancy evaluations
- Time-sensitive networking (TSN) capable
- Scheduled traffic (IEEE 802.1Qbv)
- Frame preemption (IEEE 802.1Qbu)
- Per stream filtering and policing (IEEE 802.1Qci)
- Frame replication and elimination for reliability (IEEE 802.1CB)

- IEEE 802.1AS 2020 time synchronisation
- Redundancy capabilities

Product Usage Instructions

Equipment Needed

- ADIN6310 data sheet and UG-2280 and UG-2287 user guides
- ADIN1100 data sheet
- ADIN1300 data sheet
- LTC4296-1 data sheet
- MAX32690 data sheet

Software Needed

- For TSN evaluation, install the ADIN6310 evaluation package
- Npcap packet capture

General Description

- For extensive switch evaluation, refer to the TSN switch evaluation package available from the ADIN6310 product page.

FEATURES

- 6-port Ethernet switch ADIN6310
  - 2Gb trunk ports; SGMII by SMA or ADIN1300 by RGMII
  - 4 spur 10BASE-T1L ports, ADIN1100 by RGMII
- IEEE 802.3cg-compliant SPoE PSE controller, LTC4296-1
  - Power Class 12
  - Power classification by SCCP (not enabled)
- Arm® Cortex®-M4 microcontroller, MAX32690
  - External flash and RAM
- Zephyr open source software project
  - Unmanaged mode with basic switch and PSE power
  - VLAN IDs 1-10 enabled on all ports

    - Power coupled to 10BASE-T1L cable for all spur ports
    - DIP switch options to enable other features (Time Sync, LLDP, IGMP Snooping)
- Managed mode using the switch evaluation package, TSN/Redundancy evaluations
    - Time-sensitive networking (TSN) capable
    - Scheduled traffic (IEEE 802.1Qbv)
    - Frame preemption (IEEE 802.1Qbu)
    - Per stream filtering and policing (IEEE 802.1Qci)
    - Frame replication and elimination for reliability (IEEE 802.1CB)
- IEEE 802.1AS 2020 time synchronisation
    - Redundancy capabilities
    - High availability seamless redundancy (HSR)
    - Parallel redundancy protocol (PRP)
    - Media redundancy protocol (MRP)
- Host interface hardware strapping with jumpers, a choice of
    - Single/Dual/Quad SPI interface
    - 10Mbps/100Mbps/1000Mbps Ethernet port (Port 2/Port 3)
    - SGMII/100BASE-FX/1000BASE-KX
    - Header for direct SPI access (Single/Dual/Quad)
- Scale port count by cascading by RJ45 or SGMII/1000BASE-KX/ 100BASE-FX
- PHY strapping by surface-mount configuration resistors
    - The default state is software power down for spur Ports
- Switch firmware manages PHY operation over MDIO
    - Operates from a single, external 9V to 30V supply
    - LED indicators on GPIO, TIMER pins

EVALUATION KIT CONTENTS

- EVAL-ADIN6310T1LEBZ evaluation board
- 15V, 18W wall adapter with international adapters
- 5 x plug-in screw terminal connectors for 10BASE-T1L cable and external power supply
- 1x Cat5e Ethernet cable

EQUIPMENT NEEDED

- Link partner with 10BASE-T1L interface
- Link partner with standard Ethernet interface
- Single pair cabling for T1L
- PC running Windows® 11

DOCUMENTS NEEDED

- ADIN6310 data sheet and UG-2280 and UG-2287 user guides
- ADIN1100 data sheet
- ADIN1300 data sheet
- LTC4296-1 data sheet
- MAX32690 data sheet

SOFTWARE NEEDED

- For TSN evaluation, install the ADIN6310 evaluation package

GENERAL DESCRIPTION

- This user guide describes the ADIN6310 Field switch evaluation board with support for four 10BASE-T1L spur ports and two standard Gigabit capable Ethernet trunk ports.
- The hardware includes single-pair power over Ethernet (SPoE) LTC4296-1 circuit with optional serial communication classification protocol (SCCP) support.
- The default operation of the hardware is an unmanaged mode where the MAX32690 Arm Cortex-M4 microcontroller configures the switch into a basic switching mode and the PSE is configured for Class 12 operation.
- Enhance the unmanaged switch operation by the DIP switch (S4), which provides the ability to enable features such as time synchronisation, LLDP, or IGMP snooping by default.
- Disable the PSE by using the DIP switch; default is enabled. For more extensive switch evaluation, refer to the TSN switch evaluation package available from the ADIN6310 product page.
- This evaluation package provides ability to exercise the TSN functionality in addition to the Redundancy features.

- Figure 1 shows an overview of the evaluation board.

HARDWARE OVERVIEW

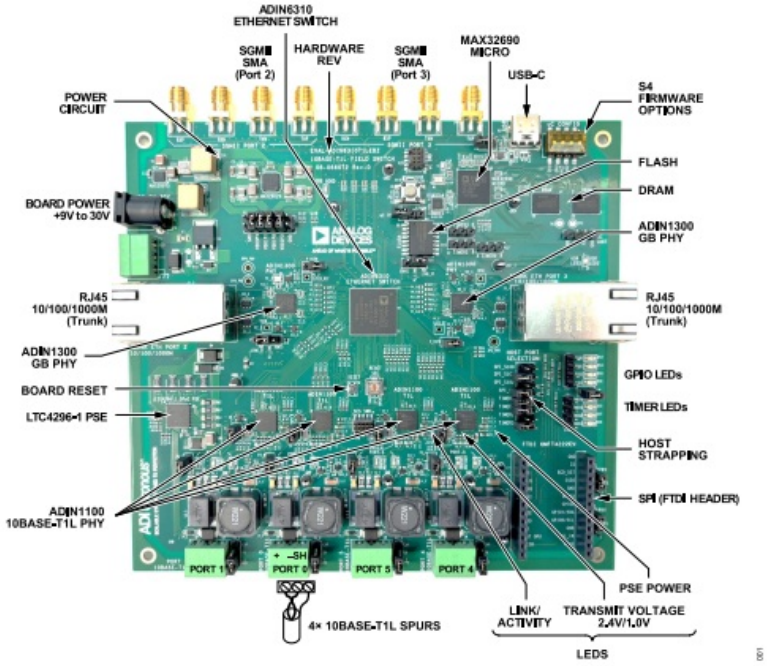


Figure 1. Detailed Overview of the Evaluation Hardware

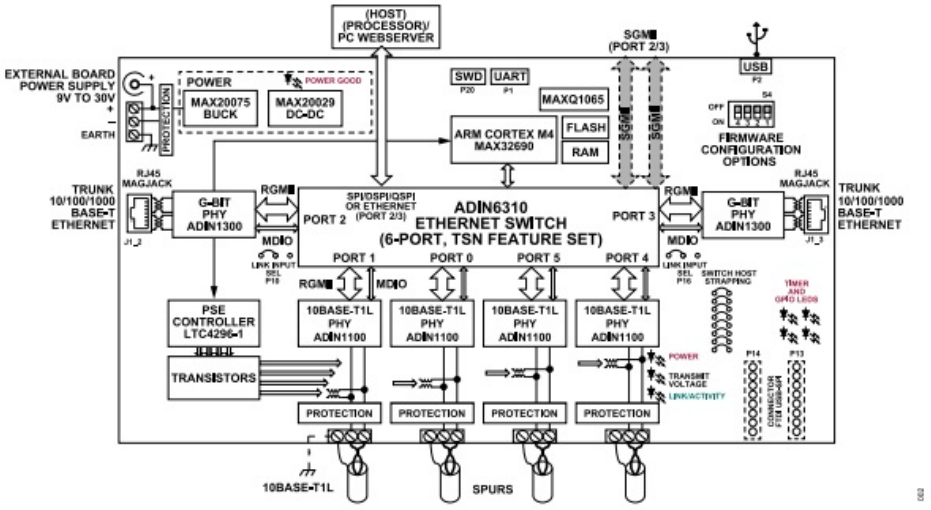


Figure 2. Block Diagram Overview

EVALUATION BOARD HARDWARE

POWER SUPPLIES

- The hardware operates from a single, external, 9V to 30V supply rail. A 15V wall adapter is supplied as part of the kit.
- Apply the wall adapter to P4 connector or 9V to 30V to the P4 connector. Alternatively, it is possible to supply power to the 3-pin connector, P3.
- The LED DS1 lights up when power is applied to the board, indicating a successful

power-up of the main power rails.

- All power rails are provided by an on-board MAX20075 buck regu-lator and MAX20029 DC-DC converter.
- These devices generate the four rails (3.3V, 1.8V, 1.1V, and 0.9V) required for operation of the ADIN6310 switch, ADIN1100 and ADIN1300 PHYs, MAX32690 and associated circuitry.
- The default nominal voltages are listed in Table 1, in addition to which rails are used for the different devices.
- The LTC4296-1 is powered directly from the incoming supply on P3 or P4. By default, the PSE is configured to enable four ports with IEEE802.3 Class 12 operation.
- If using the PSE with SCCP, increase the supply rail to the evaluation board to 20V minimum.
- Alternatively, power the board using the USB connector P2 to provide +5V power with P8 jumper inserted. As the PSE operates from a minimum of +6V, the USB connector must not be used if PSE operation is required.

Table 1. Default Device Power Supply Configuration

Rail	OUTS4	OUTS3	OUTS2	OUTS1
Nominal Voltage	3.3V	1.8V	1.1V	0.9V
ADIN6310 Switch	VDD3P3	VDDIO_A/B	VDDCORE	N/A[1]
ADIN1300 PHY	AVDD3P3	VDDIO	N/A[1]	VDD0P9
ADIN1100 PHY	AVDD_H	AVDD_L	DVDD_1P1	N/A[1]
MAX32690	VDDIOH, VDD3A, VDDB	VDDIO, VDDA	VCORE	N/A[1]
Flash	VCC	N/A[1]	N/A[1]	N/A[1]
RAM	N/A[1]	VCC, VCCQ	N/A[1]	N/A[1]
MAXQ1065	VDD	N/A[1]	N/A[1]	N/A[1]

1 N/A means not applicable.

Connector P5 provides probe access to the individual power supplies and, when inserted, connects the supply rails to the circuit. P5 must have links inserted across VDD3P3 (3-4), VDD1P8 (5-6), VDD1P1 (7-8) and VDD0P9 (9-10).

- Table 2 shows an overview of the current consumption for the switch and PHYs for various operating modes. The MAX32690 is held in reset for these measurements; the LTC4296-1 is not enabled.

Table 2. Managed Mode Board Quiescent Current (TSN Evaluation Application)

Board Configuration (P3/P4 = 15V)	Typical Quiescent Current
On Power-Up	38mA

Table 2. Managed Mode Board Quiescent Current (TSN Evaluation Application) (Continued)

Board Configuration (P3/P4 = 15V)	Typical Quiescent Current
In Hardware Power-Down (RESET_N Held Low)	25mA
+Port 2Gb Ethernet Link	69mA
+1 T1L Port	72mA
+Port 3Gb Ethernet Link	94mA
4 x T1L + 2Gb Ports	101mA

Table 3 shows a summary of the current consumption of the board for the unmanaged operation where MAX32690 enables the switch and the PSE provides power to the end device over the single pair.

Table 3. Unmanaged Mode Board Quiescent Current (MAX32690 Configures)

Board Configuration (P3/P4 = 15V)	Typical Quiescent Current[1]
On Power-Up	57mA
+Port 2Gb Ethernet Link	79mA
+Port 3Gb Ethernet Link	100mA
+1 T1L Port[2]	127mA[3]

1. S4 DIP switch is in default configuration (all OFF) for basic switch configuration and PSE providing power.
2. DEMO-ADIN1100D2Z board.
3. PSE port supplies power to the board, and the power depends on the hardware.

POWER SEQUENCING

- There are no special power sequencing requirements for the devices. The evaluation board is configured to bring up the power rails together.

EVALUATION BOARD MODES OF OPERATION

- There are three general modes to use the hardware. The first mode is the default operation, which is unmanaged mode. In this mode, the MAX32690 microcontroller configures the ADIN6310 switch and the LTC4296-1, both over SPI interface.
- The second mode is for TSN evaluation. In this mode, the ADI TSN evaluation application is used to interface to the switch over an Ethernet-connected Host interface through Port 2.
- The TSN evaluation package provides a PC based web server and allows users to interact with all the TSN and Redundancy features of the switch.
- The TSN evaluation package does not support configuration of the PSE. In this use case, use the other ports on the board to evaluate the capability of the ADIN6310, establish links with other link partners and evaluate TSN capability and 10BASE-T1L.
- For more details on this mode, see the Managed Configuration and TSN section.
- The third operating mode involves user own Host connected to the switch SPI interface through P13/P14 header and user porting the switch driver to their platform.

BOARD RESET

- The push button S3 provides user the ability to reset the ADIN6310 and optionally the MAX32690. P9 must be inserted in position (1-2), for the reset button to also reset the MAX32690.
- Pushing the reset button does not reset the 10BASE-T1L PHYs or the Gigabit PHYs directly, but the subsequent initialisation of the switch causes the PHYs to reset.

JUMPER AND SWITCH OPTIONS

ADIN6310 Host Port Strapping

- The ADIN6310 switch supports the Host control over SPI or any of the six Ethernet

ports. Configure the Host interface to be Port 2, Port 3, or SPI.

- The Host port and Host port interface selection are configured using jumpers inserted in the P7 header on the
- nets labelled TIMER0/1/2/3, SPI_SIO, and SPI_SS.
- The Timer and SPI pins have internal pull-up/-down resistors, as shown in Table 4. The strapping jumpers on the evaluation board provide user with the ability to reconfigure the strapping to select an alternative Host interface.
- For more details on all options available, refer to the section on Host strapping in the ADIN6310 data sheet. Overcome the internal pull-up/-down strapping resistors with the external resistor by inserting the strapping jumper.
- With no strapping links inserted, the Host interface is configured for standard SPI. This is also the default configuration for the hardware when shipped. Changes to Host strapping require a power cycle to take effect.

Table 4. Host Strapping Interface Selection

	Host Strapping Jumpers				
Host Port	**TIMER_3**	**TIMER_2**	**TIMER_1**	**TIMER_0**	**SPI_SS**
Internal PU/PD[1]	PD	PD	PU	PU	PU
SPI (Single) DEFAULT[2]	Open	Open	Open	Open	Open
SPI (Quad)	Open	Insert	Open	Open	Open
RGMII 1Gb[3]	Insert	Open	Insert	Insert	Insert

1. PU = Pull-Up, PD = Pull-Down.
2. MAX32690 is configured for a single SPI interface. 3 Use with the TSN evaluation application.

Table 5. Host Port Selection

Host Port	SPI_SIO2	SPI_SIO1	SPI_SIO0
Port 2[1]	Open	Insert	Open
Port 3	Open	Insert	Insert

Use with the TSN evaluation application.

Several jumpers on the evaluation board must be set for the required operating setup before using the board for evaluation. The default settings and functions of these jumper options are shown in Table 6.

Link	Position	Function
S1	3-4	Reset switch selection. Default open (other positions for internal debug only).
P1	Open	UART Interface for the MAX32690.
P2_x	Insert 2-3	10BASE-T1L shield circuit. Connect the shield of the cable to the Earth node either directly or by a capacitor.
P5	Insert 3-4 Insert 5-6 Insert 7-8 Insert 9-10	Jumpers to connect DC-DC converter to circuit and provide connectivity to supplies.
P7	Open	Host strapping header, used to tell ADIN6310 switch what interface and port the Host resides. All connections open selects standard SPI as Host interface.
P8	Open	Not used.
P9	Open	Reset header for the MAX32690. When open MAX32690 enabled.
P10	Insert 2-3	Switch Port 2 link information from ADIN1300 PHY (2-3) or pulled to ground (1-2) when Port 2 configured for SGMII mode. Default: P2_LINK = PHY Link Status.
P16	Insert 2-3	Switch Port 3 Link information from ADIN1300 PHY (2-3) or pulled to ground (1-2) when Port 3 configured for SGMII mode. Default: P3_LINK = PHY Link Status.
P11	Open	Reset for PHY Port 2.
P12	Inserted	Reset for PHY Port 3.
P15	Insert 1-2	Optional if using FTDI dongle connected to P13/P14. Supply selection for SPI, choice of 1.8V or 3.3V. Default 1.8V.
P17	Open	Header for the ADIN6310 GPIO signals.
P18	Open	Header for the ADIN6310 Timer signals.
P19	Insert	Connects power to the ADIN6310 LED circuit for the Timer/GPIO pins.
P21	Insert 1-2	Supply selection for I^2C, (not used).
P22	Open	ADIN6310 Timer1 to the MAX32690 (not used).
P23	Open	ADIN6310 Timer2 to the MAX32690 (not used).
P24	Open	ADIN6310 Timer3 to the MAX32690 (not used).
S4	OFF	DIP Switch, all switch positions OFF. Switch positions provide different operation options.

ADIN1300

GPIO AND TIMER HEADERS

A header is provided (P18 and P17) for observation of all Timer and general-purpose input/output (GPIO) signals. In addition to the header, there are also LEDs on these pins.

In unmanaged mode, TIMER0 is used as an interrupt signal to the MAX32690 SPI interface.

When S4 DIP switch is configured to enable time synchronisation, the default configuration for TIMER2 is a 1PPS (one pulse per second) signal and the user can see a blink at a 1-second rate. Similarly, when using the ADI Evaluation software package, the TIMER2 pin is configured for a 1PPS signal by default.

ON-BOARD LEDS

- The board has one power LED, DS1, that lights up to indicate a successful power-up of the board supply rails. The MAX32690 circuit has a bi-colour LED, D6, currently not used.
- There are eight LEDs associated with the ADIN6310 Timer and GPIO functions; link P19 must be inserted to see activity on these LEDs. The TIMER2 pin has a 1PPS signal enabled by default if time synchronisation is enabled.

10BASE-T1L PHY LEDs

- There are three LEDs associated with each 10BASE-T1L port, as shown in Table 7.

Table 7. 10BASE-T1L LED Operation

LED Name	Color	Function
Link/Activity	Green	On if 10BASE-T1L link is up, blink if activity.
Power	Blue	On if PSE controller is supplying power to the port.
LED1	Yellow	On if PHY transmit level of link is 2.4V p-p. Off if transmit level of link is 1.0V p-p.

PHY STRAPPING AND CONFIGURATION

PHY Addressing

The PHY addresses are configured by sampling the RXD pins after power-on, when they come out of reset. External strapping resistors are used on the board to configure each PHY with a unique PHY address. The default PHY addresses assigned to the devices is **shown in Table 8.**

Table 8. Default PHY Addressing

Port Number	PHY	PHY Address
0	ADIN1100	0
1	ADIN1100	1
2	ADIN1300	6
3	ADIN1300	5
4	ADIN1100	2
5	ADIN1100	3

PHY Strapping

There are two ADIN1300 devices on this evaluation board, connected to Port 2 and Port 3 of the switch. Either port is capable of being a Host interface to the switch, so these PHYs must be capable of bringing a link up independent of configuration from the switch. Both PHYs are hardware-strapped for 10/100 HD/FD, 1000 FD leader mode, RGMII no delays, and Auto-MDIX prefer MDIX, allowing them to establish a link with a remote partner. See Table 9. The ADIN1100 PHYs use the default strapping, as shown in Table 10.

Table 9. ADIN1300 PHY Port Configuration

Function	GB PHY Port 2, Port 3
MAC Interface	RGMII with TXC and RXC DLL enabled.
MDI Mode	Auto-MDIX, prefer MDI.
Speed	10/100 HD/FD, 1000 FD follower.

Table 10. ADIN1100 PHY Port Configuration

Function	T1L PHY Port 0, Port 1, Port 4, Port 5
MAC Interface	RGMII.
Software PD after Reset	Enabled.
Leader/Follower	Prefer follower.
Transmit Amplitude	1.0V p-p and 2.4V p-p.

PHY Link Status Polarity

- Note that the ADIN1100 and ADIN1300 LINK_ST output pins are active high by default, whereas the Px_LINK input of the ADIN6310 defaults active low; therefore, the hardware includes an inverter in the path between each of the PHY LINK_ST and the
- Px_LINK of the switch. If component space/cost is a concern, it is possible to avoid including this inverter and rely on a parameter passed as part of the switch configuration to change the PHY polarity as part of the initial configuration.
- This software inversion of the link polarity is supported only for ADI PHY types.
- In the event a PHY is used in the Host interface path to the switch, the link signal provided to the Host port must always be active low, so an inverter must be required for this port.

Link Selection/SGMII Modes

- The switch has a per-port digital input (Px_LINK). When driven low, this tells the switch that port is enabled.
- Port 2 and Port 3 can optionally be configured for SGMII, 1000BASE-KX, or 100BASE-FX mode.
- When using these ports in SGMII modes, the corresponding link jumper (P10 for Port 2, P16 for Port 3) must be connected into the SGMII position.
- This pulls the Px_LINK of the port low, which enables the port. For SGMII mode, ensure that the autonegotiation is disabled (false).
- SGMII mode is not currently supported with the unmanaged configuration from the MAX32690 firmware.
- Configure this mode if modifying the MAX32690 configuration directly, when using TSN evaluation package or when connecting your own Host to the device.

ADIN1300 Link Status Voltage Domain

- The ADIN1300 LINK_ST is primarily intended to drive the switch link signal; therefore resides on the VDDIO_x voltage domain (default voltage rail is 1.8V). If using the LINK_ST pin to drive an LED to indicate link active, a level shifter is used to provide voltage and drive capability for the LED function. The LED anode is tied to 3.3V through a 470Ω resistor.

MDIO INTERFACE

- The MDIO bus of the ADIN6310 connects to the MDIO bus of each of the six PHYs on the evaluation board. The configuration of the PHYs is done by the switch firmware by this MDIO bus.

SWITCH SWD (P6) INTERFACE

- This interface is not enabled.

10BASE-T1L CABLE CONNECTION

- Connect the 10BASE-T1L cables by a pluggable screw terminal block for each port. If more of the pluggable connectors are needed for easy connecting or changing of cables, purchase additional con-nectors from vendors or distributors, such as, Phoenix
- Contact, Part Number 1803581, which is a pluggable, 3-way, 3.81mm, 28AWG to 16AWG, 1.5mm2 screw terminal block.

GROUND CONNECTIONS

- The board has an Earth node. Although this node may or may not be electrically connected to Earth ground, in a real device, this node is typically connected to the device’s metal housing or chassis.
- Connect this Earth node as required in a wider demonstration system by the Earth terminal of the power supply connector, P3, or by an exposed metal plating of four mounting holes in the corners of the board.

- For each port, disconnect the shield of the 10BASE-T1L cable from this Earth node, connected directly, or connect by a 4700pF capacitor (C1_x).
- Select the required connection by the relevant link position of P2_x. Connect the Earth connection and metal body of the two RJ45 connectors (J1_2, J1_3) directly to the Earth node.
- Connect the local circuit ground and the external power supply (except the Earth terminal, P3) to the Earth node by approximately 2000pF of capacitance and approximately 4.7MΩ of resistance.
- Note that the board has been designed only as an evaluation board. It has not been designed nor tested for electrical safety. Any equipment, device, wire, or cable connected to this board must be already protected and safe to touch without danger of electric shock.

SPOE POWER COUPLING

- The circuit includes the five-port LTC4296-1, power supply equip-ment (PSE) controller, which can provide power over data line (PoDL)/single-pair power over Ethernet (SPoE).
- The PSE controller supports powering the four T1L ports and the circuit is designed for PSE Class 12. One port of the PSE device is unused.
- Note that a 20 to 30 V power supply is required to operate SPoE at Class 12; the provided 15 V power supply is not compliant with this power class.
- The PSE controller is powered by default through the P3 or P4 connector, which supports up to 30V. To use the PSE controller for power classes other than Class 12 requires circuit modifications to the high-side, low-side sense resistors, and high-side MOSFET.
- For details on the circuit modifications needed for the different power classes, refer to the LTC4296-1 data sheet.
- The voltage requirement for the other classes can be supported by removing the P25 jumper and providing the required voltage through the P24 connector.
- This allows the PSE controller to be powered up to 55V.
- The PSE controller circuit also includes circuit support for SCCP for purpose of classifying the power for a powered device (PD) at the end node side.
- This uses the microcontroller GPIO pins for SCCP to communicate with the connected

PD. SCCP is not enabled as part of the unmanaged/managed mode; example code for SCCP is included in the Zephyr project.
- Using SCCP, information on the device class, type, and pd_faulted is obtained before power is applied to the cable. To use SCCP, increase the input voltage to the board to 20V minimum.
- For additional details on SCCP protocol and use, refer to the LTC4296-1 data sheet and associated user guide.

MAX32690 MICROCONTROLLER

- The MAX32690 is an Arm Cortex-M4 microcontroller designed for industrial and wearable applications. For this reference design, the MAX32690 is used to configure the switch and the PSE controller.
- Associated with the MAX32690 circuit is external 1Gb of DRAM, 1Gb FLASH Memory, and a MAXQ1065 security device, which is planned to use in future versions.

Firmware on MAX32690

- There is firmware installed on the MAX32690, which supports a basic configuration of the switch and PSE controller. For more details, see the Managed vs. Unmanaged section.

UART and SWD Interfaces

- Connector P20 provides access to the MAX32690 serial interface. P1 provides access to the UART interface.

MAXQ1065 CRYPTOGRAPHIC CONTROLLER

- The MAXQ1065 is an ultra-low-power security cryptographic controller with ChipDNA™ for embedded devices that provides turnkey cryptographic functions for root-of-trust, mutual authentication, data confidentiality and integrity, secure boot, and secure firmware update.
- It provides secure communications with generic key exchange and bulk encryption or complete TLS support. It is planned to enable in future updates for encryption

purposes.

MANAGED VS. UNMANAGED

UNMANAGED CONFIGURATION

- Unmanaged configuration relies on the MAX32690 configuring the ADIN6310 switch and the LTC4296-1 PSE controller to a basic configuration.
- The MAX32690 has firmware loaded to enable the switch configuration based on the positions of the S4 DIP switch, and that runs this configuration after power-up.
- The default configuration for the hardware is unmanaged mode.
- In unmanaged mode, all links from jumpers P7 and P9 are open. When P7 is open, this configures the switch to use SPI as the Host interface and P9 open enables the MAX32690 to run the loaded firmware to configure the switch and PSE.
- The switch is configured for basic switching functionality, including VLAN IDs (1-10) with all ports enabled and configured as follows:
  - Port 0, Port 1, Port 4, Port 5: RGMII, 10Mbps
  - Port 2, Port 3: RGMII, 1000Mbps

Table 11. Jumper Positions for Unmanaged Mode

Link	Position	Function
P7	Open	Selects SPI as Host interface.
P9	Open	MAX32690 enabled.

Switch S4 provides user ability to enable additional functionality for the ADIN6310, namely time synchronisation (IEEE 802.1AS 2020), link layer discovery protocol (LLDP), and IGMP snooping. Table 12 shows the possible combinations and the functionality for each configuration. Note that the corresponding GPIO pins are sampled on power up, therefore, changes to S4 configuration require a power cycle.

Table 12. DIP Switch S4 Configuration

-

Position	Firmware Functionality
0000	Basic Switch + PSE (S4 default).
0001	Basic Switch.
0010	Basic Switch + PSE + Time Sync (802.1AS 2020).
0100	Basic Switch + PSE + LLDP.
0101	Basic Switch + LLDP.
0110	Basic Switch + PSE + Time Sync + LLDP.
0111	Basic Switch + Time Sync + LLDP.
1000	Basic Switch + PSE + IGMP Snooping.
1001	Basic Switch + IGMP Snooping.
1010	Basic Switch +PSE + Time Sync + IGMP Snooping.
1011	Basic Switch + Time Sync + IGMP Snooping.
1100	Basic Switch + PSE + LLDP + IGMP Snooping.
1101	Basic Switch + LLDP + IGMP Snooping.
1110	Basic Switch + PSE + Time Sync + LLDP + IGMP Snooping.
1111	Basic Switch + Time Sync + LLDP + IGMP Snooping.

Note that other TSN functionality or SGMII interface is not supported in unmanaged mode, but available if using managed mode. The PSE configuration is carried out by the MAX32690 firmware, which enables the LTC4296-1 device over SPI.

- The LTC4296-1 circuit is configured for 4 channels of PSE Class 12. When the PSE controller supplies voltage to a T1L port, the blue power LED for that port illuminates.

MANAGED CONFIGURATION AND TSN

- Managed mode for this reference design provides the user the ability to evaluate the broader capability of the ADIN6310 device, including TSN and Redundancy capability.
- Managed mode relies on the use of ADI's TSN evaluation package (application and web server that runs on a Windows 10 PC con-nected to the switch over Ethernet Port 2 or Port 3). The default Host interface is Port 2.
- To use managed mode with the evaluation package, ensure that the links are inserted in P7 to configure the Host interface for the port of choice, see ADIN6310 Host Port Strapping.
- If the PSE controller is not required, then insert the P9 in position 2-3 to keep the MAX32690 in reset.
- Enable the RGMII ports when using the evaluation package.

Table 13. Jumper Positions for Managed Mode

Link	Position	Function
P7	Insert 3-4	SPI_S101.
	Insert 7-8	SPI_SS.
	Insert 9-10	Timer0.
	Insert 11-12	Timer1.
	Insert 15-16	Timer3.
	Others open	Combination selects Port 2 as Host interface.
P10/P16	1-2	PHY mode: ADIN1300 PHY to switch port link input (Px_LINK).
	2-3	SGMII mode: Px_LINK pulled low to enable port.

Switch TSN Evaluation Software

- The evaluation package software is available as a software download from the ADIN6310 product page.
- The evaluation package contains the Windows-based evaluation tool and PC based web server for configuration of the switch (and PHYs).
- This package supports TSN functionality and Redundancy capability and is used for evaluation of the switch.
- This package does not support operation with the MAX32690 or LTC4296-1. A user can view individual switch port statistics, add and remove static entries from the look-up table, and configure TSN features through web pages provided by the web server running on the PC. Once cthe configuration is complete, user applications can communicate with other devices over the TSN network.
- Alternatively, the user can configure the device for Redundancy features such as HSR or PRP.

MANAGED VS. UNMANAGED

The corresponding user guide (UG-2280) is also available from the ADIN6310 product page.

Figure 3. TSN Switch Evaluation – Home Page (Managed Mode)

ses-configuration File

- When using the evaluation package, the ADIN6310 configuration is based on a configuration text file, as shown in Figure 4. The hardware-specific parameters are passed from an xml file contained in each file system, see Figure 5.
- The configuration is specific to the hardware being used. Edit the ses-configuration.txt file to match the hardware by modifying the XML file, as shown in Figure 4.
- Then, launch the application to start configuring the switch.
- Use the XML file name eval-adin6310-10t1l-rev-c.xml the field switch evaluation board, this configuration applies to all hardware revisions from REV C onward, which uses RGMII interface for all Ethernet PHYs.
- The XML file eval-adin6310-10t1l-rev-b.xml matched an older revision of hardware, which used RMII interface for the ADIN1100 PHYs. For more details on using this software, refer to the user guide (UG-2280) from the ADIN6310 product page.

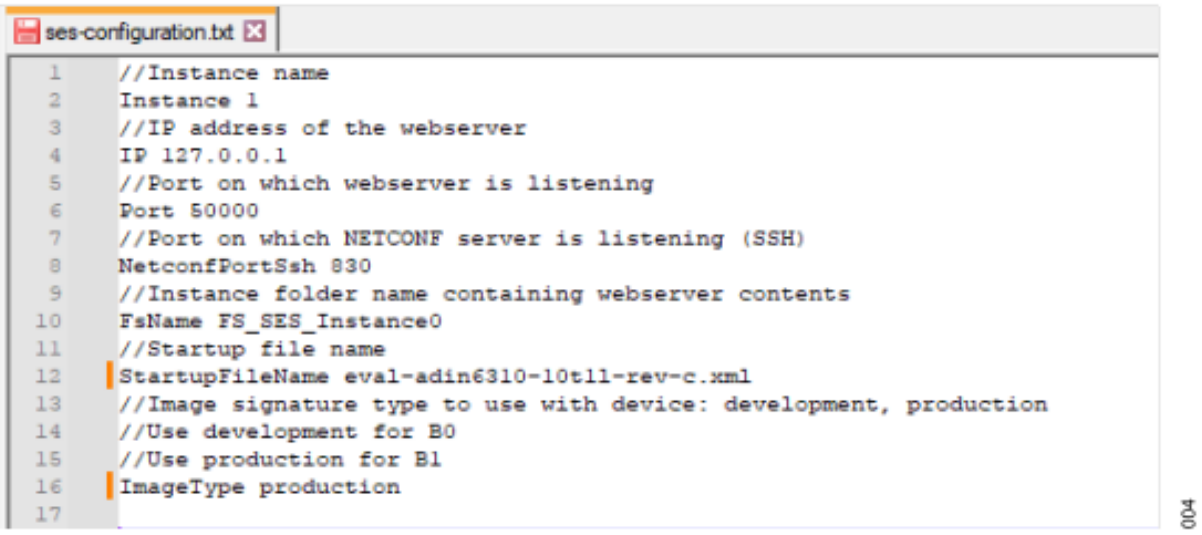


Figure 4. ses-configuration.txt with Field Switch xml File as Startup File

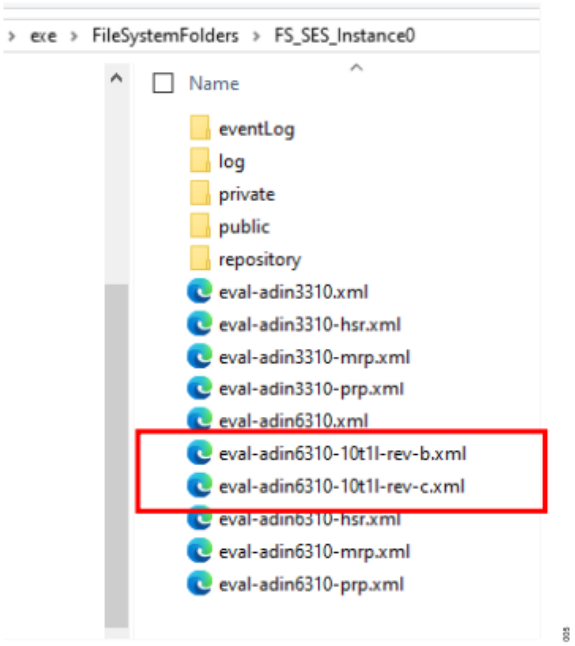


Figure 5. XML File for Use with Field Switch Hardware

TSN SWITCH DRIVER LIBRARY

- The driver package contains the ADIN6310 switch APIs used for configuration of the switch and all its functionality.
- The software is C source code and OS agnostic. Port this package to different platforms to interact with the switch and provide access to all the features currently exposed in the switch.
- The driver package is available to download from the ADIN6310 product page and must be consulted with the user guide (UG-2287).
- When using the driver APIs, the port configuration is specific to the hardware

configuration. For this field switch reference design, the following snippet of code shows the port initialisation structure specifically for this board.

- This structure is passed to the SES_Ini-tializePorts() API during the initialisation of the switch. For more details on the sequence of API calls, refer to the user guide (UG-2287).
- The structure caters for the different PHY configurations and speeds. This version of hardware uses 2 x ADIN1300 PHYs on Port 2 and Port 3 and 4 x ADIN1100 PHYs on Port 0, Port 1, Port 4, and Port 5.
- All PHYs are connected over RGMII interface. This version of hardware uses an inverter in the path from PHY to switch link input, uses external PHY address strapping resistors (phyPullupCtrl).
  When configuring ADIN1100 PHYs, the autonegotiation parameter has no influence on the PHY autonegotiation capability.

MANAGED VS. UNMANAGED

```
//{Port enable, MII, RxDelay, txDelay, clk selection, link polarity, PHY type, {autoneg, pullupctrl,
phyAddr, Speed, Duplex, Crossover}}
const SES_portInit_t initializePorts_p[] = {
{ 1, SES_rgmiiMode, { 0, 0, 0 }, 1, SES_phyADIN1100, {true, 1, 0, SES_phySpeed10, SES_phyDuplexMode▶
Full, SES_autoMdix}},
{ 1, SES_rgmiiMode, { 0, 0, 0 }, 1, SES_phyADIN1100, {true, 1, 1, SES_phySpeed10, SES_phyDuplexMode▶
Full, SES_autoMdix}},
{ 1, SES_rgmiiMode, { 0, 0, 0 }, 1, SES_phyADIN1300, {true, 1, 6, SES_phySpeed1000, SES_phyDuplexMode▶
Full, SES_autoMdix}},
{ 1, SES_rgmiiMode, { 0, 0, 0 }, 1, SES_phyADIN1300, {true, 1, 5, SES_phySpeed1000, SES_phyDuplexMode▶
Full, SES_autoMdix}},
{ 1, SES_rgmiiMode, { 0, 0, 0 }, 1, SES_phyADIN1100, {true, 1, 2, SES_phySpeed10, SES_phyDuplexMode▶
Full, SES_autoMdix}},
{ 1, SES_rgmiiMode, { 0, 0, 0 }, 1, SES_phyADIN1100, {true, 1, 3, SES_phySpeed10, SES_phyDuplexMode▶
Full, SES_autoMdix}}
};
```

SOURCE CODE FOR MAX32690

- The source code project is available on GitHub on the ADI Zephyr fork at the GitHub. The ADIN6310 example project is located in the samples/application_development/adin6310, under the adin6310_switch branch.
- The TSN driver library for the switch is not included in the branch; therefore, add the source code separately when building the project. The TSN driver library is available as a download directly from the ADIN6310 product page.
- This Zephyr project supports multiple examples based on the hardware configuration

of the DIP switch S4 as described in Table 12. The default configuration for the hardware is for the MAX32690 processor to run firmware to configure the ADIN6310

- Ethernet switch over the SPI Host interface into a basic switching mode with VLAN ID 1-10 enabled for learning and forwarding on all ports, and for the LTC4296-1 PSE to be enabled on all ports. SCCP is not enabled, but an example routine is included in the Zephyr code.

COMPILING THE PROJECT

To compile the project, run the following:

```
west build -b adin6310t1l/
max32690/m4 samples/application_develop-
ment/adin6310 -DLIB_ADIN6310_PATH=/path/to/driv-
er/ADINx310 TSN Driver Library RelX.x.x
```

Where DLIB_ADIN6310_PATH is the path to where the ADIN6310 TSN driver software package is located.

FLASHING THE BOARD

Connector P20 provides access to the MAX32690 SWD interface. Depending on the debug probe used, the microcontroller may be programmed, as shown in the following sections.

Segger J-Link

There are two approaches to loading the firmware using Segger J-Link. Firstly, ensure that the J-Link software toolchain is installed (available from Segger website) and accessible from the PATH variable (both for Windows and Linux), then do one of the following:

- ‣ Using west `west flash --runner=jlink`.
- Alternatively, the user can use the JFlash (or JFlashLite) Utility:
- Open JFlashLite and select the MAX32690 MCU as the target.
- Then, program the .hex file located at the build/Zephyr/Zephyr. hex path (in the Zephyr directory). The firmware executes after a successful load.

MAX32625 PICO

- Firstly, the MAX32625 PICO board must be programmed with the MAX32690 image available from Github. This PICO programmer offers direct access to the microcontroller memory, which allows the user to flash hex files with greater flexibility. There are two ways to program the firmware hex file to the MAX32690.

The first approach is the simplest and does not require additional installations. Similar to most DAPLink interfaces, the MAX32625PI-CO board comes preinstalled with a bootloader that enables driver less drag-and-drop updates. This allows users to use the MAX32625PICO board as a tiny, embeddable development platform. The following steps guide how to flash the firmware onto the MAX32690 device:

1. Connect the MAX32625PICO board to the Field switch board P20 connector.
2. Connect the target board to a power source, connect the MAX32625PICO debug adapter to the Host machine.
3. Drag and drop the hex file from the build step onto the DA-PLINK drive to load new firmware into the board. The firmware executes after a successful load.

The alternative approach to flashing using the PICO board using

The West Command requires the user to use a custom version of OpenOCD. The easiest method of getting this version of Open-OCD is to install the MaximSDK using the automatic installer available at MaximSDK. Ensure that the Open On-Chip Debugger is enabled in the Select components window during installation (it is by default). After MaximSDK is installed, OpenOCD is available at the Max-imSDK/Tools/OpenOCD path. Program the MAX32690 now by using west. Run the following in the terminal (must be the same from which a user previously compiled the project):

```
west flash --openocd-search ~/MaximSDK/Tools/
OpenOCD/scripts/ --openocd ~/MaximSDK/Tools/Open-
OCD/openocd.exe
```

Change the path to the MaximSDK base directory based on where it is previously installed.

RUNNING THE FIRMWARE

After programming, the firmware image runs automatically. The microcontroller logs the configuration status over UART (115200/8N1, no parity). With a debugger connected and using a terminal application such as putty, when S4 DIP switch is in position 1111, this shows the following output:

```
Reader thread start
 *** Booting Zephyr OS build v1.12.0-77516-ge▶
ba748058c33 ***
 Check Firmware Version :: SC0000519-005-288
 Configured MAC address: 00:18:80:4b:b5:b9
 PSE disabled
 VID 1 enabled on port 0 to 5 :: 0
 VID 2 enabled on port 0 to 5 :: 0
 VID 3 enabled on port 0 to 5 :: 0
 VID 4 enabled on port 0 to 5 :: 0
 VID 5 enabled on port 0 to 5 :: 0
 VID 6 enabled on port 0 to 5 :: 0
 VID 7 enabled on port 0 to 5 :: 0
 VID 8 enabled on port 0 to 5 :: 0
 VID 9 enabled on port 0 to 5 :: 0
 VID 10 enabled on port 0 to 5 :: 0
 Time Synchonization example
 SES_PtpInitCmlds :: 0
 SES_PtpSetDefaultDs - 0
 LLDP Protcol
 IGMP Snooping
 Configuration done
```

ZEPHYR SETTING UP GUIDE

First-time users of the Zephyr, refer to the Zephyr setting up guide located at Zephyr setting up guide

CASCADING BOARDS

It is possible to daisy-chain multiple boards to increase port count using either the unmanaged configuration with standard Ethernet connections, alternatively, using the TSN evaluation package over either RGMII or SGMII.

CASCADING USING UNMANAGED CONFIGURATION

- When operating in the unmanaged configuration Port 2 and Port 3 are operating as 1Gb trunk ports.Use these ports to cascade boards to increase the port count. As SPI is selected as the Host, connect Port 2 or Port 3 to either Port 2 or Port 3 on the next board in the chain.

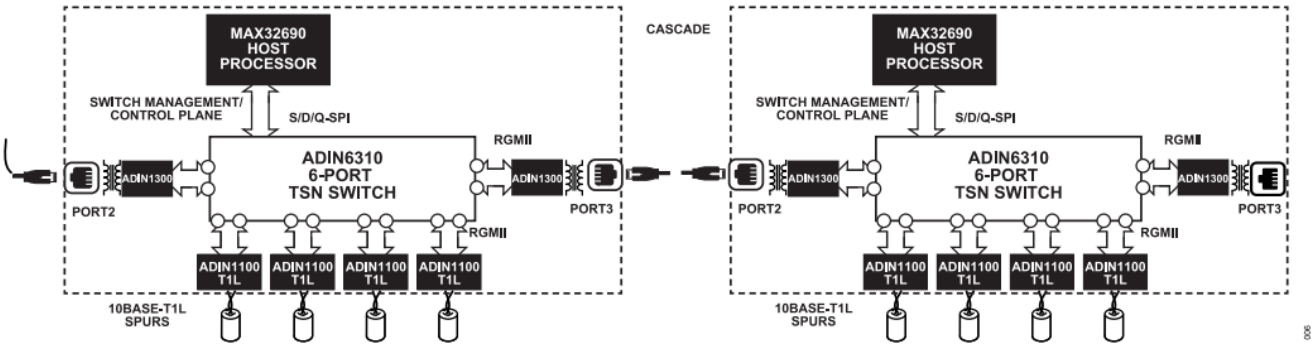


Figure 6. Cascading Using RGMII/Standard Ethernet when Using Unmanaged Configuration (MAX32690 Configures Switch)

CASCADING USING MANAGED CONFIGURATION

Using RGMII Host Interface

When using the TSN evaluation package (PC application and web server) with Port 2 and Port 3 in RGMII mode, the corresponding link jumper (P10 for Port 2, P16 for Port 3) must be connected into the PHY LINK_ST position. In the managed configuration, configure the Port 2 or Port 3 as the Host interface using the P7 jumper positions. The configuration shown in Table 13 configures Port 2 as the Host interface. In this case, cascading boards to increase the port count, Port 2 of the first board must be connected to the Host PC running the Windows TSN evaluation application. Port 3 is connected to Port 2 of the next board in the chain, and so on. The TSN evaluation package can configure multiple switches in a chain, up to ten max. For more details, refer to the user guide

(UG-2280). Ensure that the ses-configuration.txt file points to the relevant xml configuration file as discussed in the ses-configuration File section.

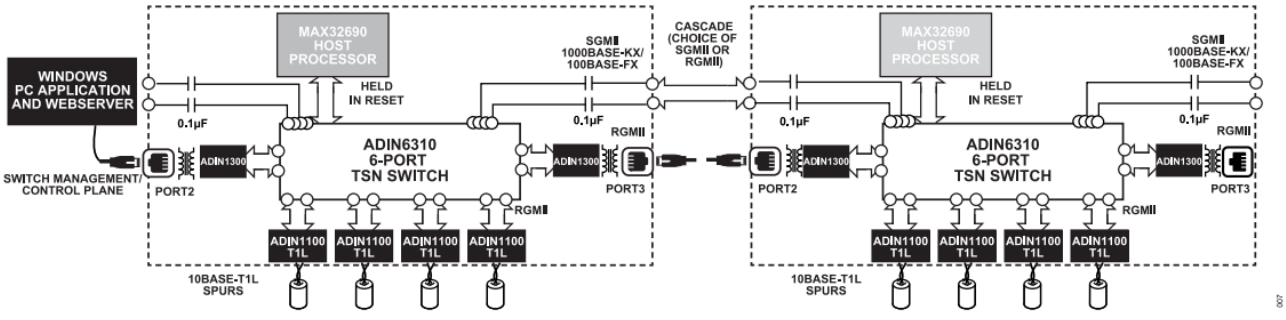


Figure 7. Cascading Using when Using Managed Configuration (TSN Evaluation Package Configures Switch)

Using SGMII to Cascade

The ADIN6310 switch supports four ports configured with SGMII modes, however, the evaluation board hardware supports configuration of SGMII modes for Port 2 and Port 3 only. SGMII modes of operation are not supported in the unmanaged mode. User can modify the Zephyr project code to use SGMII modes if required. Enable the SGMII modes by using the TSN evaluation package, where you configure Port 2 and Port 3 for SGMII, 100BASE-FX, or 1000BASE-KX mode. If Port 2 or Port 3 are used in SGMII mode, ensure to connect the corresponding link jumpers (P10 for Port 2, P16 for Port 3) into the SGMII position. When using SGMII mode between ADIN6310 devices, disable the autonegotiation as this is a MAC-MAC interface.
SGMII mode is not currently supported with the unmanaged config-uration.

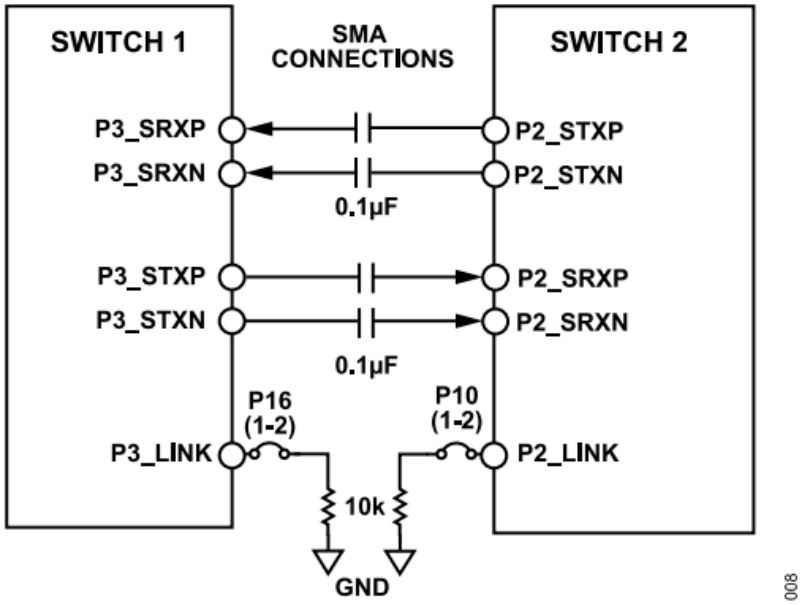


Figure 8. Cascading Using SGMII

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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Documents / Resources

	ANALOG DEVICES ADIN6310 Field Switch Reference Design [pdf] Owner's Manual ADIN6310, ADIN1100, ADIN1300, LTC4296-1, MAX32690, ADIN6310 Field Switch Reference Design, ADIN6310, Field Switch Reference Design, Switch Reference Design, Reference Design

References

- User Manual

Analog Devices

ADIN1100, ADIN1300, ADIN6310, ADIN6310 Field Switch Reference Design, Analog Devices, Field Switch Reference Design, LTC4296-1, MAX32690, Reference Design, Switch Reference Design

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