ams TMD3719 Flicker Detection User Guide

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Introduction

The TMD3719 features ambient light and color (RGB) sensing, proximity and flicker detection. The device integrates direct detection of ambient light flicker for 4 selectable frequency bins. There are two flicker detection modes; On-chip mode and data sampling mode. During the data sampling mode, the flicker detection engine can buffer data in a FIFO for calculating other flicker frequencies externally. In this document, the registers necessary to configure and the usage of both modes will be discussed.

Flicker Detection Registers

The TMD3719 registers necessary to make the flicker function work are summarized in this section. These registers can also be found in the datasheet.

The values of all registers and fields that are listed as reserved or are not listed, must not be changed at any time.

FD_CFG0 Register (Address 0x40)

Addr: 0x40		FD_CFG0			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
7:5	Reserved	000			
4:3	FD_SAMPLES	00	R/W	Flicker Detection Number of Samples	
				VALUE	**SAMPLES**
				0 (default)	128
				1	256
				2	512
				3	1024 (1)
2	Reserved	0			
1:0	FD_TIME	00	R/W	Flicker Detection Time	
				VALUE	**TIME**
				0	50 ms
				1 (default)	100 ms
				2	200 ms
				3	User Defined by FD_SAMPLE_TIME and FD_SAMPLES

FD_CFG0

1. If FD_MODE = 1 (register 0x82 [6]) then the number of samples changes from 1024 to unlimited.

FD_CFG5 Register (Address 0x45)

Addr: 0x45		FD_CFG5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FD_CHANNEL_DISABLE[1]	0xFE	R/W	**Flicker Detection Channel Disable.** Selects which channels to be used for flicker detection.

FD_CFG5 Register

1. Select which modulator channels should be connected/used by the on_ chip flicker engine. Note that the bitstreams are added before the engine evaluates the data. The register bits are one hot encoded where bit 0 means modulator 0, and so on.

FD_CFG7 Register (Address 0x47)

Addr: 0x47		FD_CFG7		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	Reserved	000000		
1:0	FD_SAMPLE_TIME_H	01	R/W	**Flicker Detection Sample Time High**. These bits are the high byte of the 10 bits used for setting the flicker detection integration time.

FD_CFG7 Register

FD_CFG7 Register (Address 0x48)

Addr: 0x48		FD_CFG8		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	Reserved	000000		
1:0	FD_SAMPLE_TIME_L	01	R/W	**Flicker Detection Sample Time Low**. This register is the low byte of the 10 bits used for setting the flicker detection integration time.

FD_CFG8 Register

ENABLE Register (Address 0x80)

Addr: 0x80	ENABLE			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved	0		
6	FDEN	0	R/W	**Flicker Detection Enable**. Writing a 1 activates flicker detection. Writing a 0 disables flicker detection.
5	Reserved	0		
4	AEN	0	R/W	**ALS Enable**. Writing a 1 enables ALS/Color. Writing a 0 disables ALS/Color.
3	PEN	0	R/W	**Proximity Enable.** Writing a 1 enables proximity. Writing a 0 disables proximity.
2:1	Reserved	00		
0	PON	0	R/W	**Power ON.** When asserted, the internal oscillator is activated, allowing timers and ADC channels to operate. Writing a 0 disables the oscillator and clears PEN and AEN. Only set this bit after all other registers have been initialized by the host.

ENABLE Registe

MEAS_MODE1 Register (Address 0x82)

Addr: 0x82		MEAS_MODE1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved	0		
6	FD_MODE	0	R/W	**Flicker Detection Mode.** Writing a 0 will set the FD to on-chip mode and writing a 1 will set the FD to data sampling mode.
5:3	Reserved	000	R/W	
2:0	FIFO_MODE	0	R/W	FIFO Mode VALUE / MODE 0 – Off 1 – 32-bit 2 – 16-bit ALS 3 – 16-bit FD 4 – 8-bit FD 5 – 7 – Reserved

MEAS_MODE1 Register

MOD_GAIN_0_1 Register (Address 0x89)

Addr: 0x89		MOD_GAIN_0_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	MOD_GAIN1	0000	R/W	Modulator One Gain VALUE / GAIN 0 – 2x 1 – 4x 2 – 8x 3 – 16x 4 – 32x 5 – 64x 6 – 128x 7 – 256x 8 – 512x 9 – 1024x 10 – 2048x 11 – 4096x 12 – 15 – Reserved
3:0	MOD_GAIN0	0000	R/W	Modulator Zero Gain VALUE / GAIN 0 – 2x 1 – 4x 2 – 8x 3 – 16x 4 – 32x 5 – 64x 6 – 128x 7 – 256x 8 – 512x 9 – 1024x 10 – 2048x 11 – 4096x 12 – 15 – Reserved

MOD_GAIN_0_1 Register

MOD_GAIN_2_3 Register (Address 0x8A)

Addr: 0x8A		MOD_GAIN_2_3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	MOD_GAIN3	0000	R/W	Modulator Three Gain VALUE / GAIN 0: 2x 1: 4x 2: 8x 3: 16x 4: 32x 5: 64x 6: 128x 7: 256x 8: 512x 9: 1024x 10: 2048x 11: 4096x 12 – 15: Reserved
3:0	MOD_GAIN2	0000	R/W	Modulator Two Gain VALUE / GAIN 0: 2x 1: 4x 2: 8x 3: 16x 4: 32x 5: 64x 6: 128x 7: 256x 8: 512x 9: 1024x 10: 2048x 11: 4096x 12 – 15: Reserved

MOD_GAIN_2_3 Register

MOD_GAIN_4_5 Register (Address 0x8B)

Addr: 0x8B		MOD_GAIN_4_5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	MOD_GAIN5	0000	R/W	Modulator Five Gain VALUE / GAIN 0 / 2x 1 / 4x 2 / 8x 3 / 16x 4 / 32x 5 / 64x 6 / 128x 7 / 256x 8 / 512x 9 / 1024x 10 / 2048x 11 / 4096x 12 – 15 / Reserved
3:0	MOD_GAIN4	0000	R/W	Modulator Four Gain VALUE / GAIN 0 / 2x 1 / 4x 2 / 8x 3 / 16x 4 / 32x 5 / 64x 6 / 128x 7 / 256x 8 / 512x 9 / 1024x 10 / 2048x 11 / 4096x 12 – 15 / Reserved

MOD_GAIN_4_5 Register

MOD_GAIN_6_7 Register (Address 0x8C)

Addr: 0x8C		MOD_GAIN_6_7		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	MOD_GAIN7	0000	R/W	Modulator Seven Gain **VALUE** / **GAIN** 0 / 2x 1 / 4x 2 / 8x 3 / 16x 4 / 32x 5 / 64x 6 / 128x 7 / 256x 8 / 512x 9 / 1024x 10 / 2048x 11 / 4096x 12 – 15 / Reserved
3:0	MOD_GAIN6	0000	R/W	Modulator Six Gain **VALUE** / **GAIN** 0 / 2x 1 / 4x 2 / 8x 3 / 16x 4 / 32x 5 / 64x 6 / 128x 7 / 256x 8 / 512x 9 / 1024x 10 / 2048x 11 / 4096x 12 – 15 / Reserved

MOD_GAIN_6_7 Register

CONTROL Register (Address 0xF6)

Addr: 0xF6		CONTROL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	00000		
2	ALS_MANUAL_AZ	0	R/W	**ALS Manual Autozero.** Starts a manual autozero of the ALS engines. Set AEN = 0 before starting a manual autozero for it to work.
1	FIFO_CLR	0	R/W	**FIFO Buffer Clear.** Clears all FIFO data, FINT, FIFO_OV, and FIFO_LVL.
0	CLEAR_SAI_ACTIVE	0	R/W	**Clear Sleep-After-Interrupt Active.** Clears SAI_ACTIVE, ends sleep, and restarts device operation.

CONTROL Register

FIFO_MAP2 Register (Address 0xFA

Addr: 0xFA		FIFO_MAP2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	000		
4	FIFO_WRITE_FD_RESULTS	0	R/W	**FIFO Write Flicker Detection Result.** If asserted, flicker detection on-chip calculation result is written to the FIFO buffer.
3	FIFO_WRITE_FD_DATA	0	R/W	**FIFO Write Flicker Detection Data.** If asserted, flicker detection data is written to the FIFO buffer.
2	FIFO_WRITE_PDATAR	0	R/W	**FIFO Write Proximity Ratio Data.** If asserted, proximity ratio data is written to the FIFO buffer.
1	FIFO_WRITE_PDATA1	0	R/W	**FIFO Write Proximity One Data.** If asserted, proximity one data is written to the FIFO buffer.
0	FIFO_WRITE_PDATA0	0	R/W	**FIFO Write Proximity Zero Data.** If asserted, proximity zero data is written to the FIFO buffer.

FIFO_MAP2 Register

FIFO_STATUS Register (Address 0xFB)

Addr: 0xFB		FIFO_STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	FIFO_OV	0	R	**FIFO Buffer Overflow**. Indicates that the FIFO buffer overflowed and information has been lost. Bit is automatically cleared when the FIFO is read.
6:0	FIFO_LVL	0000000	R	**FIFO Buffer Level**. Indicates the number of entries (each are 4 bytes) available in the FIFO buffer waiting for readout. The FIFO level can be between 0 (empty) and 64 (full).

FIFO_STATUS Register

FIFO Buffer Data Register (Address 0xFC – 0xFF)

Addr	Name	Type	Description	7 6 5 4 3 2 1 0	Reset
0xFC	FDATA	R	FIFO buffer data	00000000	0x00
0xFD				00000000	0x00
0xFE				00000000	0x00
0xFF				00000000	0x00

FIFO Buffer Data Register

Flicker Detection Modes

On-Chip Mode

Flicker function can be activated by the flicker enable bit in register 0x80 bit 6 (MEAS_MODE1.FDEN). Writing a 1 activates flicker detection. Writing a 0 disables flicker detection. The time to measure for flicker is set by using register FD_CFG0.FD_TIME (0x40 bits [1:0]). The sampling time can be set to 50/100/200 milliseconds for a frequency bin resolution of 20/10/5 Hz, respectively. Also, a user defined FD_TIME can be defined by FD_SAMPLE_TIME in registers FD_CFG7 (0x47 bits [7:0]) and FD_CFG8 (0x48 [1:0]) in combination with FD_SAMPLES of register FD_CFG0 (0x40 bits [4:3]). When setting register FD_CFG0.FD_TIME (0x40 bits [1:0]) to one of the preset sampling times, registers FD_CFG7 (0x47) and FD_CFG8 (0x48) are set with a preset value for sample time. These preset values are shown in .

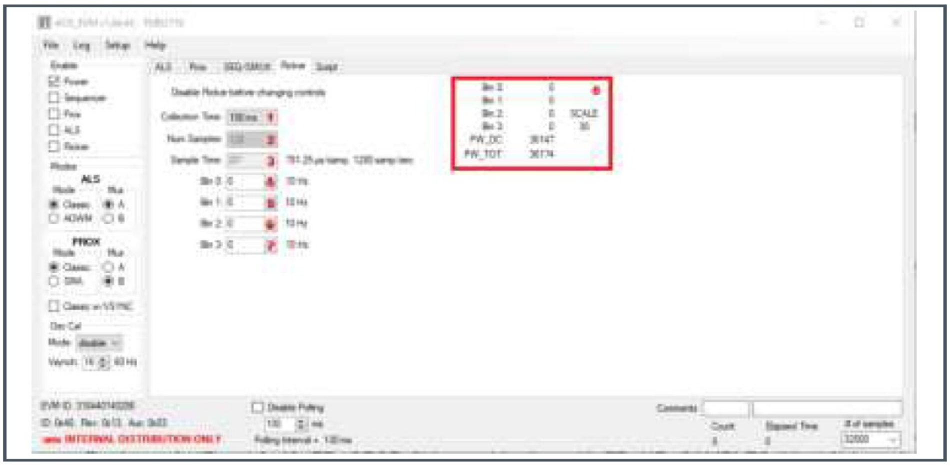
Value	FD_TIME[(3)] 0x40 bits [1:0]	FD_SAMPLES 0x40 bits [4:3]	FD_SAMPLE_TIME 0x47 & 0x48
0	50 ms[(1)]	128	143
1	100 ms[(1)]	128	287
2	200 ms[(1)]	128	575
3	User defined	1024[(2)]	User Defined

Registers FD_CFG7 (0x47) and FD_CFG8 (0x48) combine to make a 10-bit value.

Flicker Sampling Time Configurations

1. When selecting 50 ms/100 ms/200 ms, register FD_SAMPLES gets overwritten with 128.
2. Unlimited, if FD_MODE = 1, FIFO_WRITE_FD_DATA = 1, and FIFO_MODE > 0 else 1024.
3. FD_TIME = FD_SAMPLES * (FD_SAMPLE_TIME + 1) * modclk; modclk = 2.71 µs.

For example: FD_CFG0 (0x40) = 0x01(default) – This selects FD_TIME as 100 ms. Therefore, FD_SAMPLES = 128 and FD_SAMPLE_TIME = 287.
The on-chip flicker function uses the Goertzel Algorithm embedded in the device.



TMD3719 GUI

Index	Description	Register(s) [bits]	Comments
1	Time to measure flicker	0x40 [1:0]	200 ms, 100 ms (Default), 50 ms, user defined(1)
2	Number of samples to be measured for flicker	0x40 [4:3]	128 (Default), 256, 512, 1024 (Unlimited(2))
3	Integration time for flicker	0x47 [1:0], 0x48 [7:0]	Must not be changed with FDEN = 1 and PON = 1
4 – 7	Coefficients input to algorithm to decode bin distances	0x41[4:0], 0x42[4:0], 0x43[4:0], 0x44[4:0]	Inputs to the on-chip algorithm. 200 ms: 5 Hz to 160 Hz, 5 Hz steps 100 ms: 10 Hz to 320 Hz, 10 Hz steps 50 ms: 20 Hz to 640 Hz, 20 Hz steps
8	Results from the algorithm		

Explanation of Fields in the Above GUI Image

1. Can be used to select different combinations using number of samples (0x40 [4:3]) and sample time (0x47, 0x48).
2. If fd_mode = 1, fifo_write_fd_data = 1, and fifo_ mode > 0 else 1024.

Data Sampling Mode

This section gives guidance on configuring flicker for 16-bit sampling mode and accessing flicker detection data from the FIFO. This section shows an example of a specific flicker configuration. Adjustment to the configuration could be made for a different application. FIFO access can be read out with single reads starting at FDATA0 (0xFC). 4 consecutive I2C addresses have to be read to get a full data set. Upon reading FDATA3 (0xFF), then reading FDATA0 again (I2C address wrap around) it automatically decreases the FIFO_STATUS.FIFO_LVL (0xFB). If reading beyond the end of the FIFO, data will return 0x00. There is no under-run flag, this is not as error condition.

Configuring Flicker Detection:

1. Configure ENABLE (0x80) = 0x01 – (Enable PON).
2. Configure FD_CFG0 (0x40) = 0x02 – (FD_TIME = 200 ms, FD_SAMPLES = 128).
3. Configure MOD_GAIN
    - MOD_GAIN_0_1 (0x89) = 0x02 – (8x)
    - MOD_GAIN_2_3 (0x8A) = 0x02 – (8x)
    - MOD_GAIN_4_5 (0x8B) = 0x02 – (8x)
    - MOD_GAIN_6_7 (0x8C) = 0x02 – (8x)
4. Configure FD_CFG5 (0x45) = 0x00 – (All flicker channels active).
5. Configure MEAS_MODE1 (0x82) = 0x43 – (FD_MODE = sampling mode, FIFO_MODE = 16 bits).
6. Configure FIFO_MAP2 (0xFA) = 0x08 (Write data to FIFO).

Clearing the FIFO:

1. Read ENABLE register (0x80) contents and save it to a variable 'A'.
2. Set ENABLE register (0x80) to 0x1, only PON is enabled.
3. Read CONTROL register (0xF6) and save it to a variable 'B'.
4. Set variable 'B' bit 1 (FIFO_CLR) to 1, leave other bits same.
5. Write 'B' back to CONTROL register (0xF6).
6. Write variable 'A' to ENABLE register (0x80) to recover the original state.
7. Configure ENABLE (0x80) = 0x41 (PON = 1, FDEN=1).

Polling Flicker Data

1. Read FIFO_STATUS (0xFB).
2. Check FIFO_OV (0xFB [7]) – FIFO buffer overflow, if flag is set information has been lost.
3. Check FIFO_LVL (0xFB [6:0]) – FIFO level, indicates number of entries available.
4. If FIFO_OV = 1 then;
5. Clear FIFO.
6. Delay 50 ms.
7. If FIFO_LVL is not 0 then;
8. Poll FIFO buffer data FDATA (0xFC, 0xFD, 0xFE, 0xFF).

Polling of the FIFO should be done such that the FIFO does not overflow. FIFO capacity is 256 bytes, the highest FIFO level is 256/4 = 64. If 200 ms is selected for FD_TIME, FD_SAMPLES would be equal to 128 and while sampling the FIFO at 200 ms. The FIFO would more than likely overflow creating loss of data since 128 samples (256 bytes) is the full depth of the FIFO. If the FIFO sampling frequency was reduced to 100 ms, the number of samples would be 64 (128 bytes), which is only half of the FIFO size then you will not have FIFO overflow. Therefore, to calculate the appropriate sample time, determine what will fill half of the FIFO or at most 2/3 of the FIFO and use that time as the sampling period.

Summary / Results

There are two modes for configuring the flicker function in this device, on-chip and data sampling. On-chip flicker detection uses an embedded algorithm and data sampling uses FIFO to access data. ams OSRAM provides a robust flicker detection functionality in many devices, the primary application for the flicker detection function would be flicker-immune camera operation. These efforts can make it easier to minimize flicker-induced problems.

Revision Information

Changes from previous version to current revision v1-00	Page
Initial production version	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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Documents / Resources

	ams TMD3719 Flicker Detection [pdf] User Guide TMD3719 Flicker Detection, TMD3719, Flicker Detection, Detection

References

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