

Contents [[hide](#)]

- [1 ALPHA DATA ADM-VA601 Software Development Kit](#)
- [2 Introduction](#)
- [3 Hardware Requirements](#)
- [4 Software Tools](#)
- [5 Package Structure](#)
- [6 Contact](#)
- [7 FAQ](#)
- [8 Documents / Resources](#)
 - [8.1 References](#)



ALPHA DATA ADM-VA601 Software Development Kit



Introduction

This application note provides instructions for creating, modifying, and deploying a Versal ACAP image for the ADM-VA601, including all necessary features for programming and booting from Avalanche's space-grade P-SRAM (MRAM) QSPI configuration memory. The package includes all required software components to build this image.

Hardware Requirements

- ADK-VA601 kit
- ADM-VA601-FL3 Daughter board with Avalanche QSPI P-SRAM™ (MRAM)
- VITA46 Backplane
- Host PC with Vitis Unified IDE 2022.2 installed
- Micro SD card reader and micro SD card
- USB-Serial cable with DSUB9 connector

Software Tools

The FPGA project requires Vivado 2022.2, running on either Windows or Linux. See <https://www.xilinx.com/support/documentation-navigation/design-hubs/dh0013-vivado-installation-and-licensing-hub.html> for more details about supported operating systems. Building a bootable Linux image requires PetaLinux 2022.2 and a compatible Linux operating system. See <https://docs.xilinx.com/r/en-US/ug1144-PetaLinux-tools-reference-guide/Overview> for more details about supported operating systems.

Package Structure

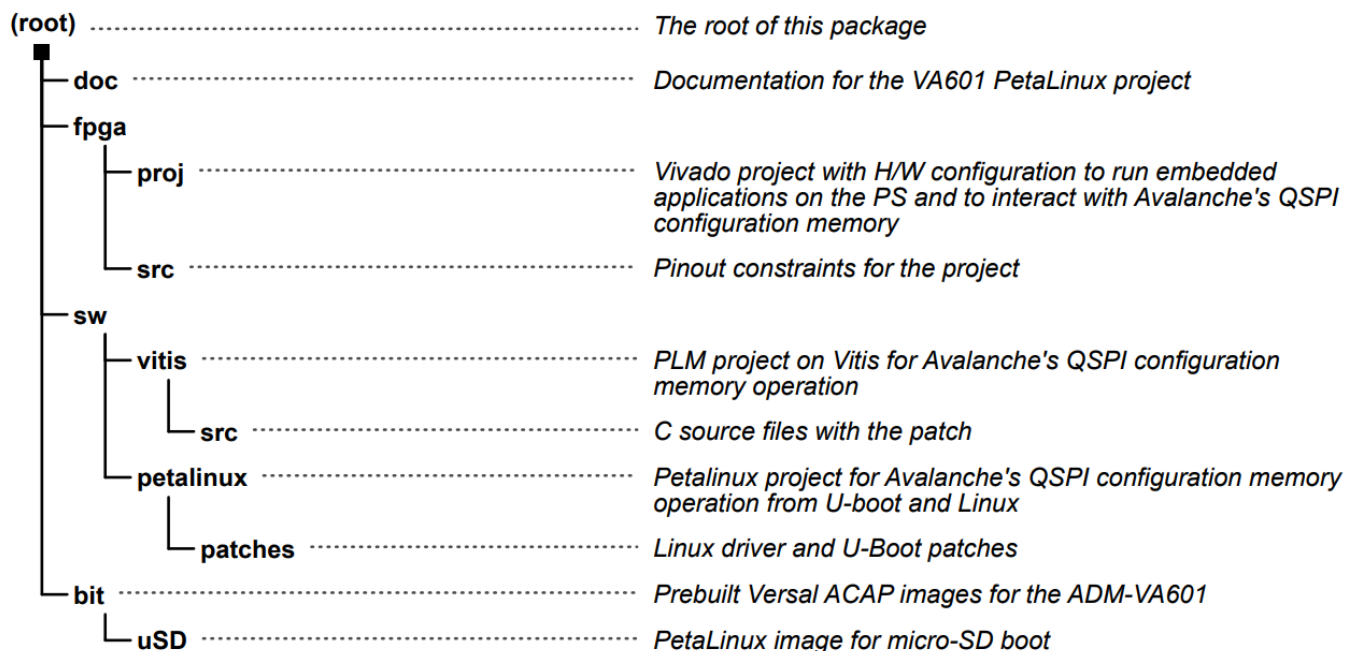


Figure 1 : Package structure

Creating the Hardware Platform in Vivado

The Vivado project includes a block design featuring CIPS and NoC IPs, the fundamental building blocks that enable the processing system (PS) to run applications. The NoC configuration provides access to PS peripherals, the PL, and DDR4 SDRAM memory, allowing PetaLinux to operate within its own memory space.

To generate the Vivado project you can use the Makefiles included in the package, assuming a Linux-based OS is used. Open a bash shell in Linux and enter the following commands:

```
export XILINX_TOOLS_VERSION=2022.2
source $(XILINX_LOC)/Vivado/$(XILINX_TOOLS_VERSION)/settings64.sh
{pkg_root}/fpga/proj:$ make
```

Note:

Alternately, if you run make from the package root folder, all the other output products for Vitis and Petalinux will be generated after the .xsa file is obtained.

The created Vivado project can later be modified by opening it in Vivado's GUI. Below is an example of the block diagram as it appears in Vivado's IPI:

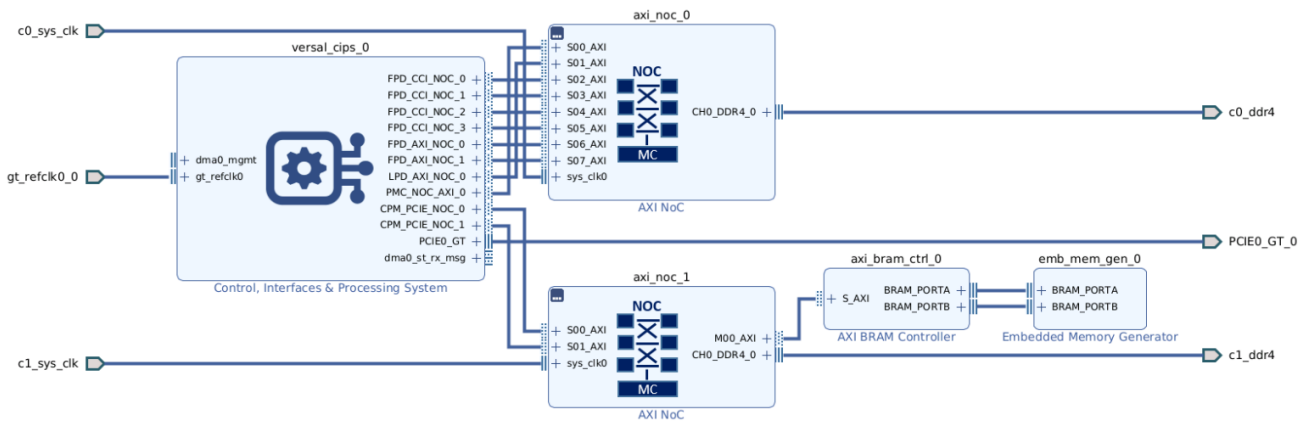


Figure 2 : Vivado base Project for the ADM-VA601 with the QSPI boot set for using the Avalanche QSPI configuration memory

The project can also be generated by running the script in Vivado's GUI. For that, open Vivado and select the following option from the main menu:

Tools -> Run Tcl script...

In the file selection dialog box that appears, navigate to {pkg_root}/fpga/proj/ps-test-va601-ava.tcl. This script will generate the block diagram, execute the build steps to create the device image, and export the platform's XSA file (ps-test-va601-ava.vitis/ps-test-va601-ava.xsa) for use in Vitis/PetaLinux. In addition to the CIPS IP configurations required to enable platform compatibility with the ADM-VA601 board, the script pre-populates the QSPI settings to work with the ADM-VA601-FL3 module, which is fitted with the

Avalanche QSPI configuration memory. The provided script for generating the project (ps-test-va601-ava.tcl) performs the following actions, which are also outlined below for manual execution by the user:

1. Run Vivado, and open the project
2. Select "Boot Mode"
3. Select "QSPI" as a Boot/Storage
4. Select "Dual Parallel" as QSPI Mode
5. Select "x4" as Data Mode
6. Enter "80" for Requested QSPI Reference Clock Frequency (MHz)

MRAM QSPI Interface Frequency (MHz) = QSPI Reference Clock Frequency (MHz)/2

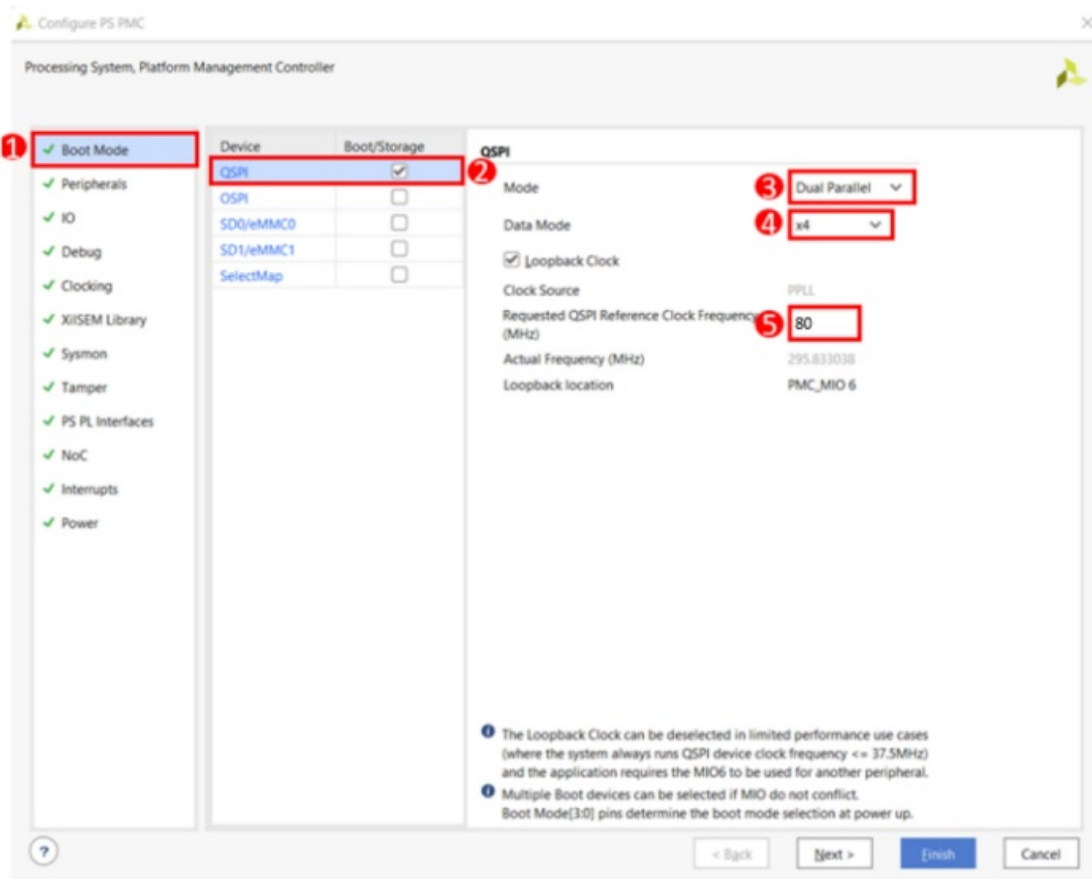


Figure 3 : QSPI Boot configuration for the Vivado Hardware Platform

Modifying Existing QSPI Driver and PLM (Platform Loader and Manager)

To enable the Versal ACAP's PLM (Platform Loader and Manager, or First Stage Bootloader) to detect and operate the Avalanche QSPI configuration memory, custom PLM firmware is required. This firmware must include bare-metal drivers patched with the new source code for the Avalanche component. To achieve this, we will create a Vitis platform using the hardware platform exported in the previous step (.xsa). This platform will contain only the Platform Loader and Manager (PLM) and can be created from a template in Vitis.

In Linux, open a bash shell and run make:

source

```
$(XILINX_LOC)/Vivado/$(XILINX_TOOLS_VERSION)/settings64.sh{pkg_root}/sw/vitis:$
make
```

Note:

make regenerates the .xsa file only from the root folder. If the Vivado hardware platform has been updated, run make from the root or Vivado folder first. Ensure the environment

setup script is sourced, then run: `export XILINX_TOOLS_VERSION=2022.2`

This will create a new PLM firmware and patch the bare-metal drivers in the BSP. For more information on how to create the PLM, visit this link:

<https://xilinx.github.io/Embedded-DesignTutorials/docs/2021.2/build/html/docs/Introduction/Versal-EDT/docs/A-creating-plm.html>

The user can manually create this PLM project using the Vitis GUI or by running the following command in the XSCT console view (also accessible in the GUI): `app create -name ${app_name} -hw ${xsa_path} -proc versal_cips_0_pspmc_0_psv_pmc_0-os standalone -template "versal PLM"`

Where:

`app_name` = ps-test-va601-ava-plm

`xsa_path` = path to .xsa file (normally under `{pkg_root}/fpga/proj/prj_name/prj_name.vitis`)

The bare-metal drivers that are patched are in the files `xloader.c` and `xloader.h`, where Avalanche's IDs get added to the the driver source code. These changes are indicated in the figures below:

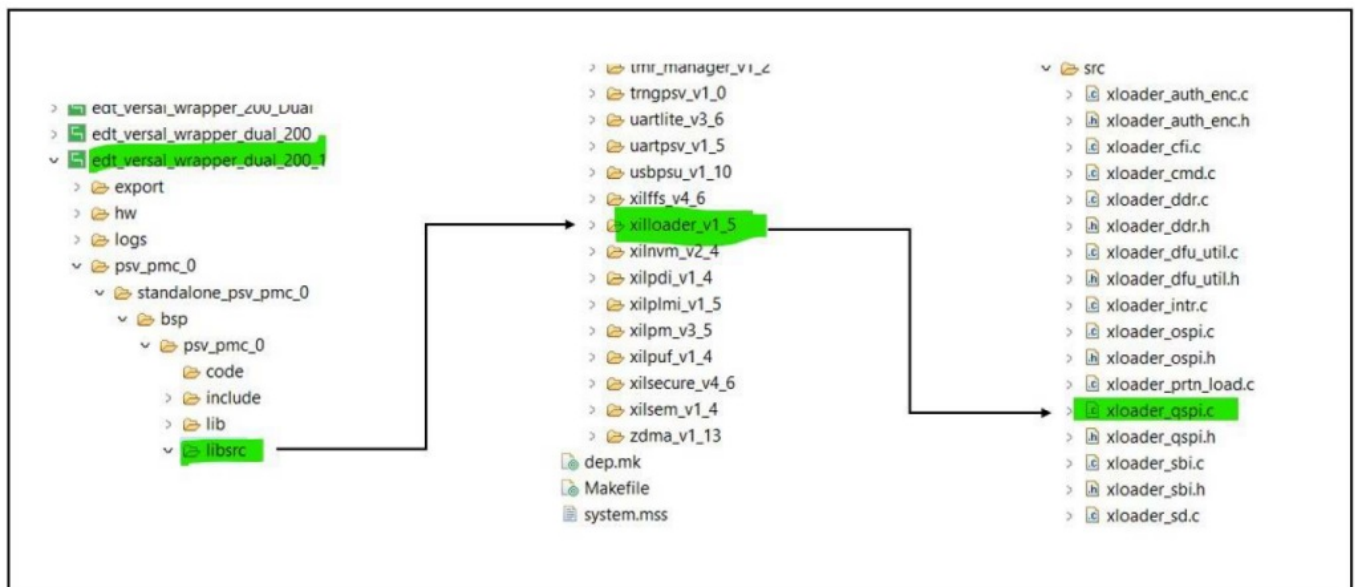


Figure 4 : xloader.c file location in the BSP

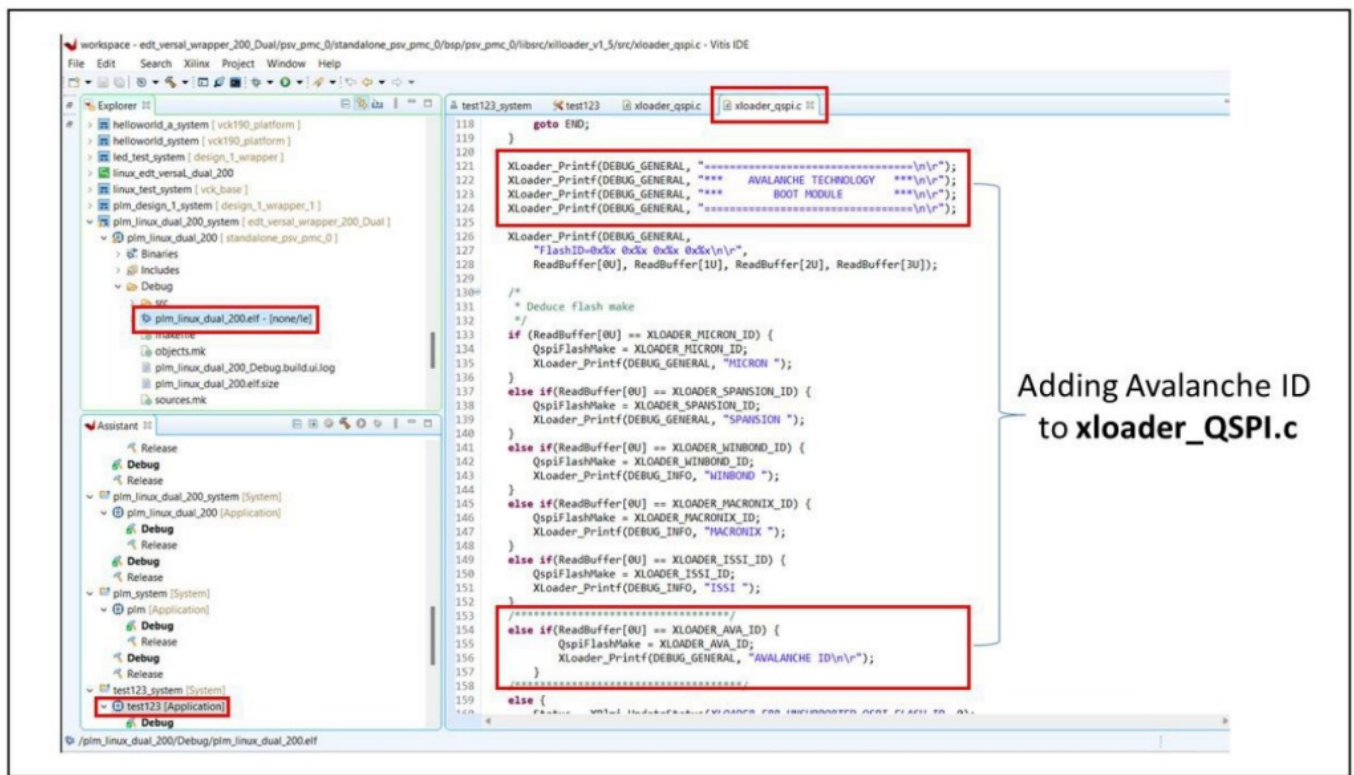


Figure 5 : Avalanche's IDs added to the bare-metal driver

Creating the Petalinux Image

The package provides scripts to create a PetaLinux image from the Vivado hardware platform, as usual. However, additional steps are required for the PetaLinux image to work with the Avalanche QSPI configuration memory:

- Define the QSPI configuration memory partitions.
- Update U-Boot (secondary bootloader) to include the Avalanche device ID.
- Update the Linux kernel to include the Avalanche device ID.
- Replace the PLM generated by PetaLinux with the modified PLM created in Vitis in the previous step.

To generate the Petalinux image with from the previously generated hardware platform (.xsa) and patched PLM (plm.elf), open a bash shell in Linux and run make from the specified path: `{pkg_root}/sw/petalinux:$ make`

Note:

Note that make will regenerate the .xsa and .elf files only when run from the package root folder. If updates are made to the Vivado hardware platform or Vitis PLM, run make from the root or respective folders first. Ensure the environment setup script is sourced, then run: `export XILINX_TOOLS_VERSION=2022.2`

Steps to create the Petalinux image (manually)

1. Source the Petalinux environment: `source $(PETALINUX)/$(XILINX_TOOLS_VERSION)/settings.sh`
2. Create the Petalinux project with the standard BSP settings for Versal: `petalinux-create -t project --template versal -n $(PRJ_DIR)`
3. Change BSP settings for our custom platform: `petalinux-config --get-hw-description=$(XSA_ORIG) --silentconfig`
4. Apply the specific device tree for the ADM-VA601:
`cp pkg_root/sw/petalinux/device-tree/system-user.dtsi project-spec/meta-user/recipes-bsp/device-tree/files/system-user.dtsi`
5. Apply Avalanche's patches to U-boot:
`cp patches/u-boot/*.bbappend project-spec/meta-user/recipes-bsp/u-boot/u-boot-xlnx_%.bbappend`
`cp patches/u-boot/*.patch project-spec/meta-user/recipes-bsp/u-boot/files/ava_u-boot_2022.2.patch`
6. Apply Avalanche's patches to Linux Kernel:
`cp patches/kernel/*.bbappend project-spec/meta-user/recipes-kernel/linux/linux-xlnx_%.bbappend`
`cp patches/kernel/*.patch project-spec/meta-user/recipes-kernel/linux/linux-xlnx/ava_kernel_2022.2_p1.patch`
`cp patches/kernel/*.patch project-spec/meta-user/recipes-kernel/linux/linux-xlnx/ava_kernel_2022.2_p2.patch`
7. Build the Petalinux image: `petalinux-build --> build Petalinux image`
8. Package BOOT.BIN in the Petalinux image with the patched PLM: `petalinux-package --boot --u-boot --plm $(ELF_ORIG) --force`

Programming and booting from QSPI configuration memory

1. Copy the provided PetaLinux image files to an SD card. These are the following:
 - BOOT.BIN
 - image.ub
 - boot.scr

2. Insert the micro-SD into the uSD socket.

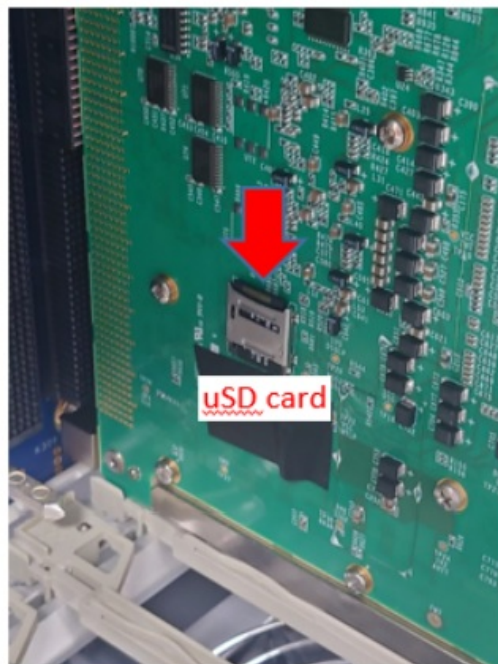


Figure 6 : micro-SD card location

3. Insert the ADM-VA600-FL3 into the top side of the VA601 (image for representation, FL3 module may differ).



Figure 3 : Flash Card Install Location

Figure 7 : ADM-VA600-FL3 location

4. Connect the USB-Serial converter cable to the UART port on the RTM.

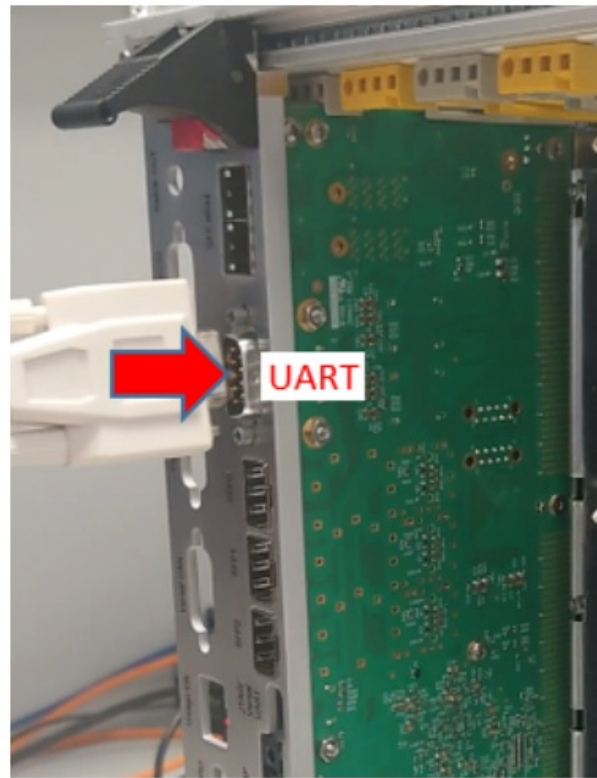


Figure 8 : UART connection

5. Set the SW2 position in microSD boot mode.

Mode Switch SW2 [4:1]: OFF, OFF, OFF, ON

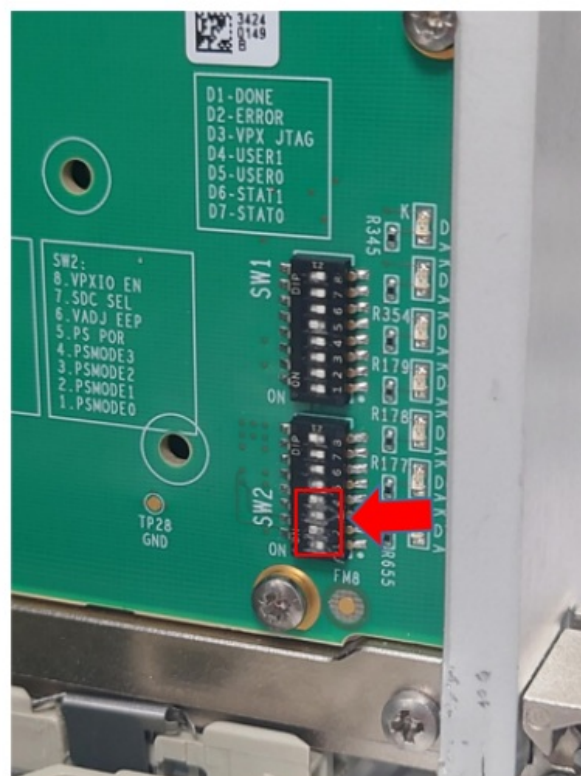


Figure 9 : microswitch SW2 positions to boot from the micro-SD card

6. Open a terminal on the USB-Serial port with the following configuration: 115200bps, 8bits, No parity, 1bit Stop, Flow Control OFF

7. Power on the ADM-VA601. U-Boot and Kernel will load:

Uboot verification command: sf probe 0 0 0 AValance device details will be displayed.

Kernel verification command: mtdinfo configuration memory partitions will be displayed.

8. Copy the files in SD card to memory using the following commands.

```
cd /run/media/mmcblk0p1
flashcp BOOT.BIN /dev/mtd0
flashcp image.ub /dev/mtd1
flashcp boot.scr /dev/mtd2
```

9. Power off the ADM-VA601.

10. Enable QSPI boot mode by changing SW2 switches positions: Mode Switch SW2 [4:1]—>ON, ON, OFF, ON

11. Power on the ADM-VA601 and the system should boot from memory.

```
(3.742)*** AVALANCHE TECHNOLOGY ***
(3.794)*** BOOT MODULE ***
(3.846)*****
(3.898)FlashID=0xE6 0x21 0x29 0x1
(3.954)AVALANCHE ID
(3.999)HP Dual-Quad SPI - 3V
(4.047)40C~125C, 2Gbits
(4.361)0.769 ms: PDI initialization time
(4.420)***Loading Image#: 0x1, Name: lpd, Id: 0x04210002
(4.488)---Loading Partition#: 0x1, Id: 0xC
(76.754) 72.178 ms for Partition#: 0x1, Size: 2816 Bytes
(81.593)---Loading Partition#: 0x2, Id: 0x0
(92.488) 7.040 ms for Partition#: 0x2, Size: 65440 Bytes
PSM Firmware version: 2022.2 [Build: Oct 7 2022 04:56:16 ]
(99.930)***Loading Image#: 0x2, Name: pl_cfi, Id: 0x18700000
(105.175)---Loading Partition#: 0x3, Id: 0x3
(209.223) 100.108 ms for Partition#: 0x3, Size: 852800 Bytes
(211.710)---Loading Partition#: 0x4, Id: 0x5
(876.088) 660.440 ms for Partition#: 0x4, Size: 1071344 Bytes
(878.632)***Loading Image#: 0x3, Name: cpm, Id: 0x04218007
(883.763)---Loading Partition#: 0x5, Id: 0x6
(889.119) 1.417 ms for Partition#: 0x5, Size: 7072 Bytes
(892.639)***Loading Image#: 0x4, Name: fpd, Id: 0x0420C003
(897.708)---Loading Partition#: 0x6, Id: 0x8
(902.198) 0.554 ms for Partition#: 0x6, Size: 1344 Bytes
(906.862)***Loading Image#: 0x5, Name: apu_subsystem, Id: 0x1C000000
(912.500)---Loading Partition#: 0x7, Id: 0x0
(919.243) 2.806 ms for Partition#: 0x7, Size: 28096 Bytes
(921.478)---Loading Partition#: 0x8, Id: 0x0
(931.737) 6.321 ms for Partition#: 0x8, Size: 63440 Bytes
(933.971)---Loading Partition#: 0x9, Id: 0x0
(1044.158) 106.251 ms for Partition#: 0x9, Size: 1068384 Bytes
N(11CE:88A)* r*n*in* *nooilllx Lers: Sie*con
*****
(1051.436)22.746 ms: ROM Time
(1054.045)Total PLH Boot Time
INFO: BL31: GET_HWNDOFF_PARAMS call success=0
INFO: BL31: fsbl-atf handover success 0.
NOTICE: BL31: Secure code at 0x0
NOTICE: BL31: Non secure code at 0x8000000
NOTICE: BL31: v2.6(debug):xlnx_rebase_v2.6.2022.1_update3-18-g0697efd45
NOTICE: BL31: Built : 03:55:03, Sep 9 2022
INFO: GICv3 with legacy support detected.
INFO: ARM GICv3 driver initialized in EL3
INFO: Maximum SPI INTID supported: 191
INFO: BL31: Initializing runtime services
WARNING: BL31: cortex_a72: CPU workaround for 859971 was missing!
WARNING: BL31: cortex_a72: CPU workaround for 1319367 was missing!
INFO: BL31: cortex_a72: CPU workaround for cve_2017_5715 was applied
INFO: BL31: cortex_a72: CPU workaround for cve_2018_3639 was applied
INFO: BL31: Preparing for EL3 exit to normal world
INFO: Entry point address = 0x80000000
INFO: SPSR = 0x3c9

U-Boot 2022.01 (Sep 20 2022 - 06:35:33 +0000)

CPU: Versal
Silicon: v2
Model: Xilinx Versal vck190 Eval board revA (QSPI)
DRAM: 8 GiB
EL Level: EL2
MMC: mmc@f1050000: 0
Loading Environment from SPIFlash... SF: Detected AVALANCHE_2x1Gb with page size 512 Bytes, erase size 12
```

Figure 10 : Petalinux booting from QSPI memory

Contact


- Address: Suite L4A, 160 Dundee Street,

- Edinburgh, EH11 1DQ, UK
- Telephone: +44 131 558 2600
- Fax: +44 131 558 2700
- email: sales@alpha-data.com
- Website: <http://www.alpha-data.com>
- Address: 10822 West Toller Drive, Suite 250
- Littleton, CO 80127
- Telephone: (303) 954 8768
- Fax: (866) 820 9956 – toll-free
- email: sales@alpha-data.com
- Website: <http://www.alpha-data.com>

FAQ

- **Q: What software tools are required for the ADM-VA601 Software Development Kit?**
 - A: Vivado 2022.2 and PetaLinux 2022.2 are required for the FPGA and Linux image projects, respectively.
- **Q: Can I modify the Vivado project after generation?**
 - A: Yes, the Vivado project can be modified using Vivado's GUI.

Documents / Resources

	<p>ALPHA DATA ADM-VA601 Software Development Kit [pdf] User Guide</p> <p>ADM-VA601 Software Development Kit, ADM-VA601, Software Development Kit, Development Kit</p>
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References

- [User Manual](#)

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ADM-VA601, ADM-VA601 Software Development Kit, ALPHA DATA, Development Kit, Software Development Kit

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