ALLEGRO microsystems APEK85110 Half Bridge Driver Switch Board User Manual

**microsystems APEK85110 Half Bridge Driver Switch Board
User Manual**

Contents

Description

The Allegro APEK85110 Half-Bridge Driver Switch Board is a demo board containing two AHV85110 GaN FET drivers and two GaN FETs in a half-bridge configuration.
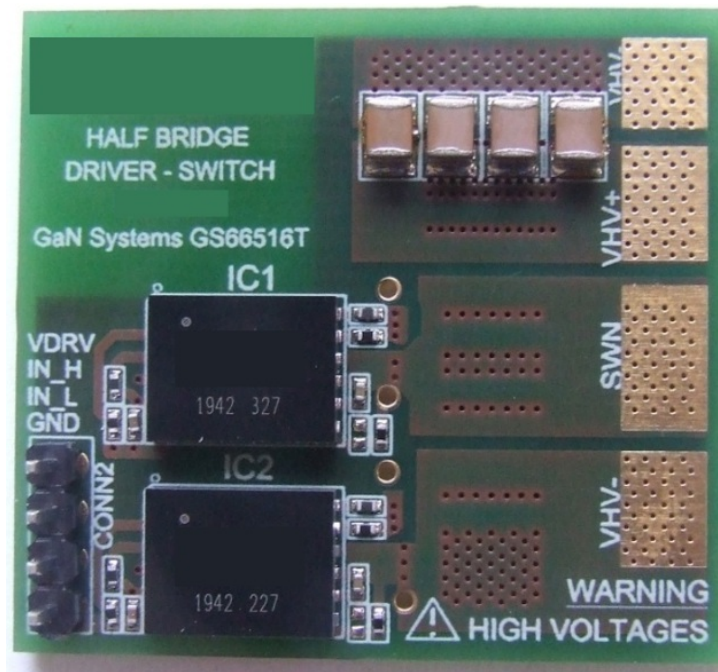
Figure 1: APEK85110 Evaluation Board

The APEK85110 can be used to perform double pulse tests (see Double Pulse Test section) or to interface the half-bridge to an existing LC power section, as shown below.

The isolated AHV85110 driver does not require secondary-side power or bootstrap components. Gate drive power is supplied to the secondary side from the primary-side supply voltage, VDRV. The amplitude of the gate drive can be varied by varying VDRV between 7 and 15 V.

The Allegro Half-Bridge Driver Switch Board is available in two versions: APEK85110 Top-Cooled: Uses GaN Systems GS66516T devices mounted on the bottom side of the PCB where a heat sink if used, can be mounted directly onto the transistors.

APEK85110 Bottom-Cooled: Uses GaN Systems GS66508B devices mounted on the top side of the PCB where a heat sink if used, can be mounted on the bottom side of the PCB, and heat is transferred through the PCB.

Quick Start Guide
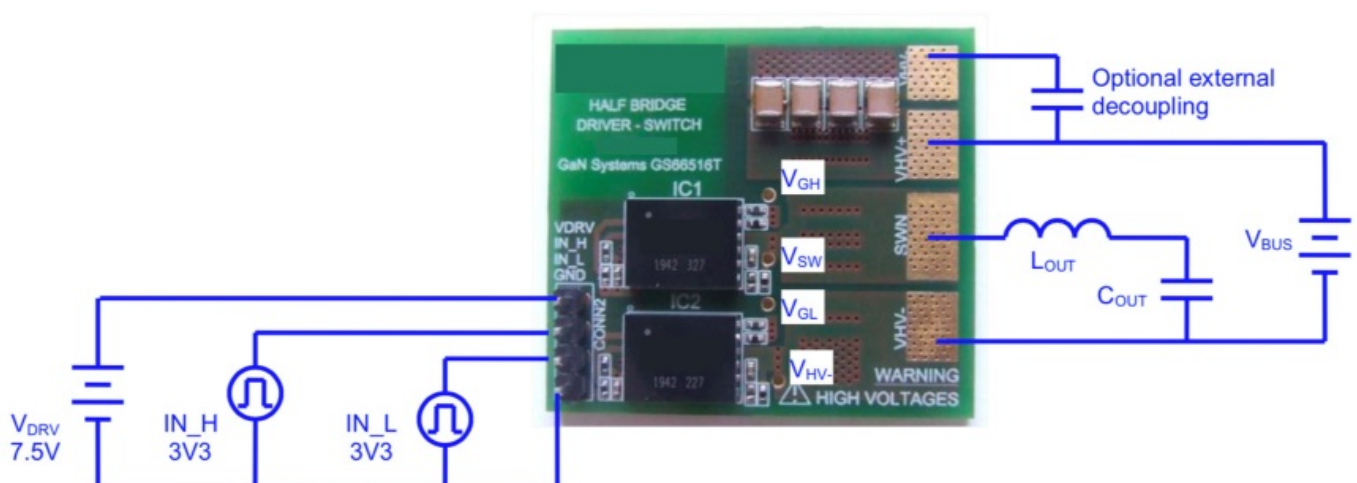
Figure 2: APEK85110 Quick Start

1. Apply VDRV = 7.5 V

2. Apply input gate signals, with adequate dead time, to the IN_L and IN_H inputs.

3. Convenient test points are located on the test board as shown above. A suitable differential oscilloscope should be used to monitor the high-side gate signal from VGH to VSW.

Gate Pull-Up and Pull-Down Resistors

The AHV85110 gate driver has independent outputs for the gate pull-up and gate pull-down allowing control of the on and off rise and fall times. The default values for these resistors are:

- OUTPUT: R1 and R5 = 10 Ω
- OUTPD: R3 and R7 = 1 Ω

These values can be modified to suit the application.

PCB Layout

APEK85110 Top-Cooled

Figure 3: APEK85110 Silkscreen and Component Placement

Figure 4: APEK85110 Top-Side Copper (L) and Layer 2 Copper (R)
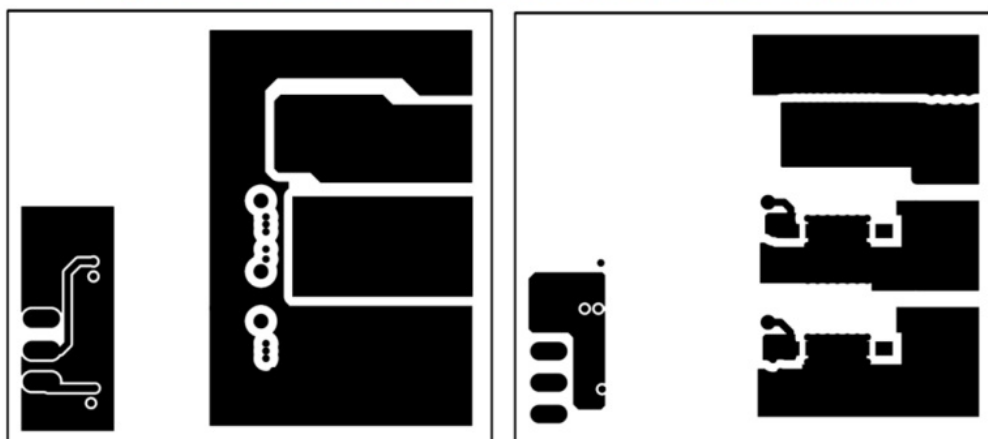
Figure 5: APEK85110 Layer 2 Copper(L) and Bottom-Side Copper (R)
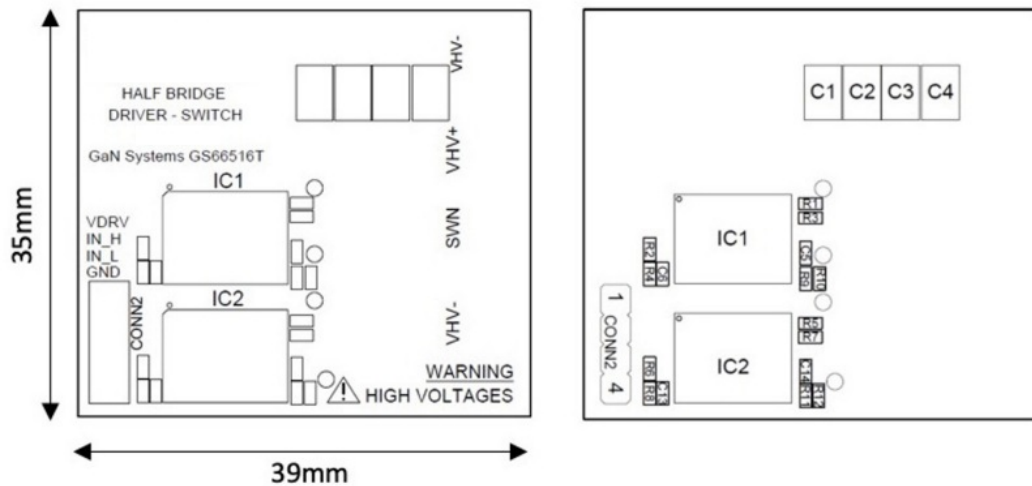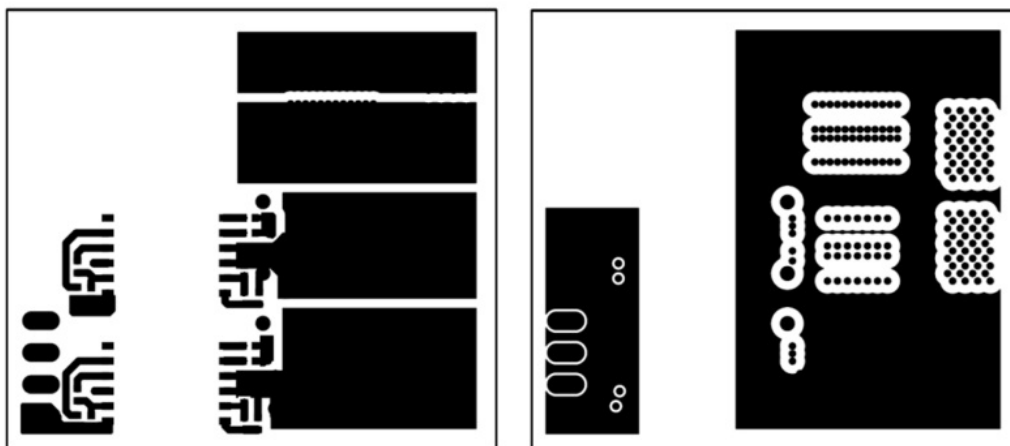
Figure 6: APEK85110 Silkscreen and Component Placement

Figure 7: APEK85110 Top-Side Copper (L) and Layer 2 Copper (R)

Figure 8: APEK85110 Layer 2 Copper(L) and Bottom-Side Copper (R)
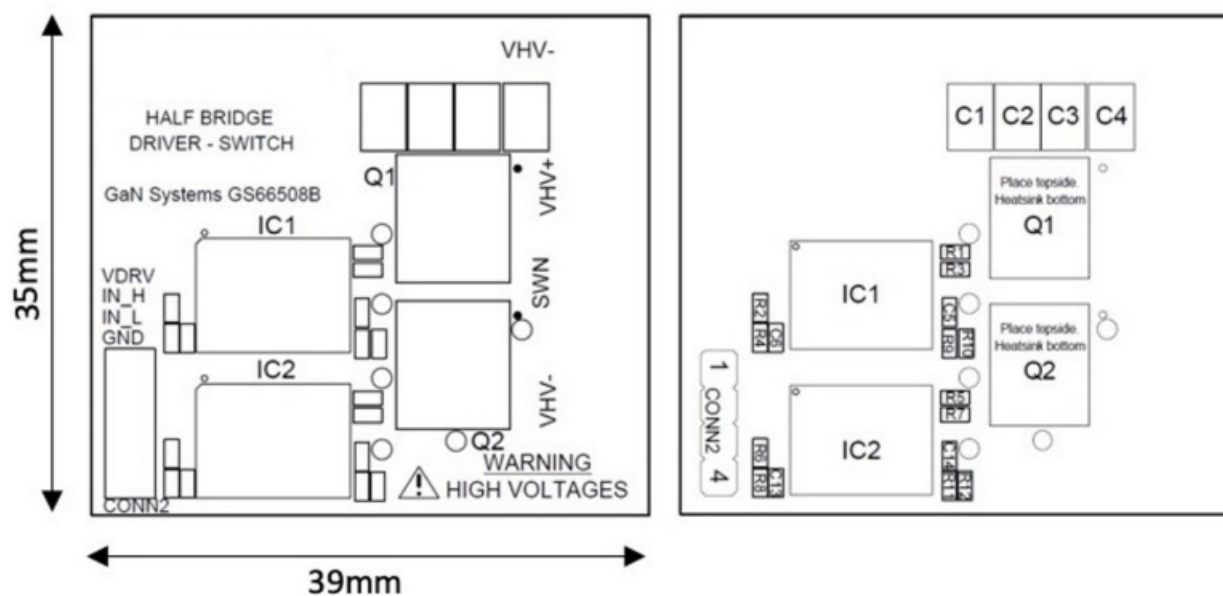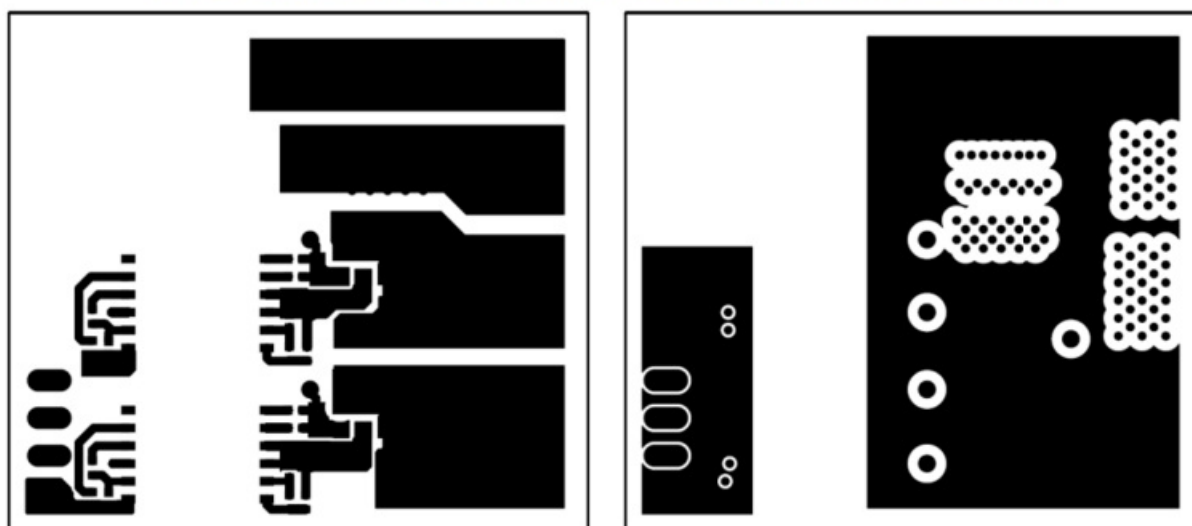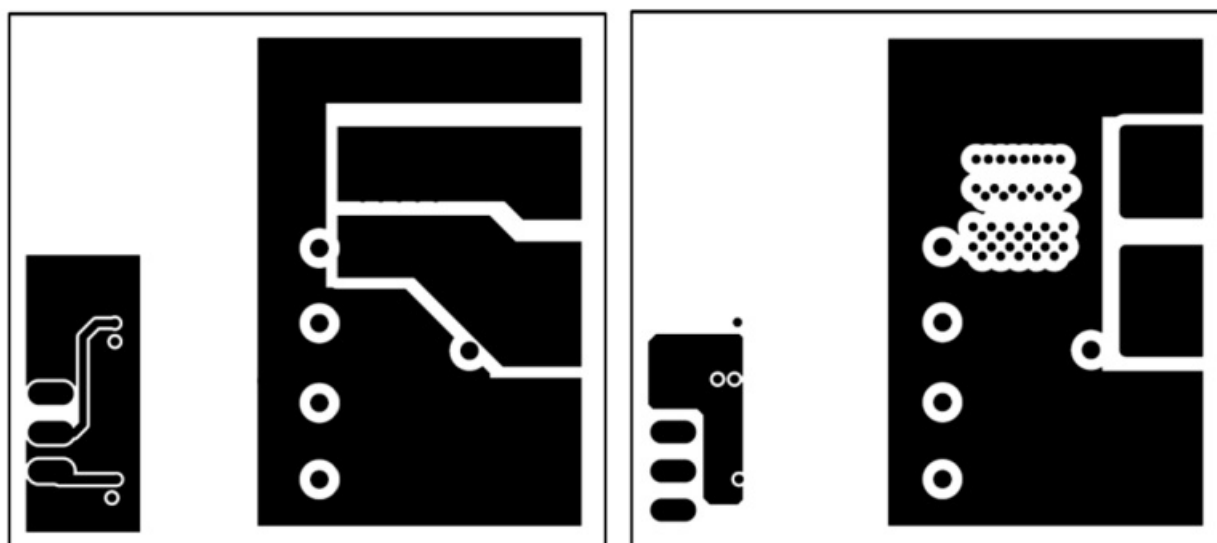
Figure 8: APEK85110 Layer 2 Copper(L) and Bottom-Side Copper (R)

APEK85110 SCHEMATIC

Figure 9: APEK85110 Schematic

APEK85110 Half Bridge Driver Switch Board Bill Of Materials

Table 1: Bill of Materials

Item	Ref Name	Description	Value	Comment
1	C1, C2, C3, C4	CAP 100 nF 630 V X7R C 1210	100 nF	
2	C5, C14	22 nF, 16 V, CAP, CER, X7R, S0402	22 nF	
3	C6, C13	CAP, CER,1 µF, 25 V, X5R, S0402	1 µF	
4	CONN2	CONN, HDR, 4WAY, 2P54	4WAY, 2P54, VER	
5	HSINK1	HSINK, 33 × 33 × 33mm, Fin, 2.1°C/W	THINK FIN	Suggested heat sink for bottom-cooled
6	IC1, IC2	AHV85110 7.66 × 10 MODULE, V03	AHV85110	
7	Q1, Q2	NGAN GS66516T 650 V 60 A	GS66516T	GS66516T used on HEY-HBDS-G-12A-A
8	R1, R5	RES, SMD, 10R, 0.063W, 1%, S0402	10 Ω	
9	R10, R12	RES, SMD, 0R0, 0.063W, 1%, S0402	0 Ω	
10	R2, R6	RES, SMD, 100K, 0.063W, 1%, S0402	100 kΩ	
11	R3, R7	RES, SMD, 1R0, 0.063W, 1%, S0402	1 Ω	
12	R4, R8	RES, SMD, 1K6, 0.063W, 1%, S0402	1.6 kΩ	
13	R9, R11	RES, SMD, NA, 1%, S0402	n/a	

Double Pulse Test

Theory

The double pulse test is used to evaluate the switching characteristics of a power switch under hard switching but in a safe manner for a low-side switch, the setup is as shown below:
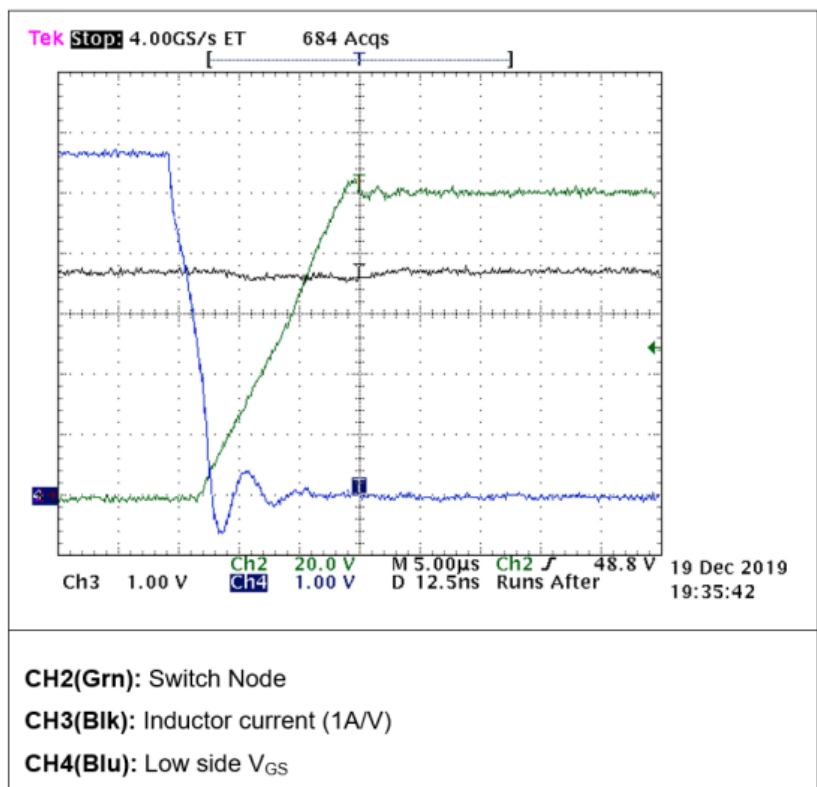
The low-side switch is driven with two pulses as shown below. The high-side switch can be held off or driven with the inverse of the low-side gate switch (with adequate dead time).

Figure 11: Double Pulse Test Waveforms

An inductor is placed in parallel with the high-side switch. The goal of this inductor is to establish the test level current in the low-side switch at the end of the first pulse. The falling edge of pulse 1 is used to examine the hard turn-off characteristics of the switch. The rising edge of pulse 3 is used to examine the hard turn-on characteristics of the switch. By only applying these two pulses, the switches are only on for a very short time and will not overheat.

Test Results

Components:

Drivers:	Allegro AHV85110
Inductor:	Wurth 74437529203471 (470 µH 5.5
RPU:	10 Ω
RPD:	0 Ω
CSEC:	22 nF X7R
Mode:	2

Test Setup

DC Bus Voltage:	100 V
Load Current:	3.6 A
tON_1:	16 µs
tOFF_1:	1 µs
tON_2:	1 µs

Double Pulse Overview: 100 V, 3.8 A

Tek Stop: 4.00GS/s ET   684 Acqs

Ch3 1.00 V   Ch2 20.0 V   M 5.00µs   Ch2 ƒ   48.8 V   19 Dec 2019
               Ch4 1.00 V   D 12.5ns   Runs After   19:35:42

CH2(Grn): Switch Node

CH3(Blk): Inductor current (1A/V)

CH4(Blu): Low side V_{GS}

Hard Switch On: 100 V, 3.8 A

Tek Stop: Single Seq 4.00GS/s ET

Ch3 1.00 V   Ch2 20.0 V   M 5.00µs   Ch2 ƒ   48.8 V   19 Dec 2019
               Ch4 1.00 V   D 12.5ns   Runs After   19:38:49

CH2(Grn): Switch Node

CH3(Blk): Inductor current (1A/V)
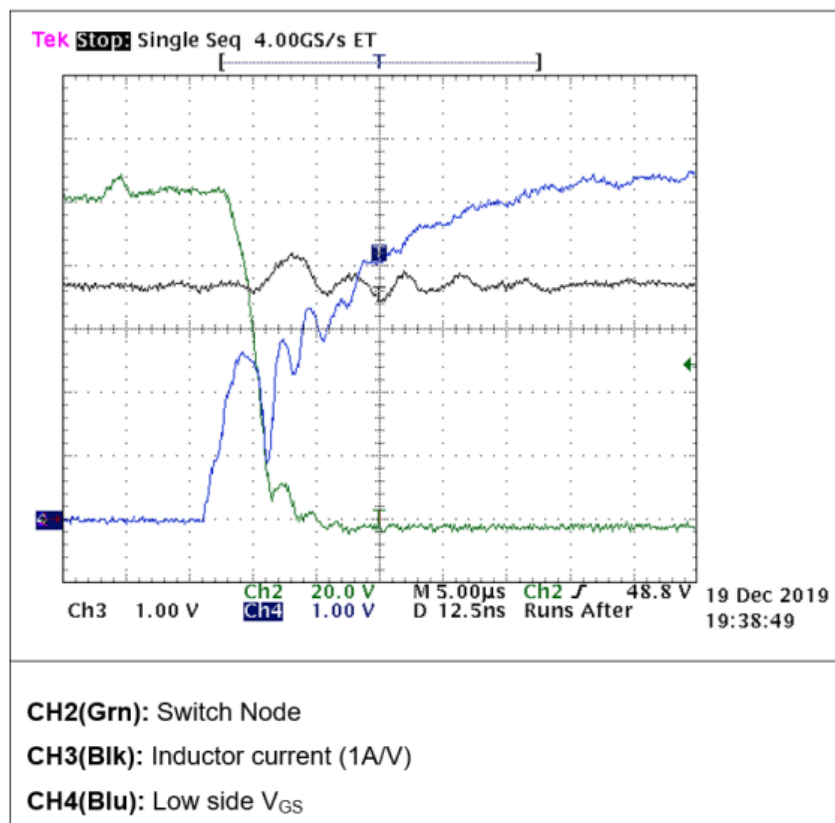
CH4(Blu): Low side V_{GS}

Hard Switch Off: 100 V, 3.8 A
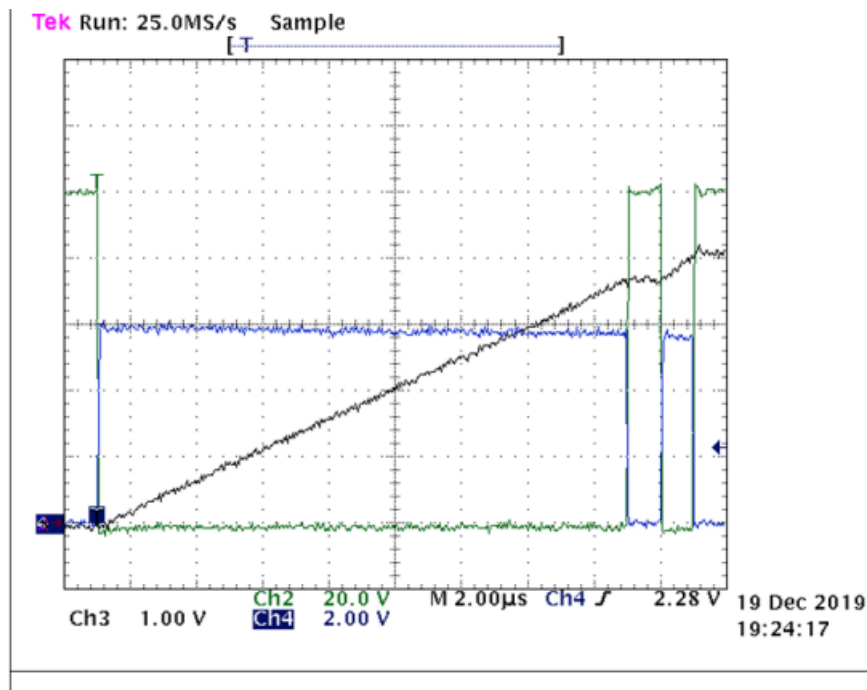
CH2(Grn): Switch node
CH3(BIK): Inductor current (1A/V)
CH4(Blu): Low side Vgs

Documents / Resources

	ALLEGRO microsystems APEK85110 Half Bridge Driver Switch Board [pdf] User Manual APEK85110, Half Bridge Driver Switch Board, APEK85110 Half Bridge Driver Switch Board, Bridge Driver Switch Board, Driver Switch Board, Switch Board

References

- **Allegro MicroSystems | Innovation with Purpose**