Allegro MicroSystems A81411 Evaluation Board Owner's Manual

Contents

Allegro MicroSystems A81411 Evaluation Board

DESCRIPTION
The A81411 Evaluation Board is designed to help system designers evaluate the operation and performance of a power management IC. The A81411 Evaluation Board provides connections to a Buck-Boost Pre-Regulator, 5× Linear Regulators and SPI communications.

FEATURES

- Wide input range: 3.2 to 36 V VIN operating
- 2.2 MHz synchronous buck-boost preregulator (VREG: 5.35 V) with internal compensation
- Five internal linear regulators with fold-back short-circuit protection
  - VUC: 3.3 V or 5 V (selectable by a pin) regulator for microcontroller
  - VLDOA: 5 V (or 3.3 V factory option) general-purpose low-dropout (LDO) regulator
  - VLDOB: 5 V or 3.3 V (selectable by a pin) always-on LDO regulator
  - VLDOP1 and VLDOP2: Two programmed (5 V or 3.3 V) and enabled via serial-port-interface (SPI) LDO regulators with short-to-battery protection for remote sensors
- Two high-voltage enable inputs (ENBAT and ENCAN)

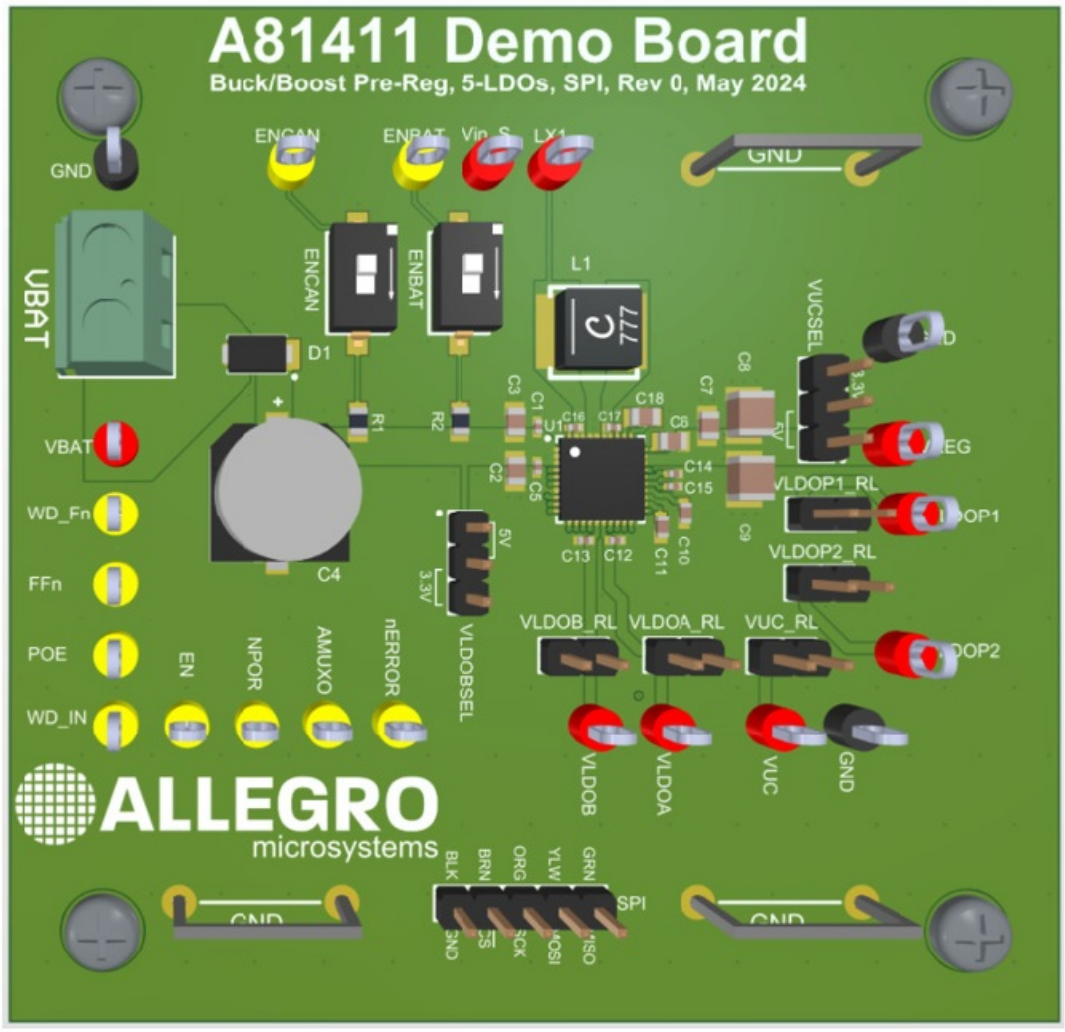

Figure 1: A81411 Evaluation Board

Table 1: A81411 Evaluation Board Configurations

Configuration Name	Part Number	VLDOA Output Voltage	Package
A81411	A81411KEVGTR	5 V	40-pin QFN with thermal pad
	A81411KEVGTR-1	3.3 V	

Table 2: General Specifications

Specification	Min	Nom	Max	Units
Input Operating Voltage	3.2	–	36	V
VIN VLDOB Start Voltage	5.7	6	6.3	V
VIN UVLO Start Voltage	5.72	5.88	6.12	V
VIN VLDOB Stop Voltage	4	–	5	V
VIN UVLO Stop Voltage	2.65	2.9	3.15	V
VIN UVLO Hysteresis	–	2.5	–	V
ENBAT/ENCAN Upper Threshold	2.7	3.2	3.5	V
ENBAT/ENCAN Lower Threshold	2.2	2.6	2.9	V
ENBAT/ENCAN Hysteresis	–	500	–	mV
EN Upper Thresholds	–	–	2	V
EN Lower Thresholds	0.8	–	–	V

USING THE EVALUATION BOARD

This section provides an overview of the connections and configuration options of the A81411 Evaluation Board. Each group of connections highlighted in Figure 2 has a details section below. Figure 2 shows the default jumper positions. The A81411 datasheet contains detailed information on the use and functionality of each pin. Consult the A81411 datasheet for more detailed information than is contained in this user guide.

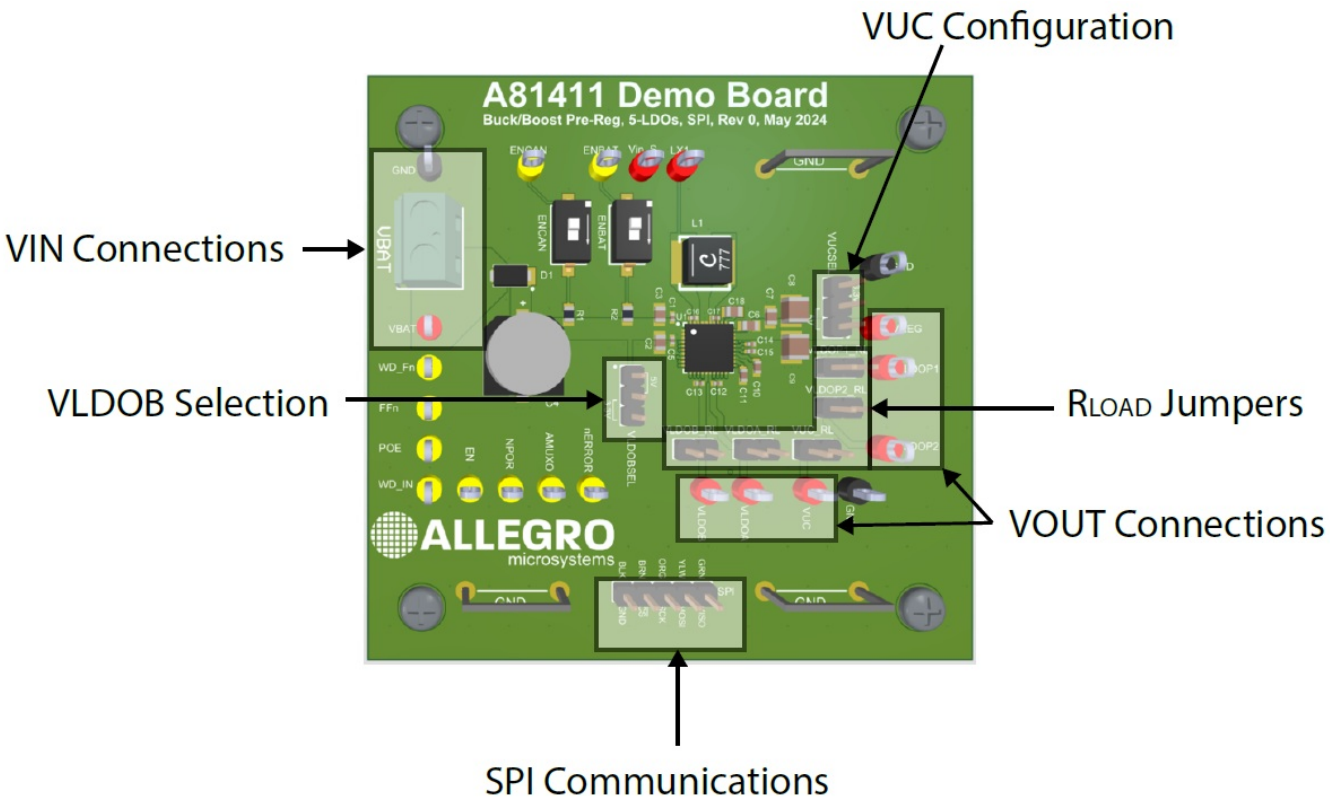

Figure 2: A81411 evaluation board connections

Power Input

Connect a power supply to the green terminal block using two wires and tighten down the screws to clamp the

wires in place. Clip leads can be used on the test points located on either side of the green terminal block. Observe the polarity on the board, connect the VIN to the positive supply terminal VBAT and GND to the negative supply terminal.

Linear Regulator Outputs
All five linear regulators have a test point connected to their output pin and a two pin header for their associated load resistors. While measuring the output voltage, connect the positive probe of the multimeter to the appropriate test point and the negative terminal of the multimeter to a nearby GND connection. To apply the load resistors incorporated on the board, install a two pin jumper on the appropriate two pin header for the desired output load resistor. To measure the output current, remove the two pin jumper and replace it with the two probes of an ammeter.

Output Voltage Configuration
The A81411 has the ability to configure five LDO outputs between either 5 V or 3.3 V outputs. The VUC and VLDOB regulator out-put voltages are pin selectable between 3.3V or 5V. These two regulators each have a three-pin jumper labeled VUCSEL and VLDOB-SEL for easy configuration. For either regulator, place a two-pin jumper between the middle pin and the side marked with either 3.3 V or 5 V to select the output voltage for those regulators.

The VLDOA regulator output voltage is a factory option. Two different A81411 part numbers are available for either the 3.3 V or 5 V option.
The two VLDOP1 and VLDOP2 are selectable for either 5 V or 3.3 V and can be enabled by way of SPI communications.
The VLDOB regulator is an always-on regulator. It starts regulation when the VIN voltage is above the undervoltage threshold, even if none of the available enable pins are high.

SPI Communications
The A81411 has a General User Interface (GUI) for easy communications through the SPI port to a PC using an FTDI cable, down-loadable from the Allegro website. See the datasheet for detailed MCU SPI communication instructions.

Enable
The A81411 Evaluation Board can be enabled by pulling either the EN pin high, the ENCAN pin high, or the ENBAT pin high. For convenience, the ENCAN and ENBAT pins each have a switch to pull either of these pins high and enable the part. The EN pin has a test point to which an external signal such as that from a microcontroller can be used to enable the A81411. The external signal applied to the EN pin must be above 2 V and not more than 5 V.

Diagnostic Outputs
The A81411 incorporates a series of outputs to alert the microprocessor if any faults occur. Each one of these pins have a test point connected to them for easy access. Those signals include a Watchdog Fault (WD_Fn), power on reset (NPOR), a fault flag (FFn) and a gate driver enable (POE).

Switching Frequency
The switching frequency of the pre-regulator is fixed at 2.2 MHz typical, and is decreased to 1.1 MHz if the VIN voltage is increased above 19 V. It can be monitored by connecting an oscilloscope probe to the LX1 test point and GND.

Startup Procedure
To begin using the A81411 Evaluation Board, follow the instructions below and refer to the diagram in Figure 2 or the test point descriptions outlined in the A81411 Test Point Descriptions table.

1. Ensure the VUCSEL & VLDOB jumpers are in the proper positions for the desired output voltage.
2. Install the jumpers required to connect the regulated output load resistors on the A81411 Evaluation Board.

3. Apply an input voltage across the VBAT terminals above UVLO (5.88 V typical) with a minimum supply current of 1.5 A.
4. In addition to VLDOB, which is already operational, provide an enable signal between EN, ENBAT, or ENCAN to activate VREG and the other LDOs.

Table 3: A81411 Test Point Descriptions

Test Point	Description
VBAT	Positive terminal for input voltage connection or connect wires to the VBAT screw down test block. V + on the right.
GND	Negative terminal for input voltage connection or connect wires to the VBAT screw down test block. GND on left.
ENCAN	High level enable for wake by CAN.
ENBAT	Ignition enable input from the key/switch via a series resistor.
Vin_S	Vin_Sense is connected close to the DUT and is used to sense the actual voltage appearing on the input pin
LX1	Switching node of the pre-regulator (2.2 MHz).
VREG	Output voltage of the pre-regulator.
VLDOP1	Output voltage of VLDOP1 regulator (enabled and configured through SPI).
VLDOP2	Output voltage of VLDOP2 regulator (enabled and configured through SPI).
VUC	Output voltage of VUC regulator (Select 3.3 V or 5 V using VUCSEL jumper).
VLDOA	Output voltage of VLDOA regulator (5 V or 3.3 V factory setting).
VLDOB	Output voltage of VLDOB regulator, always ON (Select 3.3 V or 5 V using VLDOBSEL jumper).
nERROR	Active low input used to drive POE low.
AMUXO	Output of the Analog Multiplexer.
NPOR	Reset output to the MCU
EN	Input to enable the A81411 (5 V max).
WD_IN	Watchdog input from MCU.
POE	Power on enable.
FFn	Fault flag, active low.
WD_Fn	Watchdog fault flag, active low.

EVALUATION BOARD PERFORMANCE DATA

The following section provides performance data for the A81411 evaluation board.

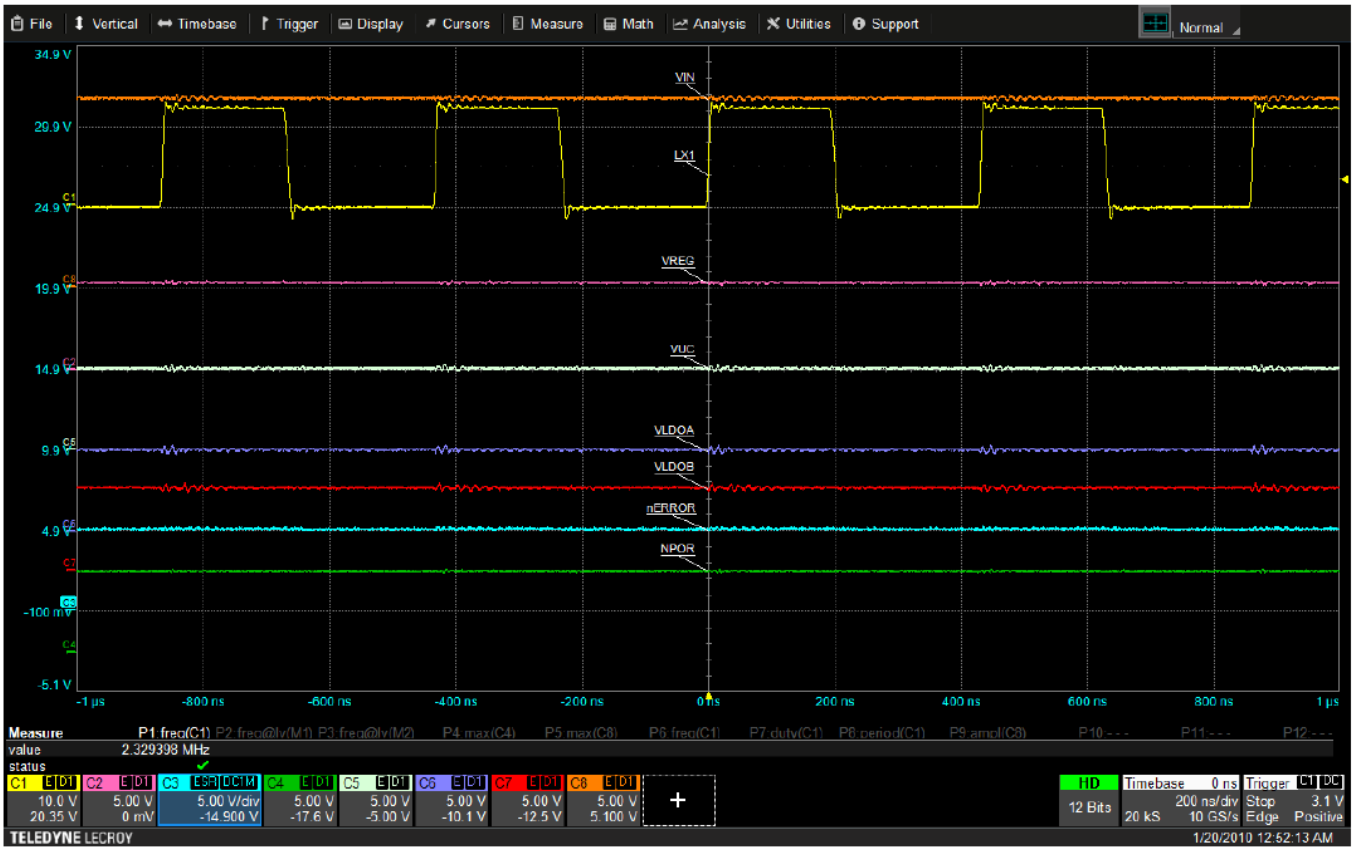

Figure 3: Startup sequence triggered on VIN

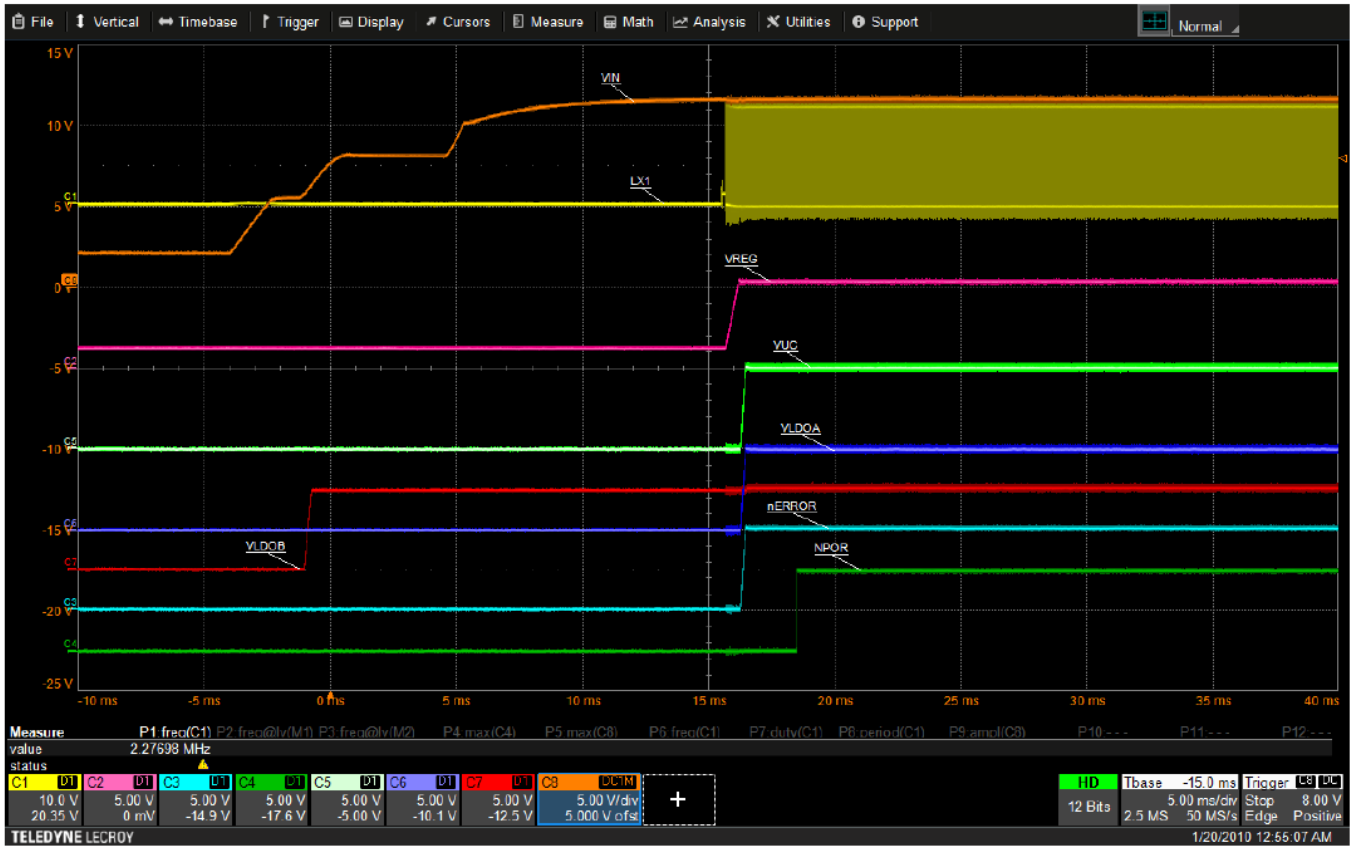

Figure 4: Normal operation, nERROR and NPOR pins remain high

SCHEMATIC LAYOUT

The figure below shows the A81411 evaluation board schematic.

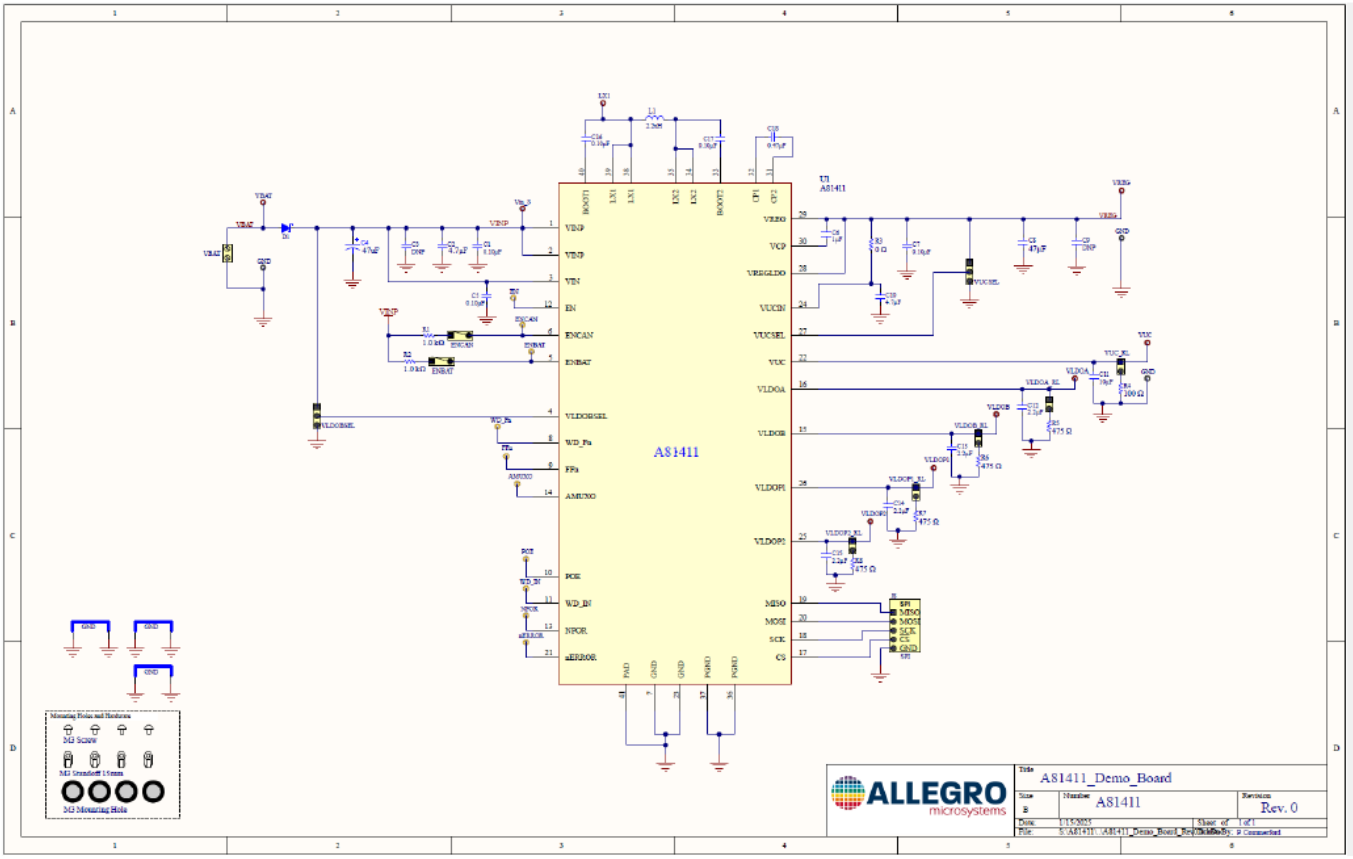

Figure 5: A81411 evaluation board schematic

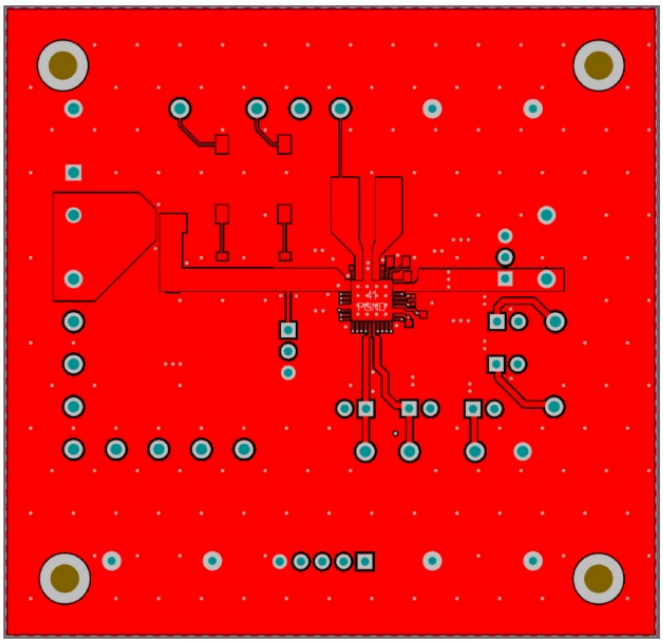

Figure 6: PCB top layer

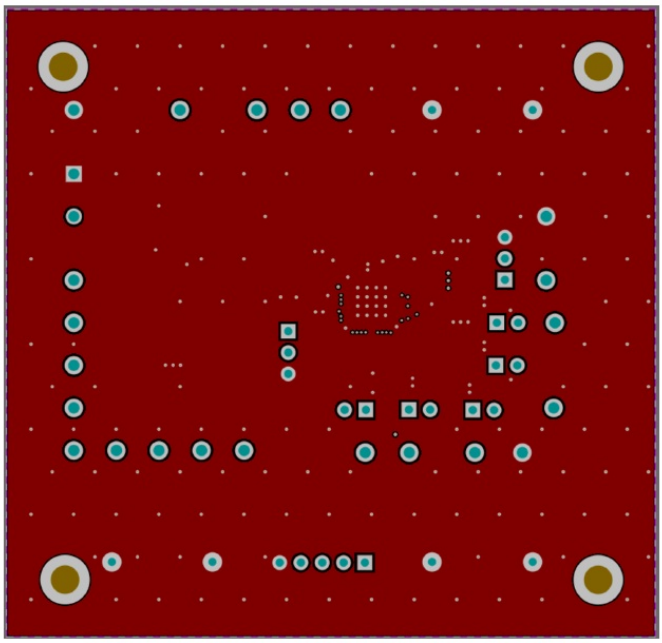

Figure 7: PCB inner layer 1 (PGND plane)

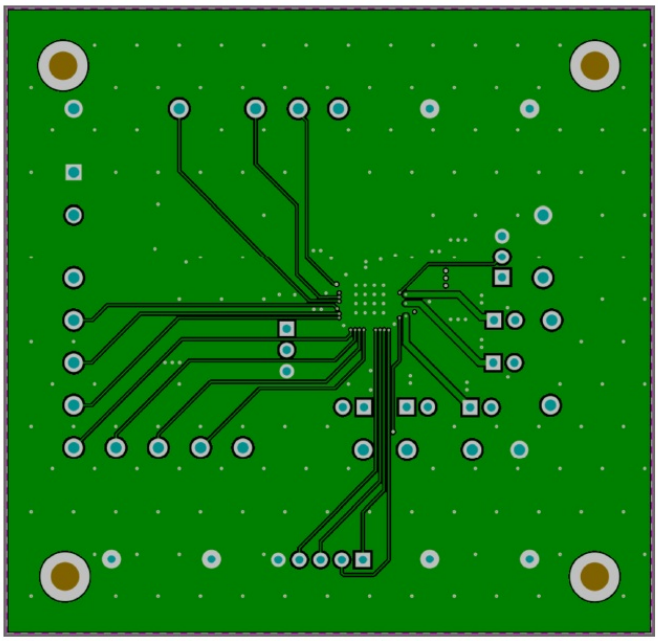

Figure 8: PCB inner layer 2 (PGND plane)

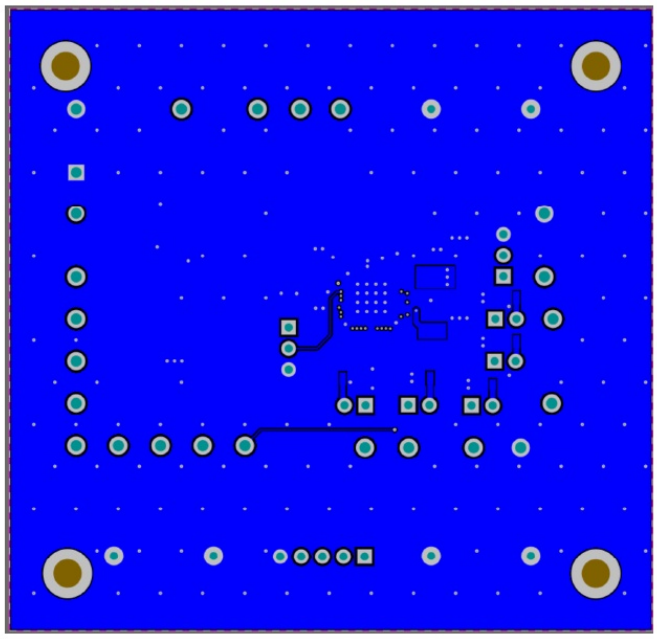

Figure 9: PCB bottom layer

BILL OF MATERIALS

Table 4: A81411 Version Evaluation Board Bill of Materials

ELECTRICAL COMPONENTS					
Designator	**Quantity**	**Comment**	**Description**	**Manufacturer**	**Manufacturer Part Number**
C1, C5, C16, C17	4	0.10 µF	CAP CER 0.1 µF 50 V X7R 0402	Murata	GCM155R71H104KE02D
C2	1	4.7 µF	CAP CER 4.7 µF 50 V X5R 0805	Murata	GRT21BR61H475ME13L
C4	1	47 µF	CAP ALUM 47 µF 20 % 50 V SMD	Nichicon	UBC1H470MNS1GS
C6	1	1 µF	CAP CER 1 µF 25 V X7R 0805	Murata	GRM219R71E105KA88D
C7	1	0.10 µF	CAP CER 0.1 µF 50 V X7R 0805	Murata	GRM21BR71H104KA01L
C8	1	4.7µF	CAP CER 47 µF 10 V X6S 1210	Murata	GRT32EC81A476ME13L
C10	1	4.7 µF	CAP CER 4.7 µF 25 V X5R 0603	Murata	GRM188R61E475KE11D
C11	1	10 µF	CAP CER 10 µF 10 V X5R 0603	Murata	GRT188R61A106KE13D
C12, C13, C14, C15	4	2.2 µF	CAP CER 2.2 µF 16 V X5R 0402	Murata	GRM155R61C225KE11D
C18	1	0.47 µF	CAP CER 0.47 µF 50 V X7R 0805	Murata	GCM21BR71H474KA55L
D1	1	Diode (Schottky)_ DO 221BC	Diode, Schottky, 45 V, 3 A, DO-221BC	Vishay Semiconductors	V4PAL45-M3/I
R1, R2	2	1.0 kΩ	Resistor, 1.0 kΩ, 1/8 W, 1%, 0805	Vishay Dale	CRCW08051K00FKTA
R3	1	0	Resistor, 0Ω, 1W, 2512	Stackpole Electronics	RMCF2512ZT0R00
R4	1	100 Ω	Resistor,100 Ω, 1/8 W, 1%, 0805	Panasonic	ERJ-6ENF1000V
R5, R6, R7, R8	4	475 Ω	Resistor, 475 Ω 1/4 W, 1%, 1206	Panasonic	ERJ-8ENF4750V
U1	1	A81411	Buck-Boost Pre-Regulator, 5 × Linear Regulators and SPI	Allegro MicroSystems	A81411KEVTR-T
L1	1	2.2 µH	Inductor, 2.2 µH, 12.2 A, 10.3 mΩ	Coilcraft	XGL6030-222MEC

OTHER COMPONENTS					
Designator	**Quantity**	**Comment**	**Description**	**Manufacturer**	**Manufacturer Part Number**
GND1, GND2, GND4	3	GND	Ground Bar, 18 AWG Bus Bar, 12 mm Body	Alpha Wire	297 SV005
J1, J2	2	VLDOBSEL. VUCSEL	CONN HEADER VERT 3POS 2.54 MM	Wurth Electronics	61300311121
J3, J4, J5, J6, J7	5	VUC_RL, VLDOA_ RL, VLDOB_ RL, VLDOP1_RL, VLDOP2_RL	CONN HEADER VERT 2POS 2.54MM	Wurth Electronics	61300211121
J8	1	SPI	CONN HEADER VERT 5POS 2.54 mm for SPI with VCC pin	Wurth Electronics	61300511121
MS1, MS2, MS3, MS4	4	M3 screw	PAN HEAD SCREW_M3 X 8 MM CROSS SL	Wurth Electronics	97790803111
STND1, STND2, STND3, STND4	4	M3 Standoff 15 mm	‘Standoffs & Spacers 5.0 HEX 15.0 mm NYLON	Keystone Electronics	25512
SW1, SW2	2	ENCAN, ENBAT	SW, SPT	ITT C&K	SDA01H1SBD
TP1, TP2, TP3, TP4, TP7, TP9, TP10, TP12, TP13	9	‘VBAT, VIN_S, LX1, VREG, VUC, VLDOA, VLDOB, VLDOP1, VLDOP2	Test Point, Red, Through Hole Mount, 1.6 mm	Keystone Electronics	5010
TP5, TP6, TP8	3	GND	Test Point, Black, Through Hole Mount, 1.6 mm	Keystone Electronics	5011
TP11, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22	1	NPOR, nERROR, EN, ENCAN, ENBAT, WD_Fn, FFn, AMUXO, POE, WD_IN	Test Point, Yellow, Through Hole Mount, 1.6 mm	Keystone Electronics	5014
X1	1	VBAT	Terminal Block, 5.08 mm, Vertical, 2 position	TE Connectivity	282837-2
C3	1	DNP	CAP CER 0.1 µF 50 V X7R 0805	Murata	GCM21BR71H104KA37K
C9	1	DNP	CAP CER 22 µF 25 V X7R 1210	Murata	GRM32ER71E226ME15L

RELATED LINKS
Product page: https://www.allegromicro.com/en/products/regulate/regulators/multiple-output-

regulators/a81411
Datasheet: https://www.allegromicro.com/~/media/files/datasheets/A81411-Datasheet

Revision History

Number	Date	Description
–	February 10, 2025	Initial release
1	February 26, 2025	Updated Features section

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Documents / Resources

	Allegro MicroSystems A81411 Evaluation Board [pdf] Owner's Manual A81411, A81411KEVGTR, A81411KEVGTR-1, A81411 Evaluation Board, A81411, Evaluation Board, Board

References

- User Manual